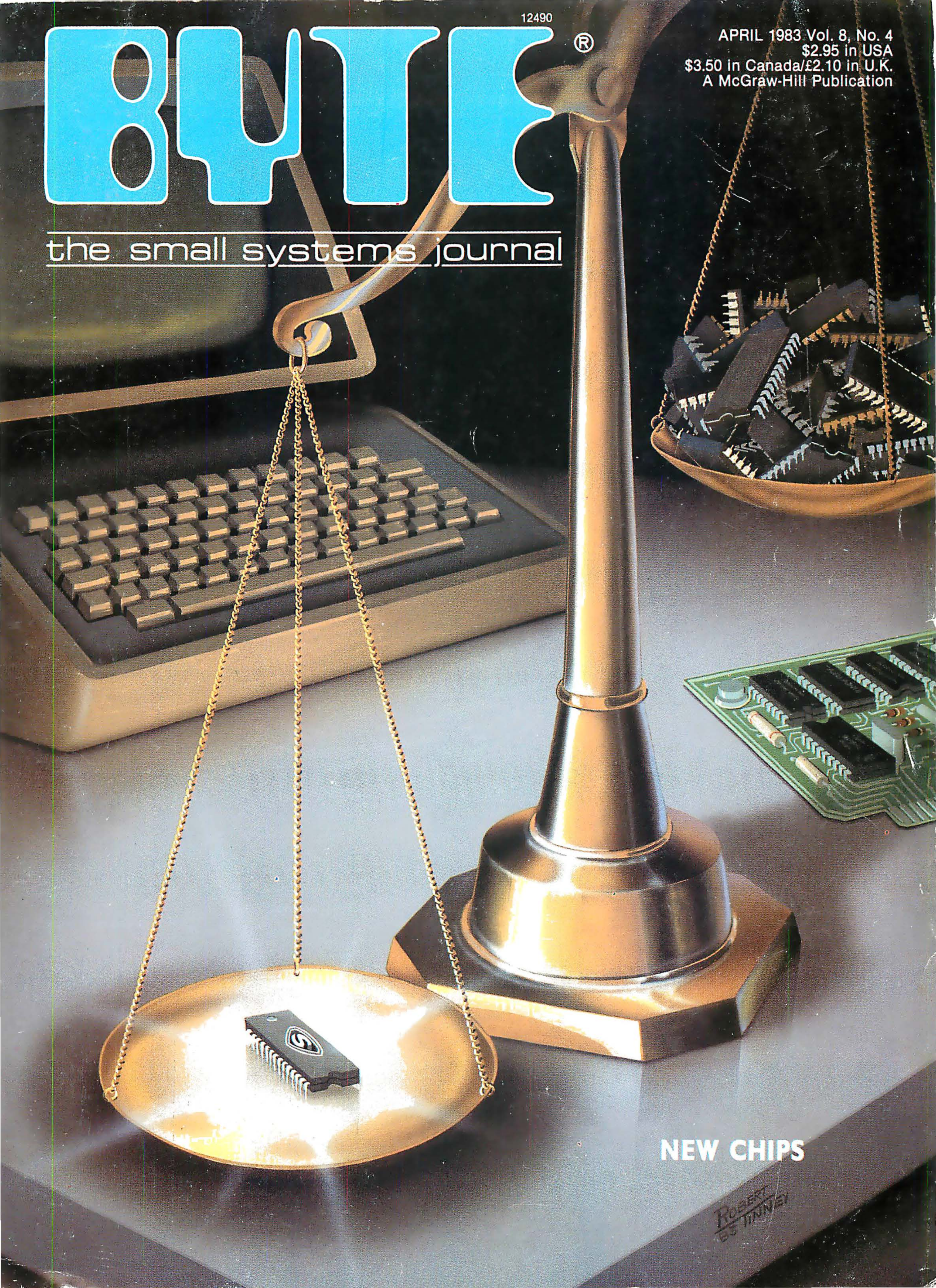
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BYTE®

the small systems journal

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Inside Apple

Apple Computer Inc., 20525 Mariani Avenue, Cupertino, California 95014 Vol. 1 No. 2

For the authorized Apple dealer nearest you, call 800-538-9696 (800-662-9238 in California.)

Fruitful Connections.

There are more people in more places making more accessories and peripherals for Apples than for any other personal computer in the world.

Thanks to those people – in hundreds of independent companies – you can make the humblest 1978 Apple II turn tricks that are still on IBM's Wish List for 1984.

But now we're coming out with our very own line of peripherals and accessories for Apple® Personal Computers.

For two very good reasons.

First, compatibility. We've created a totally kluge-free family of products designed to take full advantage of all the advantages built into every Apple.

Second, service and support.



Now the same kindly dealer who keeps your Apple PC in the pink can do the same competent job for your Apple hard-disk and your Apple daisywheel printer.

So if you're looking to expand the capabilities of your Apple II or III, remember:

Now you can add Apples to Apples.

A joy to behold.

The new Apple Joystick II is the ultimate hand control device for the Apple II.

Why is it such a joy to use?

With two firing buttons, it's the first ambidextrous joystick – just as comfortable for lefties as righties.

Of course, it gives you 360° cursor control (not just 8-way like some game-oriented devices) and full X/Y coordinate control.

And the Joystick II contains high-quality components and switches tested to over 1,000,000 life cycles.

Which makes it a thing of beauty. And a joystick forever.



Gutenberg would be proud.

Old Faithful Silentype® has now been joined by New Faithfuls, the Apple Dot Matrix Printer and the Apple Letter Quality Printer.



So now, whatever your budget and your needs, you can hook your Apple to a printer that's specifically designed to take advantage of all the features built into your Apple. With no compromises.

The 7x9 Apple Dot Matrix Printer is redefining "correspondence quality" with exceptional legibility. With 144x160 dots per square inch, it can also create high resolution graphics.

The Apple Letter Quality Printer, which gets the words out about 33% faster than other daisywheel printers in its price range, also offers graphics capabilities. See your authorized Apple dealer for more information and demonstrations. Because, unfortunately, all the news fit to print simply doesn't fit.



Up the creek without a paddle?

Or lost in space? Or down in the dungeons?

Whatever your games, you'll be happy to know that someone has finally come out with game paddles built to hold up under blistering fire. Without giving you blisters.

Apple Hand Controller II game paddles were designed with one recent discovery in mind:

People playing games get excited and can squeeze very, very hard.

So we made the cases extra rugged. We used switches tested to 3,000,000 life cycles. We shaped them for holding hands and placed the firing button on the right rear side for maximum comfort.

So you'll never miss a shot.

A storehouse of knowledge.

If you work with so much data or so many programs that you find yourself shuffling diskettes constantly, you should take a look at Apple's ProFile,™ the personal mass storage system for the Apple III Personal Computer.

This Winchester-based 5-megabyte hard disk can handle as much data as 35 floppies. Even more important for some, it can access that data about 10-times faster than a standard floppy drive.

So now your Apple III can handle jobs once reserved for computers costing thousands more.

As for quality and reliability, you need only store one word of wisdom:

Apple.



Launching pad for numeric data.

Good tidings for crunchers of numerous numbers:

Apple now offers a numeric keypad that's electronically and aesthetically compatible with the Apple II Personal Computer. So you can enter numeric data faster than ever before.

The Apple Numeric Keypad II has a standard calculator-style layout. Appropriate, because unlike some other keypads, it can actually function as a calculator.

The four function keys to the left of the numeric pad should be of special interest to people who use VisiCalc.® Because they let you zip around your work sheet more easily than ever, adding and deleting entries.

With one hand tied behind your back.



VisiCalc is a registered trademark of VisiCorp. Inc.

Circle 27 on Inquiry card.

How to buy a computer by the numbers.

Introducing the Cromemco C-10 Personal Computer. Only $1785, including software, and you get more professional features and performance for the price than with any other personal computer on the market. We've got the numbers to prove it.

The C-10 starts with a high-resolution 12" CRT that displays 25 lines with a full 80 characters on each line. Inside is a high-speed Z-80A microprocessor and 64K bytes of on-board memory. Then there's a detached, easy-to-use keyboard and a 5¼" disk drive with an exceptionally large 390K capacity. That's the C-10, and you won't find another ready-to-use personal computer that offers you more.

But hardware can't work alone. That's why every C-10 includes software — word processing, financial spread sheet, investment planning and BASIC. Hard-working, CP/M[R]-based software that meets your everyday needs. Software that could cost over $1000 somewhere else. FREE with the C-10. There's really nothing else to buy.

But the C-10's numbers tell only part of the story. What they don't say is that Cromemco is already known for some of the most reliable business and scientific computers in the industry. And now for the first time, this technology is available in a personal computer.

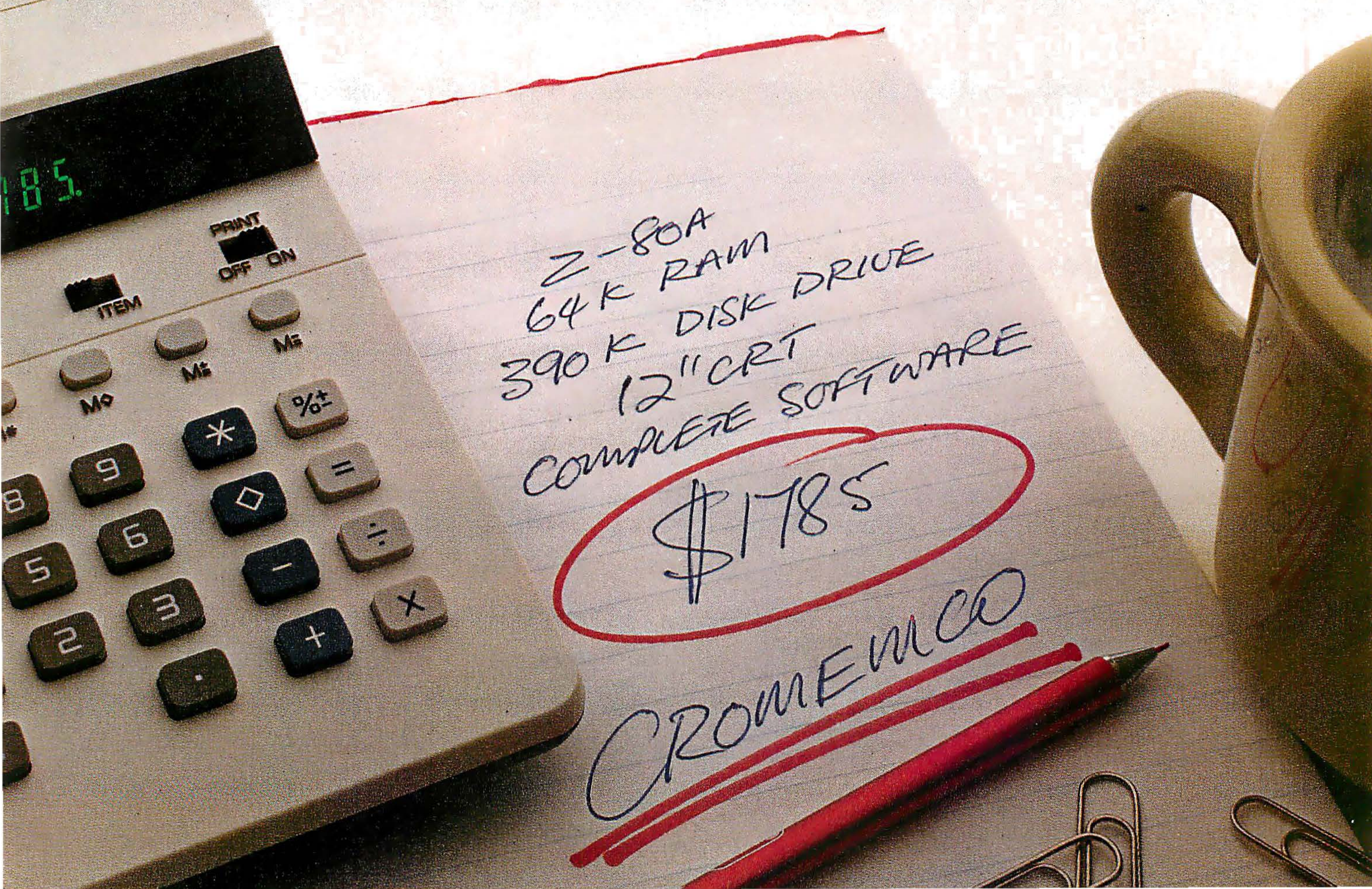
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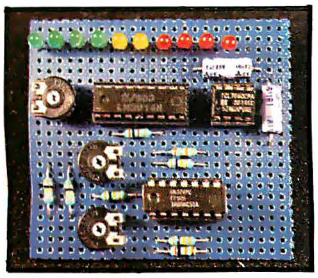
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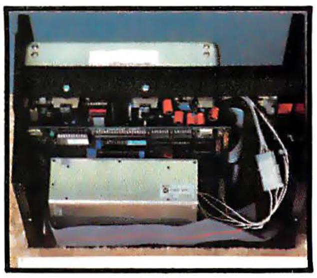
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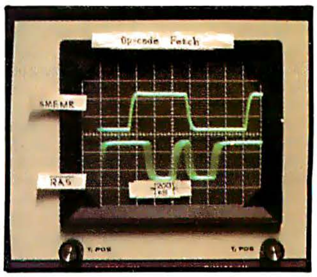
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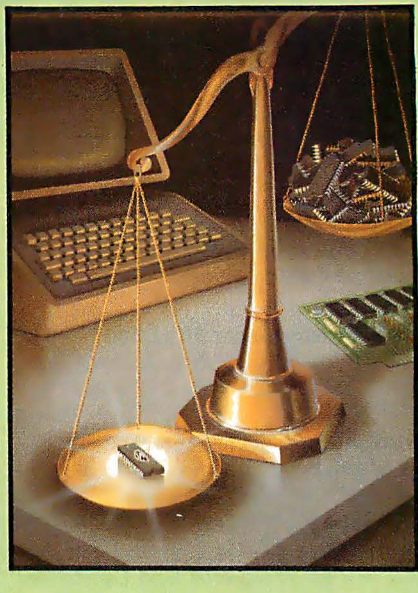
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In This Issue

Innovations in microprocessor and support chips are closing the gap between the speed and power of minicomputers and that of micros. As Robert Tinney's cover illustrates, the scales are tipped in favor of the 16-bit chips. "The National Semiconductor NS16000 Microprocessor Family" by Glenn Leedy introduces you to the NS16032 processor and its related chips. "Design Philosophy Behind Motorola's MC68000" by Thomas W. Starnes begins a multi-part study of the heart of machines such as the Lisa and the Radio Shack Model 16. In "Intel's 80186," Tony Zingale describes this new chip that combines the functions of the 8086 and several support chips in one device. "The CRT 9007 Video Processor and Controller" by Brian Cayton and Mort Herman discusses a sophisticated chip that greatly simplifies the design of smart terminals. Steve Levine looks at "Super Graphics Hardware from NEC." "The Intel 8087 Numerics Processor Extension" by R. B. Simington describes the theory and use of this coprocessor chip to speed up numeric computations on 8086/8088-based computers. In the first BYTE West Coast report, Phil Lemmons brings us news of the way in which software houses are responding to the new advances in hardware. Steve Ciarcia tells you how to "Build an RS-232C Breakout Box." Plus our regular features.

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Editorial

The New Generation of Human-Engineered Software

Gregg Williams, Senior Editor

Apple's new Lisa epitomizes the state of the art in computer sophistication and ease of use. Its integrated software and mouse make this machine a harbinger of what's in store for microcomputers. These new advances mean serious business.

Software companies, for one, appear to be staking their future on products that feature video windows, which allow various projects to appear on the video screen simultaneously, and the mouse, a hand-held box-shaped device that provides an alternative to the computer keyboard. Many new products announced in the past few months are incarnations of what has become known as integrated software. The microcomputing industry is at the threshold of a new trend in user-friendly, human-engineered software—a trend spurred by new technologies and rising product development costs.

New technologies, particularly 16-bit processors and inexpensive computer memory, make more sophisticated software possible. Increased sophistication, however, means higher development costs, which are inevitably passed on to the consumer. Manufacturers, however, see a solution in easy-to-use software. By making such software, they expect to reach a boarder market base; with more potential buyers, the price per unit remains generally affordable.

Why Human-Engineered Software?

This move toward easy-to-use software is the result of a chain of events and influences. We begin with the 16-bit microprocessors, which have been around for several years. Their main contribution is that they have given the ambitious programmer some elbow room. Eight-bit processors are inherently limited by their 64K-byte address space and this in turn imposes restrictions on a programmer's creativity. Granted, clever hardware design and programming can often get around this storage problem, but only up to a point. On the other hand, with 16-bit (and larger) microprocessors capable of addressing millions of bytes of data, programmers have ample room in which to do their work.

The second link in this chain of events is the decreasing cost of mass storage devices and, in particular, computer memory. Only within the last year has memory become inexpensive enough to be used without manufacturers worrying too much about how additional memory will increase the price of the unit. Now that larger memories are affordable and are becoming standard, software companies must decide how they'll use the extra memory to its maximum potential. This brings us to the third link in this chain, which involves a choice to be made by software developers: they can create either computationally more powerful programs or easier-to-use programs. Both options have their advantages, but most companies are going with the latter for one reason: they are courting the average person who is being introduced to computers and their many uses through advertisements on television and in the print media. These people are the new computer users.

Why is this new computer user so important? First of all, the general public is just becoming aware of software and how it can make a computer work for them. Thinking that a lucrative software market is

beginning to open, each company understandably wants to get its foot in the door first with these new users. These companies are hoping that once people buy one of their packages, they are likely to consider them for their future software needs.

The far more compelling reason for courting this new user via easy-to-use software is cost. As the complexity of software goes up, so do the costs associated with designing, programming, testing, and documenting it. To keep these added costs from increasing the product's price and decreasing its potential market, software houses have realized that they must expand their market. Programs using current software technology will sell to only those people who currently use microcomputers. If, on the other hand, software designers use this extra power to make programs that are both powerful and easy to use, they can expect to sell to the potentially huge market of "software-hungry" users, thus vastly increasing the market for their product. The extra production costs would (they hope) be spread over such a large group that the extra cost per program sold would rise only slightly.



Prototype of Visicorp's Visi On integrated applications environment. Note the multiple video windows and mouse. Since this photo was taken, Visicorp has changed to a two-button mouse.

The Big Question

The big question is "What makes software easy to use?" Microsoft and Visicorp are firmly committed to the mouse and the desktop-manager concept as the answer. Microsoft will incorporate a mouse and window-management system into advanced versions of its Multitool series of packages (Multiplan is its first such package). Visicorp stole some of Apple's thunder when it previewed Lisa-like features on the IBM Personal Computer at Comdex last fall with a package called Visi On (see photo). Visi On, which is billed as an "integrated applications environment," has a two-button mouse and can support multiple tasks running in separate windows. Note that these software companies are putting great emphasis on a *hardware* device (the mouse) that will add between $150 and $250 to the cost of some of their products; this fact alone indicates the depth of these companies' commitment to the future.

However, the real answer to the question posed in the previous paragraph is that nobody knows what will make software easy to use. Apple, Microsoft, and Visicorp each has its own option. Other companies, of course, have other solutions (for an excellent discussion of some different plans, see Phil Lemmons' BYTE West Coast, "Hard Choices for Software Houses," on page 242).

The air is already filled with claims and promises about the merits of each company's products, but nobody *knows* what makes software easy to use; the final answer will be in what the people buy. ■



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New Chips for Dynamic Memory Fans

I enjoyed Rob Belics's excellent article, "Practical Dynamic Memory System Design" (December 1982 BYTE, page 372). Your readers may like to know about two newer chips that have made dynamic memory much easier to use: the 4164 and the 6883.

The 64K- by 1-bit 4164 costs about the same per bit as the 16K- by 1-bit 4116 but requires only a single +5-V supply and uses less power and board space. The single power supply feature eliminates the need, in most systems, for an expensive three-voltage power supply and the chance that chips might be fried by application of supply voltages in the wrong order. The smaller memory cells make the 4164 more sensitive to alpha-radiation-induced random bit changes, but this happens infrequently enough that it is not much of a problem for most applications.

The Motorola 6883 synchronous address multiplexer makes interfacing dynamic memory to the 6809 microprocessor almost as easy as hooking up static memory. It handles all $\overline{CAS}$ and $\overline{RAS}$ timing, address multiplexing, and memory refresh. It can also interface the 6809 to Motorola's 6847 video display generator (as in the Radio Shack Color Computer) and provides all system timing so that dynamic memory refresh and display refresh are transparent.

Both the 4164 and the 6883 are well worth knowing about for anyone interested in dynamic-memory system design.

David Nye
209 West Lowe's Creek Rd.
Eau Claire, WI 54701

Turning on the 4116

I feel I must point out an important omission from Rob Belics's article "Practical Dynamic-Memory System Design" in regard to power supplies for the 4116 DRAM (dynamic random-access read/write memory) chip. Mr. Belics briefly describes these as "three separate power-supply voltages that must first be applied in a certain order." I searched the article carefully, and Mr. Belics never tells us in what order these supplies must be turned on and off.

In the April 1981 "Ask Byte" column (page 328), Steve Ciarcia states, "The most important thing to remember when designing any computer that uses 4116s is that the power-supply voltages must be turned on and off in sequence. To keep from blowing the 4116 on power-up, the −5-V supply must be turned on before the +5-V and +12-V supplies. On power-down, the −5 and +12 are removed. . . . the sequence can be accomplished through the time constants of the power supply itself. . . ."

Charles Reeves Jr., Physicist
Nuclear Division
Union Carbide
270 Park Ave.
New York, NY 10017

Multidos Update

Once again, the work of a software developer has outstripped the publishing process and an update is needed to my review "Multidos: A New TRS-80 Disk Operating System" (December 1982 BYTE, page 392).

The price of Multidos has increased from $79.95 to $99.95. There is also a new, $39.95 version called ZDOS; although not as full-featured as Multidos, it provides double-density support and SUPERBASIC (write to Cosmopolitan Electronics, 5700 Plymouth Rd., Ann Arbor, MI 48105, for full details). The additional $20 charge for Multidos buys you a disk sector and file editor or ZAP utility, a disk-drive timer utility, a tape-to-disk conversion utility, and a RAM (random-access read/write memory) test utility. The DOS part of Multidos version 1.6 now includes two-sided drive support, a PATCH command, a RESTOR command to recover a file deleted with the KILL command, a CAT (catalog) command that reads the directory of almost any Model I or III disk, and many additional options for the original commands.

Multidos is now claimed to support disk I/O (input/output) at 4.7 MHz, if you have a clock speedup that allows this.

SUPERBASIC, the disk BASIC that comes with Multidos, has added commands to remove REM statements; pack BASIC program lines together while preserving program logic; and save the current BASIC program in memory while working on another program, then return to the original program (or append it to the new one).

Vernon Hester, the author of Multidos, has released one newsletter so far and promises to publish patches in 1983 that will enable some popular software to run under Multidos.

Let me close by saying that I have found Multidos to stand up very well to over a year's use; it is fast and and reliable and provides a very flexible BASIC development environment.

Rowland Archer Jr.
5420 Loyal Place
Durham, NC 27713

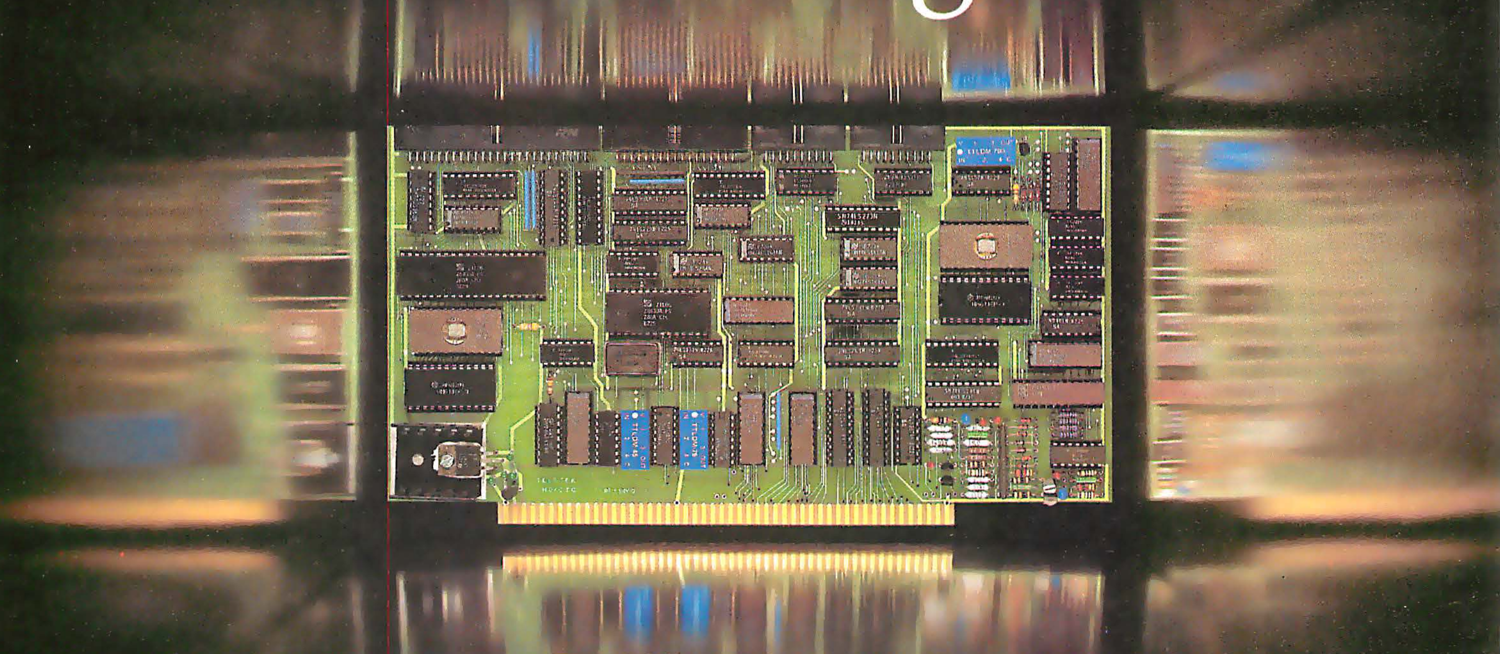
MDBS Takes Issue with User's Column

In the December 1982 BYTE "User's Column" (page 222), Jerry Pournelle notes that Micro Data Base Systems Inc. is working on enhancing the BDS Compiler. This new C compiler, called C', has been available for several months. Perhaps its most notable traits are its production of extremely compact object code and its relatively fast execution and compilation.

I would like to correct several misimpressions conveyed in Dr. Pournelle's column. First, Micro Data Base Systems Inc. is not a "bunch of Purdue University people." The company's management and staff of over 100 persons are not employees of Purdue University. While a number of our employees hold bachelors, masters, and doctorate degrees from Purdue, many others received training at other equally fine institutions.

A second error pertains to our database management product, MDBS. Dr. Pournelle states that "MDBS and the CODASYL database systems are *hierarchical* in structure." This is incorrect. Systems based on the CODASYL approach are not at all limited to hierarchical architectures. Indeed, the flexibility provided by CODASYL-network structures was a major advance over hierarchical systems. Furthermore, MDBS should not be confused with either CODASYL-network systems or hierarchical systems. MDBS is a post-relational system of the extended-network variety, which means that it overcomes many limitations of the old-time hierarchical, relational, and CODASYL-network approaches to database management.

Bored Waiting? Here's The Board You've Been Waiting For.



A hard disk and cartridge tape controller together on one board? Magic? Not really. It's Teletek's HD/CTC. The hard disk and cartridge tape drive controller provide the support necessary to interface both rigid-disk drives and a cartridge tape deck to the S-100 bus.

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- Controller communications with the host processor via 2K FIFO at any speed desirable (limited only by RAM access time) for a data block transfer. Thus the controller does not constrain the host processor in any manner.
- Two 28-pin sockets allowing the use of up to 16K bytes of on-board EPROM and up to 8K bytes of on-board RAM.
- Individual software reset capability.
- Conforms to the proposed IEEE-696 S-100 standard.
- Controller can accommodate two rigid-disk drives and one cartridge tape drive. Expansion is made possible with an external card.

Teletek's HD/CTC Offers A Hard Disk Controller, Plus Cartridge Tape Controller, All On One Board.

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It should also be pointed out that, unlike MDBS, the many microcomputer file handlers that are very loosely referred to as relational databases have little in common with usual, long-established notions of what constitutes database management. These file handlers do not even begin to approach systems such as IBM's SQL/DS, the de facto standard for relational systems. The limitations of file management are not overcome merely by referring to files as databases.

With respect to MDBS documentation, it must be noted that "A Primer on Data Base Management Systems" by Dr. Clyde Holsapple, cited in the article, is not a component of the MDBS reference manual. It is a separate tutorial that is routinely and quite successfully used in introductory university courses on database management systems at the undergraduate level. We have distributed thousands of copies of the primer in the last few years, and the feedback has been overwhelmingly favorable.

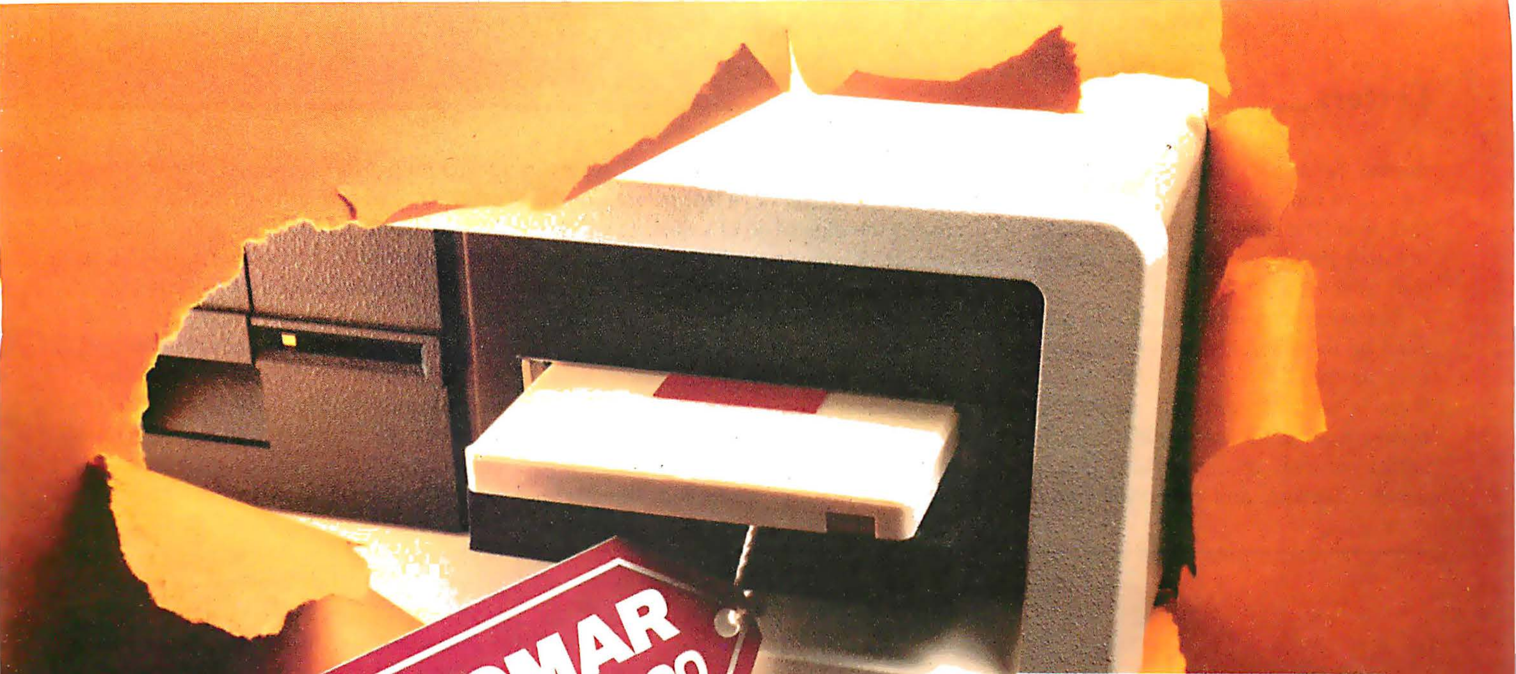
Gary J. Koehler, Ph.D.
President and Chief Executive Officer
Micro Data Base Systems Inc.
POB 248
Lafayette, IN 47902

Video Displays and Elimination of Health Risks

The letter in the December 1982 BYTE from John C. Villforth of the U.S. Bureau of Radiological Health attempted to reassure VDT (video display terminal) users that these machines do not emit harmful levels of radiation. In reality, there are very good reasons for suspecting that the current generation of cathode-ray tube VDTs are hazardous and are causing cataracts and other diseases. Fortunately, however, VDTs can be built by several other methods that reduce or eliminate radiation emissions.

In cathode-ray tubes (CRTs), a high-speed beam of electrons is abruptly decelerated as it slams into the face of the tube. It is a basic fact of physics that this process produces x-rays and microwave and ultraviolet radiation. Mr. Villforth writes that the government has done studies showing that CRT x-ray emissions under "normal" conditions are not "significantly above the natural background radiation to which we are all exposed." Just exactly what does this mean? Why

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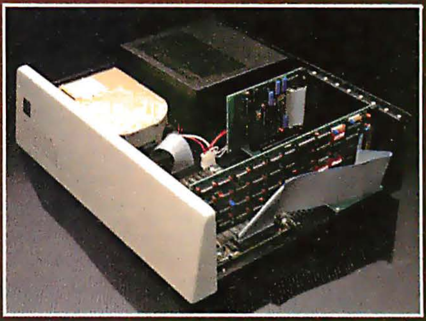
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doesn't he tell us some actual measurements, in millirads per hour at a point 1 foot from the screen, so we can make up our own minds about just how dangerous they are?

Radiation emissions from CRTs may indeed be low, but it does not follow that they are not hazardous. With radiation, there is no threshold—all exposures, no matter how low, carry with them some additional risk of cancer and leukemia, genetic damage, and depressed functioning of the body's immunological system. Radiation to the eye in particular increases the likelihood of cataracts and eye damage. Furthermore, the x-rays, microwaves, and ultraviolet radiation may act together, in synergy, to do many times more damage than each by itself.

It is fundamentally unscientific to assert that measurements of radiation emitted from CRTs show that this radiation is safe. The only real way to tell is to analyze carefully controlled, long-term epidemiological studies of the rates of cataracts and radiation-caused diseases in people using CRTs versus the rates of these diseases in people not using CRTs. These studies should be started immediately (because cataracts and cancer can take many years to become manifest), and they should be carried out by truly independent scientists. The federal cover-ups of the cancers among GIs and residents of Utah and Nevada caused by fallout from atomic-bomb tests show clearly that no federal agency—including the Bureau of Radiological Health—can be trusted to tell us the truth about radiation.

Fortunately, video display terminals can be built in a manner that eliminates radiation exposure. Liquid-crystal or light-emitting-diode displays emit no radiation. Another method is to have the operator look through glass at the image from a CRT reflected from a mirror. IBM already makes such terminals. Even the use of a lead-glass shield over the CRT screen should make a big difference.

Those of us who must use the ordinary computer CRTs can do several things to minimize the radiation risk. First, don't sit too close to the thing. (Radiation levels decrease with the square of the distance from the screen.) Second, turn the brightness (the voltage through which the electron beam is accelerated) down as low as you can without decreasing readability. Careful adjustment of room lighting to eliminate screen glare will enable the brightness to be turned down even lower, as does the highly visible amber screen, which is mandated by law in several European countries. And third, do investigate products such as lead-glass shields, which are claimed to have radiation shielding capabilities.

I'm not arguing for a risk-free society. I only point out that in this case we're taking a risk—one that may turn out to be quite severe—for no corresponding benefit. Radiation-free VDTs can easily be built to emit no radiation. But it's up to us, the computer users, to demand that such machines be built. No market, no product.

For those interested in further information, I strongly recommend the book *Radiation and Human Health* by John W. Gofman, M.D. and Ph.D., and one of the world's foremost authorities on the health dangers caused by ionizing radiation (Sierra Club Books, 1981). Another excellent book, which focuses in particular on microwaves, is *The Zapping of Ameri-*

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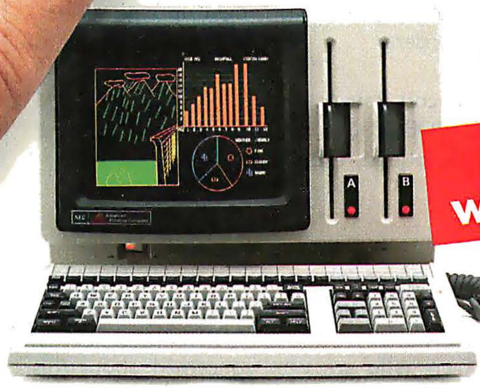
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ca by Paul Brodeur (W. W. Norton and Company, 1977).

Edward M. Gogol
407 South Dearborn, Suite 930
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Open Correspondence on JRT Pascal

At our local users group meeting of December 16, 1982, a show of hands was called on the subject of JRT Systems' $29.95 Pascal offering.

Of the 12 people present who had ordered JRT Pascal, only 3 had actually received the product, yet 11 had already had their checks processed and returned. I myself have been waiting for more than four months. My check was processed over three months ago. I have called the factory twice; once I was put on hold for 15 minutes, the second time I was told that my product had been shipped three weeks prior and that I should wait another week. At the end of an additional two-week wait, I wrote the factory, and three weeks later wrote again. I received my third direct-mail offering for JRT Pascal two weeks ago, and again I wrote the company to ask that they ship my product immediately. Because so many other people share my experience with JRT Systems, I urge you to suspend the firm's advertising privileges until it can show proof that it has caught up with all back orders.

Scott Rainey
POB 6530
Portland, OR 97228

We are having delays in the shipping of JRT Pascal to our customers. I have received a number of letters from customers who are very concerned about this. Similar letters have been sent to the editors of the magazines in which JRT Systems advertises.

It has always been our policy to immediately cancel any order on request or make an immediate refund if payment has been processed and shipment not yet made.

As of today we have shipped 10,000 Pascals and have 7000 orders on backlog. About 6000 of those are less than six weeks old. A six- to eight-week shipping delay is not unprecedented in the computer industry, but it is not acceptable to JRT Systems.

How did this backlog develop, and what am I doing to correct it? In May 1982 I cut the price of JRT Pascal from $295 to $29.95. I tested this formula by mass mailings of 100, then 400, then 1000, brochures. Sales response was excellent—10 to 15 percent—on the early mailings. I was able to rapidly expand the mass mailings and advertising leading to these approximate sales figures: May, 100; June, 350; July, 700; August, 1400; September, 2000; October, 4000; November, 3000; December, 5000.

In August, JRT Systems moved from my home to a small office on Irving Street in San Francisco. By October this office was severely crowded with six people, three phones, and two computers. In mid-December we leased 6000 square feet of space in Mill Valley. The shipping department has now moved into 1600 square feet of the new space. In the past two weeks, the shipping staff has grown from one to four full-time people. In this same period we completed installation of a sophisticated set of new shipping programs that automate, log, and validate every aspect of the shipping operation. Last week we exceeded 500 Pascal shipments per day. With our new system we can exceed 1000 per day.

We still have delays in obtaining copied disks rapidly enough, especially in 5¼-inch formats. Changes planned for the near future will eliminate this problem.

In short, the delay in shipping JRT Pascal is due to our staggering sales growth. We are moving as fast as possible to expand production capacity. [Letter is dated January 2, 1983].

J. R. Tyson, President
JRT Systems
550 Irving St.
San Francisco, CA 94122

As Mr. Tyson points out in his letter, shipping delays are not uncommon in the computer industry, as in all industries. Our readers should be aware of this situation when dealing with any firm. You have the right to demand a full refund if a product you have ordered is not shipped within thirty days of receipt of the order, or you may elect to wait for it to be delivered. The choice is yours. . . . P. C.

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Microprocessor	16-Bit 8088 8-Bit Z-80 (Opt)	16-Bit 8088	?
USER Memory	128K-1 Mbytes	16K-256 Kbytes	?
IBM-PC Compatible Expansions Slots Beyond Professional Configuration[1]	8 Slots	0	?
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Resident Cache Buffer Hard Disk Storage	5M/10M	—	?
OPTIONAL OPERATING SYSTEMS (Supported by Company)[2]			
MS-DOS (PC-DOS)	Yes	Yes	?
CP/M 86	Yes	Yes	?
MP/M 86	Yes	—	?
OASIS-16	Yes	—	?
XENIX	Soon	—	?
OPTIONAL HARDWARE EXPANSION BOARD (Supported by Company)			
RS-232 Communications	Yes	Yes	?
B/W and Color Display Controller	Yes	Yes	?
Expansion Memory	Yes	Yes	?
Z-80 CP/M-80 Board	Yes	—	?
Cache Buffer Hard Disk	Yes	—	?
Time/Calendar Board	Yes	—	?
IEEE Bus Controller	Yes	—	?
8" Floppy Disk System	Yes	—	?
8" Hard Disk System	Up to 40 Mbytes	—	?
Tape Cartridge System	Yes	—	?

[1]For comparison purposes, typical professional configurations consist of 16-Bit 8088 Processor, 128K RAM with Parity, Dual 320K 5-inch Floppies, DMA and Interrupt Controller, Dual RS-232 Serial Ports, Centronics Parallel Port and Dumb Computer Terminal or Equivalent.

[2]Columbia Data Products also supports CP/M 80® with an optionally available Z-80 CP/M Expansion Board.

*As advertised in BYTE Magazine, August 1982.

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Another Atari Character Editor

In his article "Character Editor for the Atari" (December 1982 BYTE, page 167), Tim Kilby says, "While several character editors are available commercially, none are specifically designed for use with ANTIC 4 and ANTIC 5 modes." That's not quite accurate.

I am the author of The Next Step, published by Sierra On-Line. It is an Atari graphics package centered around the idea of redefined character sets and has been on the market for about a year. Among other features, it contains explanations and example programs similar to those found in Mr. Kilby's article. The Next Step contains a powerful, easy-to-use character editor that fully supports ANTIC modes 4 and 5. As a matter of fact, it is the character editor that John Harris used for both the ANTIC mode 4 background and the player-missile graphics in his Atari version of Frogger.

As Tim Kilby says, redefined character sets are one of the most powerful features of the Atari computers. When teamed with custom display lists, as supported by The Next Step, impressive graphics are well within the reach of the BASIC programmer. Thank you for your help in spreading this knowledge.

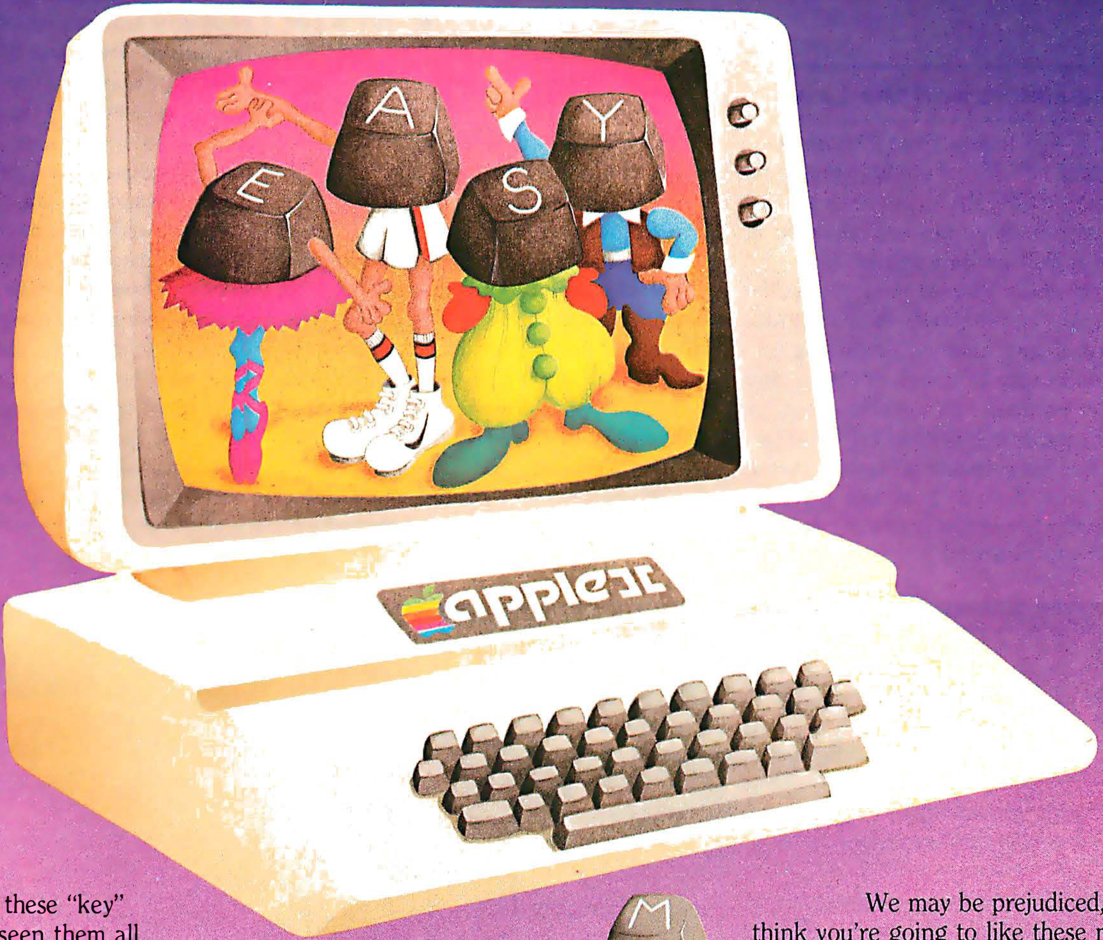
Bob Stewart
The Logic Smiths
Pine Trail
Groton, MA 01450

Problems with FORTRAN-86

The problem with microcomputer FORTRAN compilers is more widespread than indicated by the letters from David Dunthorn and T. M. Putnam criticizing Microsoft's FORTRAN-80 and IBM Personal Computer FORTRAN, respectively (December 1982 BYTE, page 22). Version 1.0 of Intel's FORTRAN-86 (for Intel's 8086-based microprocessor development systems) incorrectly compiles data statements that use repeat factors, generates numerical error codes that are not documented in the Intel *FORTRAN-86 User's Quide*, frequently creates bad object code for operations involving 4-byte integers, and recently refused to compile an 8-line subroutine whose only executable statements were a type-conversion, an integer multiply, and RETURN.

The Enhancer II™ Proudly Presents

A Whole New Cast of "Key" Characters!



Recognize some of these "key" characters? You've seen them all before on your Apple® II screen, but now the Enhancer II has given them all new identities!

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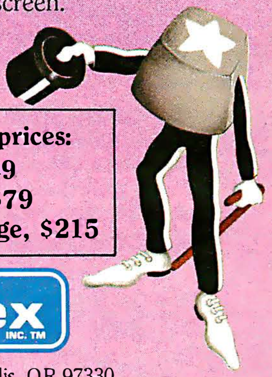


Besides that, the Enhancer II gives your Apple II typewriter mode, with each key assuming the identity of a conventional typewriter key. Not only will you recognize all the characters; you'll positively rejoice at having upper and lowercase letters, auto repeat, shift and shift lock again! The Enhancer II also has a type-ahead buffer of 128 characters, so you can keep sending messages to your Apple II even while it's busy with something else.



And if you want to meet even more new characters, the optional Function Strip™ will introduce you to 16 brand-new keys across the top of your keyboard which are yours alone to define. (These characters will never get mixed up with characters from the keyboard!)

We may be prejudiced, but we think you're going to like these new "key" characters from Enhancer II. In fact, we'll bet that once you've seen them perform, they'll become the stars of your screen.



Suggested retail prices:
Enhancer II, $149
Function Strip, $79
Combined Package, $215

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(503) 758-0521

The Enhancer II and Function Strip can be used with any Apple with a keyboard encoder board.

Apple and the Apple logo are registered trademarks of Apple Computer, Inc.

Circle 429 on inquiry card.

Intel had promised a July 1982 release date of a revised compiler, but as of mid-December 1982, I haven't seen so much as an updated bug list.

Meanwhile, the list price of this remarkable piece of software is a mere $4300.

Jay Reynolds Freeman
POB AJ
Belmont, CA 94002

Disclaimers and the Law

I found the letters from David Dunthorn and T. M. Putnam regarding Microsoft's FORTRAN interesting. Unfortunately, both parties are mistaken in their belief that nothing can be done.

IBM's program license stating that the FORTRAN "is provided 'as is' without warranty of any kind . . . including . . . implied warranty of merchantability and fitness for particular purpose" may not be worth the paper it is printed on. If we can assume that the software is "goods" then it comes under Article 2 of the Uniform Commercial Code (UCC).

Article 2 deals with the law of sales, warranties, disclaimers, remedies, etc. It has been substantially adopted by every American jurisdiction except Louisiana. While the specific question of whether software is "goods" has been not been answered, two different courts have ruled that it is "goods" when sold in a turnkey operation. (See *Triangel Underwriters Inc. v. Honeywell Inc.* (1978 E.D. NY) 457 F. Supp 765, 24 UCCRS 1088, affd in part and revd in part (1979, CA2 NY) 604 F2d 737, 26 UCCRS 1162, later app. *Triangel Underwriters Inc. v. Honeywell Inc.* (1981, CA2 NY) 651 F2d 132 and *W. R. Weaver Co. v. Burroughs Corp.* (1979, Tex Civ App 8th Dist) 580 SW2d 76, 26 UCCRS 64.)

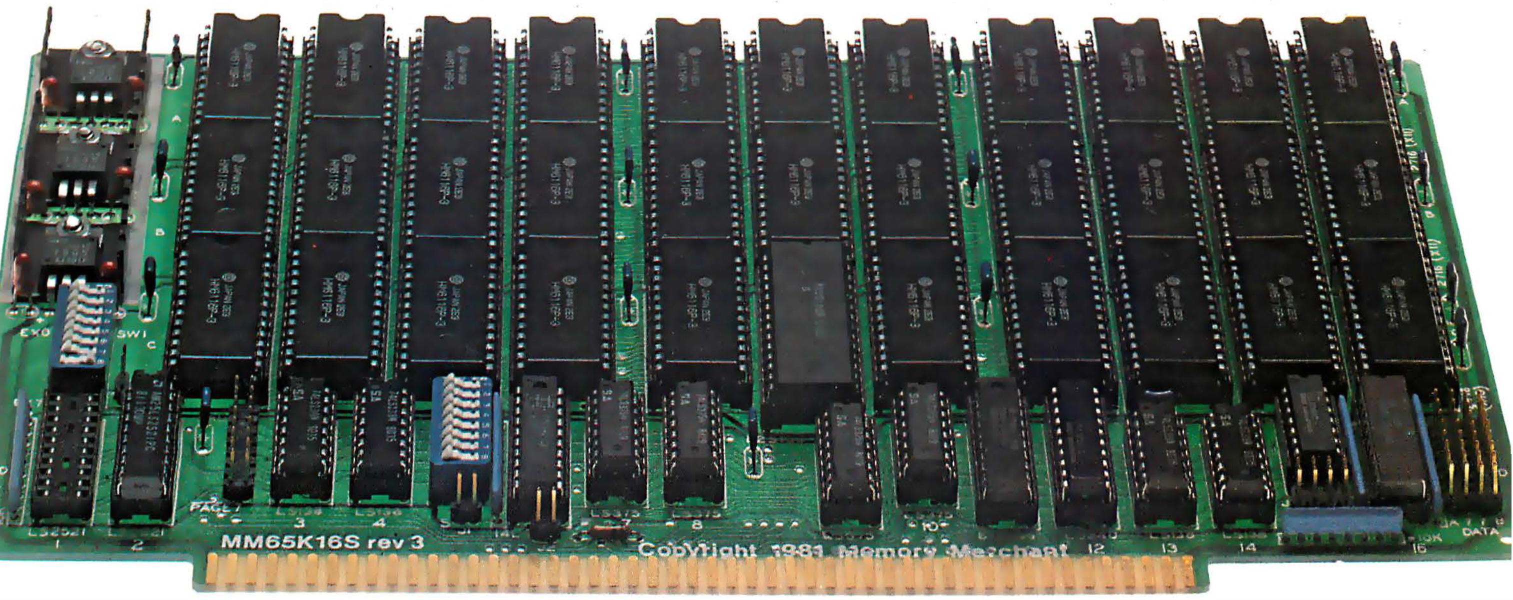
Under the UCC, the implied warranties of merchantability and fitness for a particular purpose cannot be disclaimed after the sale. If the disclaimer first appears in the manual after it is bought, it is not worth the paper it is printed on (see *Zoss v. Royal Chevrolet*, (1972 Ind. Super) 11 UCCRS 527).

Furthermore, the states of Kansas, Maine, Maryland, Massachusetts, Michigan, Minnesota, Mississippi, Vermont, Washington, and West Virginia all limit a seller's or manufacturer's right to disclaim or limit the implied warranties.

Many warranties have limitation-of-damages provisions (e.g., "In no event shall the ACME Computer Company be liable for loss of profits, or benefits, indirect, special, consequential or other similar damages arising out of any breach of this warranty or otherwise.") These limitations are often upheld because the seller or manufacturer will repair the goods. However, in those cases where the seller or manufacturer refuses or cannot make the repair, a judge may rule that the original warranty "has failed in its essential purposes" and the full array of UCC remedies become available to the consumer. These remedies could include all actual, consequential, and incidental damages that the consumer suffered. Recovery could include such things as time spent trying to program around the bug, lost income because the program would not work, and the like.

In addition the UCC requires good faith

64K STATIC RAM MEMORY



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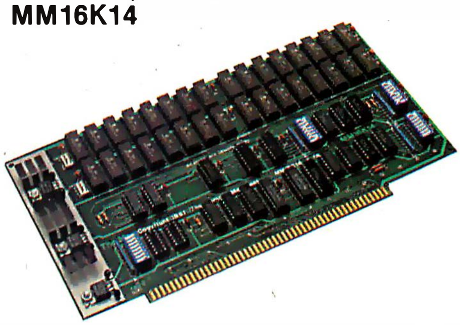
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among the parties. If Microsoft knew of the bug in its FORTRAN-80 package and refused to correct it or failed to put an adequate disclosure of it in its packaging, then punitive damages could also arise on the basis that it fraudulently and knowingly refused to repair a program with a bug (cf. *Hibschmann Pontiac Inc. v. Batchelor*, 266 Ind. 310, 362 NE2d 845 (1977)).

The fact that FORTRAN-80 went through three more releases with the same bug could indicate bad faith on the behalf of Microsoft and this by itself could allow punitive damages (see *Cantrell v. Amarillo Hardware Co.*, 266 Kan. 681, 602 P2d 1326 (1979)).

Finally, I am surprised that Microsoft would admit in a letter that it "has no intention of fixing the bug in FORTRAN-80 regarding FORMAT re-use." Such a letter will be deemed an admission against interest and would greatly ease any punitive damage claim against Microsoft.

As a final point, if Microsoft or IBM advertises its program as in full compliance with the ANSI (American National Standards Institute) Standard FORTRAN X3.9-1966 or any other ascertainable standard, then it has created an express warranty that the product will meet that standard. This express warranty cannot be disclaimed.

L. J. Kutten, Attorney at Law
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St. Louis, MO 63105

Don't Blame Pascal

Jerry Pournelle's User's Column is stimulating, provoking, and sometimes misleading. He is appalled by the difficulties that Alex Pournelle has experienced in developing his introductory Pascal package (December 1982 BYTE, page 222). I sympathize with Alex, but from what Dr. Pournelle has written it appears that his problems have more to do with bad implementations of Pascal than with the language itself. It is unreasonable, for example, to blame Pascal for poor diagnostics, poor error recovery, collapsing compilers, and failure of nonstandard functions.

We all need strings, and it is unfortunate that they are not part of the standard language. Pascal implementors have added string handling in various ways, none of which is completely satisfactory. Pournelle says that no Pascal compiler allows you to concatenate a single character to a string (page 226). This is not so, because Pascal/Z does this and other string operations in a fairly clean and consistent way.

The standard proposed, but not yet ratified, by the International Standards Organization for Pascal specifies two levels of compliance, level 0 and level 1. A level-1 compiler must support *conformant array parameters* (CAP) that permit the size of an array to be passed to a procedure or function. The ratification of the standard has been delayed by the United States representatives, who have refused to accept CAP in Pascal. I do not know of a microcomputer compiler that supports CAP, but some mainframe compilers do.

Pascal uses nested scoping, which may have been a great idea for ALGOL-60 but is somewhat passé today. Strict nested scoping does not support static variables in procedures. PL/I and C provide static variables, but, contrary to widespread belief, FORTRAN does not. (The FORTRAN standard does not mention stacks but is worded in such a way that stack allocation of variables is permitted.) Some versions of ALGOL-60 allow statically allocated *own* variables, but this seems to have been a kludge.

SIMULA-67 introduced *classes*, and many languages developed subsequently, including Ada, have a similar feature. A class is a collection of variables and procedures, some of which are private to the class and some are visible outside it. You can simulate packages in Pascal or C, but neither language supports them properly. As Lori Clarke et al. pointed out at the 1980 Ada Conference, if you have packages, "nesting is for the birds."

Wirth clearly recognized the weakness of Pascal's loop constructions, because his next language, Modula-2, allows loop exits. It is possible to code quite elegant loops in Pascal using loop variables. The method was introduced by L. V. Atkinson; here is a simple example:

```
VAR state : (searching, found, fail);
state := searching;
REPEAT
  IF end-of-list
    THEN state := fail
  ELSE IF item-matches
    THEN state := found
  ELSE get-next-item
UNTIL state <> searching;
CASE state OF
  found : . . .
  fail : . . .
END
```

The three-valued state variable allows us to distinguish normal and abnormal loop termination clearly and explicitly.

I have written this letter reluctantly because I find that debates about programming languages (and operating systems) are usually acrimonious and unhelpful. Most of these debates tend to be over such trivia as where the semicolons go and how many symbols you need to implement your favorite algorithm. We can compare languages meaningfully only if we agree beforehand on the environment in which they will run and the applications for which they will be used.

Peter Grogono
Metonymy Productions
4125 Beaconsfield Ave.
Montreal, Quebec H4A 2H4
Canada

Software Boycott

Software piracy has been a concern to software vendors for some time. To protect their investment, vendors resort to copy protection and limiting the number of backup copies that can be made. Unfortunately, this often precludes the use of hard-disk storage and makes the system fragile. Businesses find it frustrating to have their systems down for a few weeks until the vendor ships a new disk. BYTE and other magazines have presented all sides of the pirating issue in the past.

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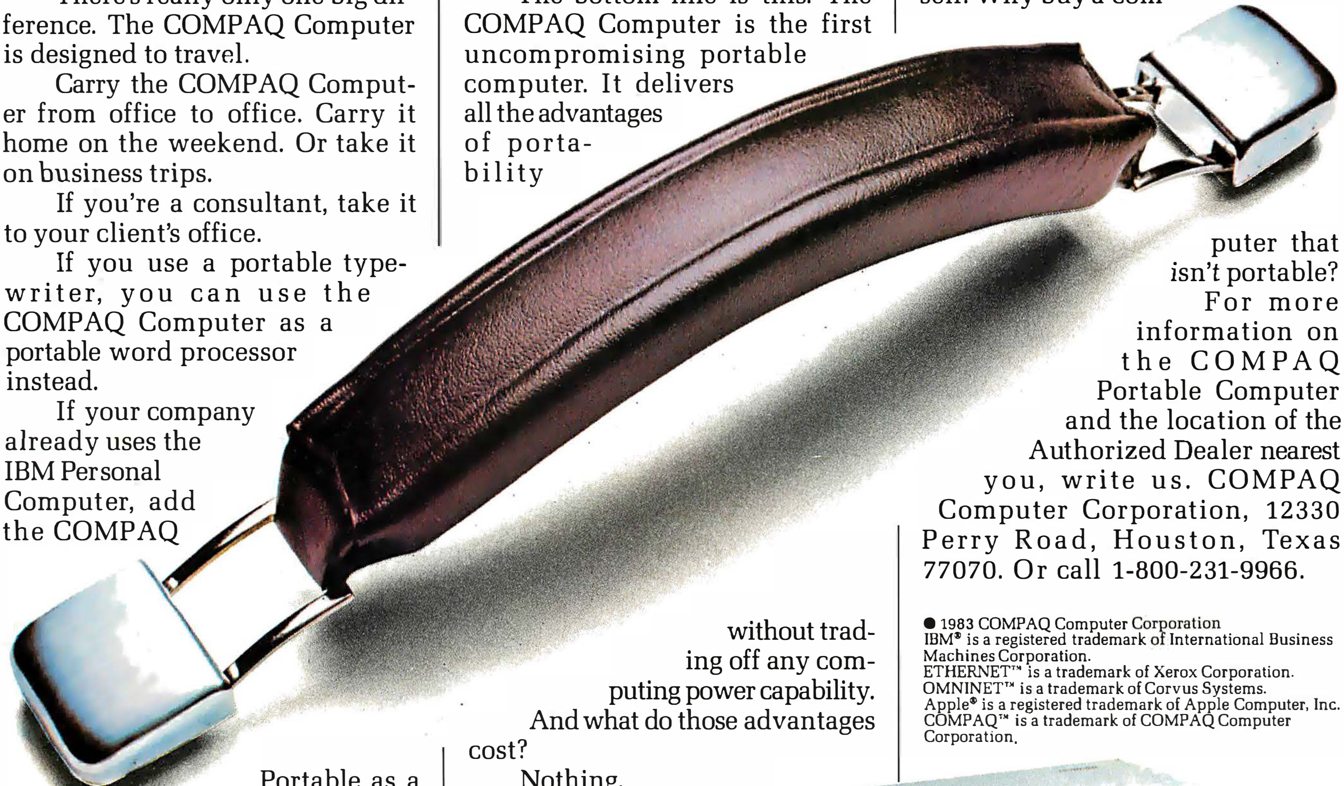
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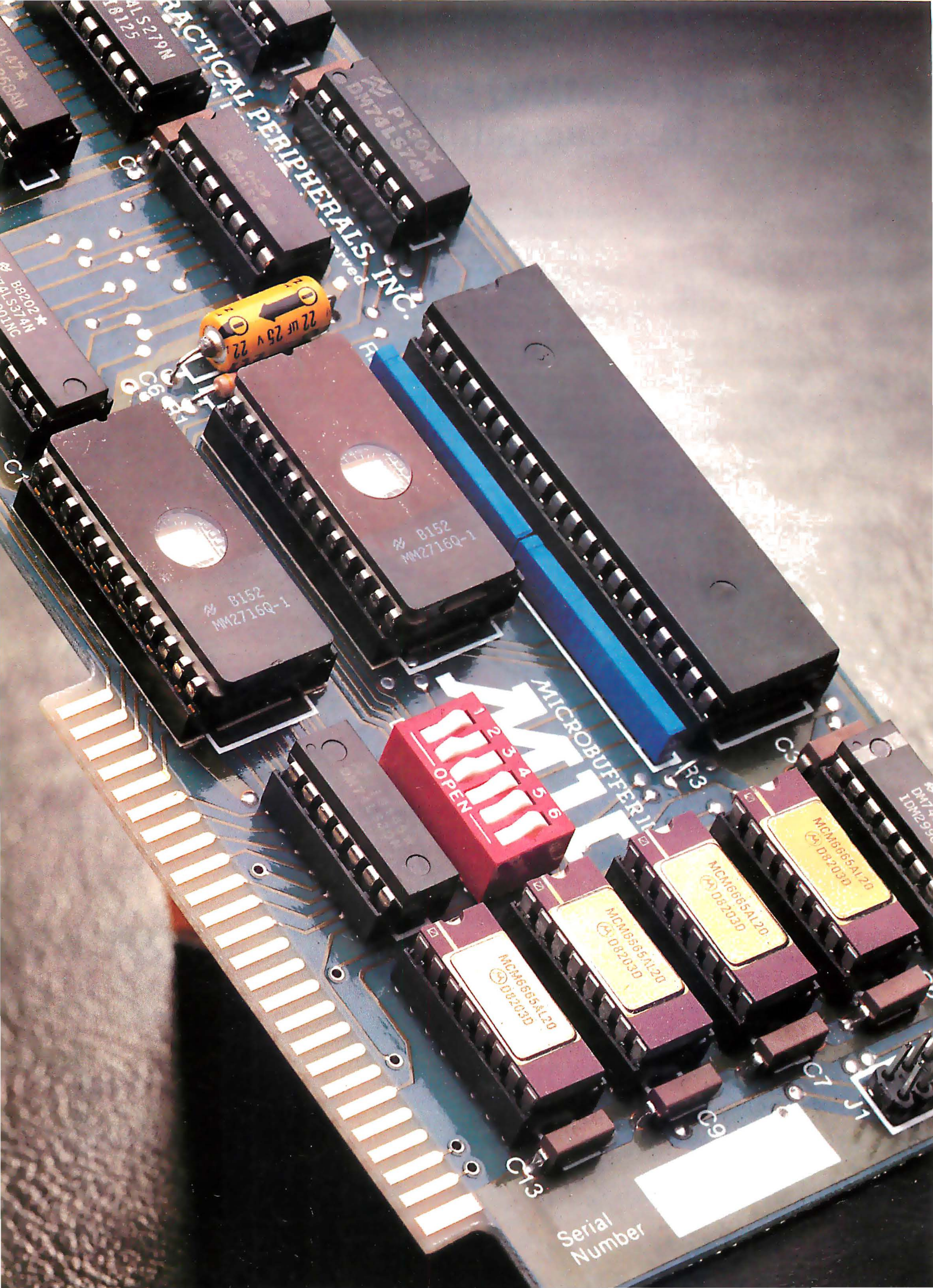


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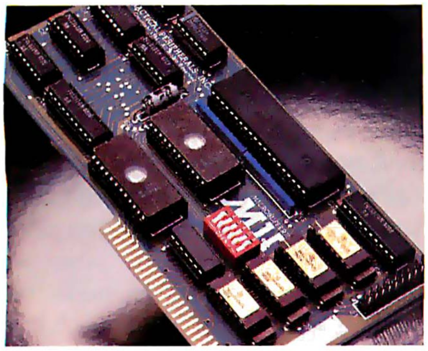
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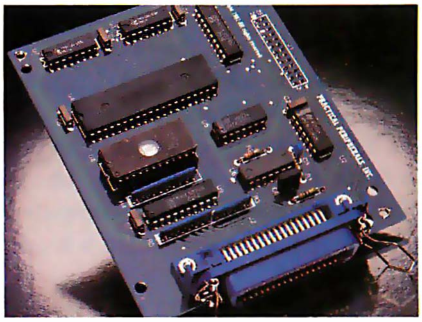
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Build an RS-232C Breakout Box

This diagnostic tool can help you make working serial connections.

Steve Ciarcia
POB 582
Glastonbury, CT 06033

Hundreds of exhibit-goers swirled around me as I elbowed wearily, yet warily, through the computer-convention crowd. Like Frodo Baggins approaching Mount Doom, I had to go to a place I feared to be: the BYTE booth. If I stayed anywhere near it, I was certain to be accosted by someone asking technical questions. (When your picture is plastered all over books sold at half a dozen booths, it's hard to remain incognito.)

Just as I started to take refuge behind the wall of 6000 boxed magazines in the BYTE booth, a voice behind me called out, "Steve, Steve! Help! I was going to send you an 'Ask BYTE' letter, but I need an answer right now on how to interface one of your projects to my computer."

I turned to respond as a man in his early thirties, carrying a briefcase and two shopping bags, hurriedly approached the counter. Panting a bit, he spoke with overtones of nervous anxiety combined with a note of triumph. I shrugged and responded, "Sure, I'll be glad to help if I can."

Most questions of this kind require minimal effort: at worst, digging out a few sheets of scratch paper and scribbling a schematic diagram or two. After all, most computers use similar parallel or serial interfaces.

"I have this computer. . . . " As the man started to speak, he cleared about four feet of counter space with one elbow, leaned over to one of his shopping bags, and started pulling out pieces of equipment and cables. "Here, hold this . . . um . . . somewhere in here are the monitor, recorder, and this other junk . . . and, wait, here it is! I want to connect it to this here Microvox of yours. Can you do it for me? I've made some homebrew modifications to my computer, but that shouldn't keep it from working."

I've been told that, to be perceived as a good teacher, you have to be able to leave everything as an exercise for the student. Here I was, in the middle of a convention with 50,000 people, and this guy had dragged in his whole computer system. Mind you, I've spent hours talking shop with computer hobbyists in public places, and I've designed as much circuitry on the back of napkins as you see in this column each month. This, however, was a new twist.

His computer? It was an off-the-shelf budget model that I'd used before but hadn't tried with the Microvox speech synthesizer. It had a serial output, so I presumed it would work easily. As we shall see, that assumption was a mistake.

On the surface, it seemed a simple task. The unit had a four-wire serial interface that was described as conforming to the RS-232C specification established by the Electronic Industries Association. The connections in the interface were defined for transmit, receive, status, and ground lines. The Microvox can be connected in that way or through various other handshaking protocols. Inside the Microvox are jumper connections to reverse the functioning of the transmit and receive lines so that the Microvox can be set up as either kind of RS-232C device—data terminal equipment (DTE) or data circuit-terminating equipment (DCE). Given that there were only four wires, it should have been duck soup, right?

My first surprise came in finding that my querist's computer used a DIN (Deutsche Industrie-Norm) connector rather than the DB-25 connector typically used for RS-232C links. But by referring to his computer's instruction manual, we were able to attach the Microvox, set up as a DCE device, and hard-wire the computer's status input so it would see a "ready" condition all the time. The computer was set up as a DTE device, receiving data on pin 2 and transmitting on pin 3.

To our disappointment, when we executed the program to make the synthesizer talk, his computer transmitted nothing that could be received by the Microvox. I grumbled, "OK, maybe there's at typo in the Microvox manual." We reversed pins 2 and 3, setting the Microvox as a DTE device, and tried again. No luck. Still bending down over the hobbyist's machine, I looked over the top of my

wire-rimmed glasses and asked as politely as I could, "Are you sure the serial output on this thing works?"

The subsequent discussion revealed that one of the modifications he had installed was a 20-mA (milliampere) current-loop output. But a serial printer attached to it had worked just prior to his bringing the computer to the show.

Because he had serial data coming out, we decided that it must be the Microvox that wasn't communicating. But how to test it at the show? Hmmm. . . .

As I pondered that question, my gaze came to focus 20 feet across the aisle in another exhibit booth, on a computer system demonstrating a printer. As I looked closer, I saw an RS-232C cable connecting the computer and printer. Certain ideas came quickly into my mind. Gathering up the Microvox, my inquirer and I squeezed across the aisle and approached the booth's proprietor.

Fast footwork and a smooth tongue are necessities in such circumstances. You have to put off saying the phrases "have a problem," "test," and "your computer" as long as possible. So, as I slipped the Microvox onto his serial printer cable, I distracted the exhibitor's attention by saying something like, "Hi, we have a booth over there, and we saw that you were demonstrating this neat printer, and we were wondering if we could try something on your system. . . . Can I put this here? . . . Do you mind if I just plug this in your computer . . . to test just one little thing?"

I had the cable connected before the potential horror of what I was proposing had time to sink in. In fact, the exhibitor was a bit amused as the Microvox started speaking the text that was intended for the printer.

A half hour later, after explaining the theory of text-to-speech algorithms to the curious exhibitor, we went back to the BYTE booth and the original problem. Finding that the Microvox worked, and while not directly suggesting that my shopping-bag computer hobbyist's RS-232C output did not, I searched for a new strategy to make him happy.

Clearly, the problem was not simply one of making the right connections. I needed some way to take a better reading of what was happening. Even a mere bent paper clip and a light-emitting diode (LED) would have helped.

Again we went on the prowl for equipment. Three aisles away I found an exhibitor selling certain RS-232C diagnostic tools called breakout boxes who felt that he could trust me enough to lend me one of his less expensive models for a while. We took it back to the BYTE booth and set to work. We attached the breakout box to the serial output connector and watched for activity on the LED indicators. The transmit LED flickered as the data went to the Microvox, but I was still suspicious.

Back into the throng. Another aisle over I borrowed a DVM (digital voltmeter) and used it to check the voltage levels on the RS-232C output. Serial data appeared to be present, but it ranged from −0.7 to +6.8 V (volts) rather than from +12 to −12 V, as you typically find. The cheap ($150) breakout box was responding to the +6.8-V level, but it had no way of indicating negative voltage levels or open circuits.

Armed with this information, I checked some of the modifications that my comrade in debugging had made. Apparently the 20-mA current-loop circuit was at fault. It was optically isolated, as it should have been, but the optoisolators and other components were being powered directly from the RS-232C signals. The LEDs and protective shunting diodes were shorting out half the data! I disconnected the current loop, and two hours after the computer was first slipped out of its shopping bag, the Microvox spoke.

"Standard" RS-232C

Among the most exasperating experiences in any computer user's career is connecting two serial devices. I don't mean a terminal and a modem—making that connection is a piece of cake—but any other connection can be real trouble.

For instance, every time I buy a new piece of equipment, things seem to work this way: I spend five minutes reading the sales brochure, five minutes executing the financial transaction, and five hours trying to figure out how to make the new equipment communicate with my computer.

If you scan through product advertisements and equipment data sheets, frequently you see claims that products have "standard RS-232 interfaces." The people who perpetrate these lies have probably never connected two pieces of equipment together in their lives. What this phrase really means is that both ends of the communication line will probably be voltage-compatible and won't incinerate each other. Both will send and receive asynchronous or synchronous serial data following a specific timed sequence (bit rate) known by both ends. Beyond that, virtually nothing is reliably standard.

The only sure way to connect two serial devices is to examine the documentation for each and determine the proper connections of inputs and outputs, with lines crossing if need be. If the manuals are not available, then voltage-sensing and status-display devices must be used to examine individual lines. Depending on DTE or DCE convention, the same pin number may be either an input or output. And, generally speaking, in a fully implemented handshaking configuration, single-point signal monitoring is not enough. Frequently, multiple lines must be monitored to observe dynamic relationships.

One of the most useful pieces of test equipment is the RS-232C breakout box.

I don't intend to spend too much time discussing RS-232C handshaking or interfacing. That subject has been covered in numerous other articles in BYTE, most recently by Dr. Ian Witten (reference 7). In my experience, simply knowing the conventions hasn't helped one bit. I always have to study the manuals for each interface and often have to verify voltage levels with a meter. When all the handshaking signals are used, it can be a prolonged task.

Ultimately, successful serial interconnection depends more on your ability to measure, cross-connect, and jumper-connect signal lines until *some* combination works. And sometimes you have to deal with a case wherein the lines might be connected properly but, as in the example above, operating at the wrong voltage levels.

The point of this month's article is to describe some of the hardware involved in testing the RS-232C connection. We'll look at various circuits that make voltage measurements, including two kinds of breakout boxes. Finally, to allow dynamic testing of the data communication on the transmit and receive lines, we will see how to build a terminal simulator, which

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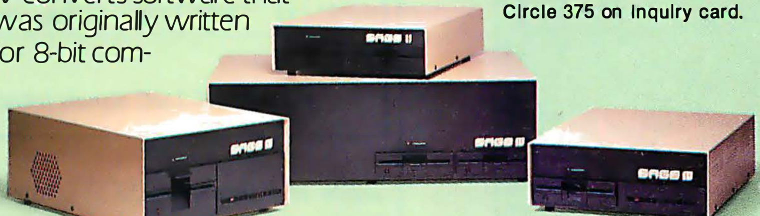
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Pin	EIA	CCITT	Signal	Source
1	AA	101	Protective (Earth) Ground	
7	AB	102	Signal Ground	
2	BA	103	Transmitted Data (TD)	DTE
4	CA	105	Request to Send (RTS)	
20	CD	108.2	Data Terminal Ready (DTR)	
23	CH	111	Data Signal Rate Selector (DTE source)	
24	DA	113	Transmitter Signal Element Timing (DTE source)	
14	SBA	118	Secondary Transmitted Data	
19	SCA	120	Secondary Request to Send	
3	BB	104	Received Data (RD)	DCE
5	CB	106	Clear to Send (CTS)	
6	CC	107	Data Set Ready (DSR)	
22	CE	125	Ring Indicator (RI)	
8	CF	109	Received Line Signal Detector (or Carrier Detect—CD)	
21	CG	110	Signal Quality Detector	
23	CI	112	Data Signal Rate Selector (DCE source)	
15	DB	114	Transmission Signal Element Timing (DCE source)	
17	DD	115	Receiver Signal Element Timing (DCE source)	
16	SBB	119	Secondary Received Data	
13	SCB	121	Secondary Clear to Send	
12	SCF	122	Secondary Received Line Signal Detector	

Table 1: *RS-232C signals listed by function and source.*

sends and receives ASCII (American National Standard Code for Information Interchange) characters at any standard data rate.

The RS-232C Breakout Box

One of the most useful pieces of test equipment is the RS-232C breakout box. This device is essentially a 25-line extension cable with apparatus attached that allows you to perform experiments on the serial link by inserting cross-connections, jumpers, and open circuits between the various signal lines. The most common use of the breakout box is to switch the Transmitted Data and Received Data lines (pins 2 and 3 in the commonly used connectors, abbreviated TD and RD). Another typical use is to make various combinations of connections between Request to Send (RTS, pin 4), Clear to Send (CTS, pin 5), Data Set Ready (DSR, pin 6), Carrier Detect (CD, pin 8—its official name is Received Line Signal Detector), and Data Terminal Ready (DTR, pin 20). The more expensive units can also monitor voltage levels or decode serial data. Table 1 identifies the RS-232C signals by source.

A variety of commercial breakout boxes, ranging in price from $100 to $1000, are on the market. The more expensive products include such additional features as bilevel or trilevel signal monitoring, absolute voltage sensing, and signal-injection capabilities. Some of these features may or may not be important in your application.

When you are choosing a breakout box, be sure you get your money's worth. In some of the $100 units, it appears that $99 of the cost is for the case. The mechanical features are similar at all price levels, and only the addition of electronic bells and whistles adds to the cost.

In any breakout box, you find two 25-pin type-D subminiature (DB-25) connectors, two sets of 25 connection



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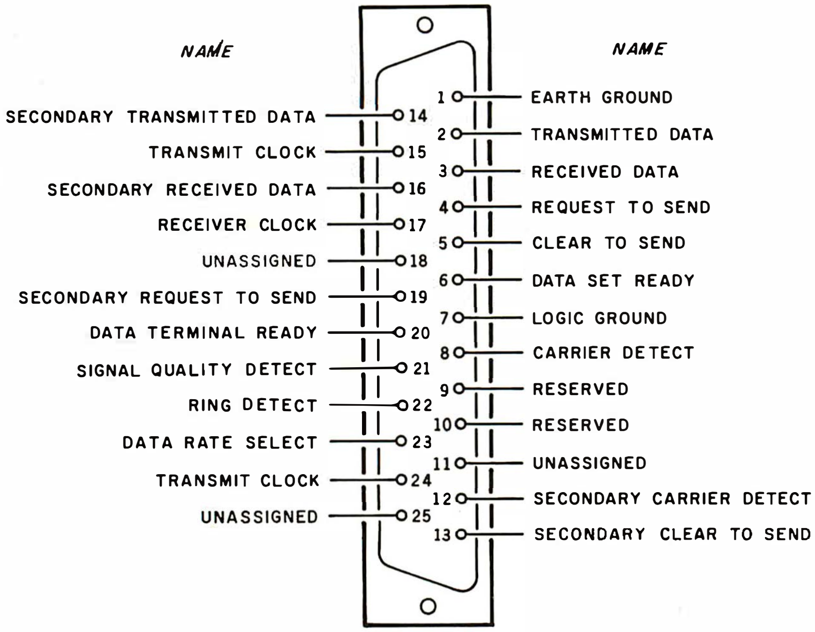


Figure 1: *Pinout specifications of the RS-232C interface. The popular DB-25 connector is most often used for RS-232C connections, but it is not required by the EIA standard.*

posts, and 24 or 25 switches. To begin testing, you connect the breakout box in series between the two pieces of equipment. The 25 lines on the first side go to 25 connection posts (often wire-wrap pins are used), and then 24 of the lines go into one side of three 8-pole DIP (dual-inline pin) switches. (Pin 1, the protective ground line, is directly routed to the output connector.) The 24 lines are directed through the DIP switches to another set of connection posts and then to the output connector. Figure 1 shows the pinout specification of the connectors.

To test the connection between two DTE-type RS-232C devices when no handshaking is involved, you merely insert the breakout box in the link; then, with all the switches closed except the two connected to pins 2 and 3, insert crossed jumpers between the connection posts to interchange the two signals. After you've made sure this works, you can permanently wire a cable to do the same job.

While most commercial breakout boxes connect and switch 24 of the 25 lines, most common RS-232C applications involving printers, low- and medium-speed modems, and video-display terminals generally use only connector pins 1 through 8, plus pin 20. For these applications, we can construct a bare-bones breakout box, such as the one shown in the schematic diagram of figure 2 on page 38.

This simple construction will give you all the necessary features of a $150 box for about $15. Besides a signal-switching capability, this circuit incorporates passive voltage monitoring. Three components—a blocking diode, a constant-current diode, and an LED—indicate the presence of a potential of +4 V or greater on any signal line. The LED does not light for open circuits or negative voltages. Many low-priced RS-232C monitors use this type of circuit, and some cautions regarding its use are appropriate. Such an indicator draws its power from the signal itself (requiring about 4 mA), and in marginal situations it might kill the signal being measured.

For the RS-232C status signals, a line potential anywhere between +3 V and +15 V is logic 1, and a potential from −3 V to −15 V is a logic 0. If these signals are generated from low-power operational amplifiers (op amps) rather than RS-232C drivers, there may not be enough oomph to communicate and light LEDs simultaneously. (Op amps are frequently used as a cost-cutting measure in budget equipment.) Finally, this cheap monitor senses only positive voltages (unless the circuit is reversed in polarity and duplicated everywhere) and gives no indication of negative voltages or ground potential. For example, you couldn't tell the difference between a broken cable lead and a logic-0 (inactive) status signal. Remember that RS-232C is a bipolar signal. As much happens (or doesn't) at negative potentials as at positive.

A Functional, Low-Cost Breakout Box

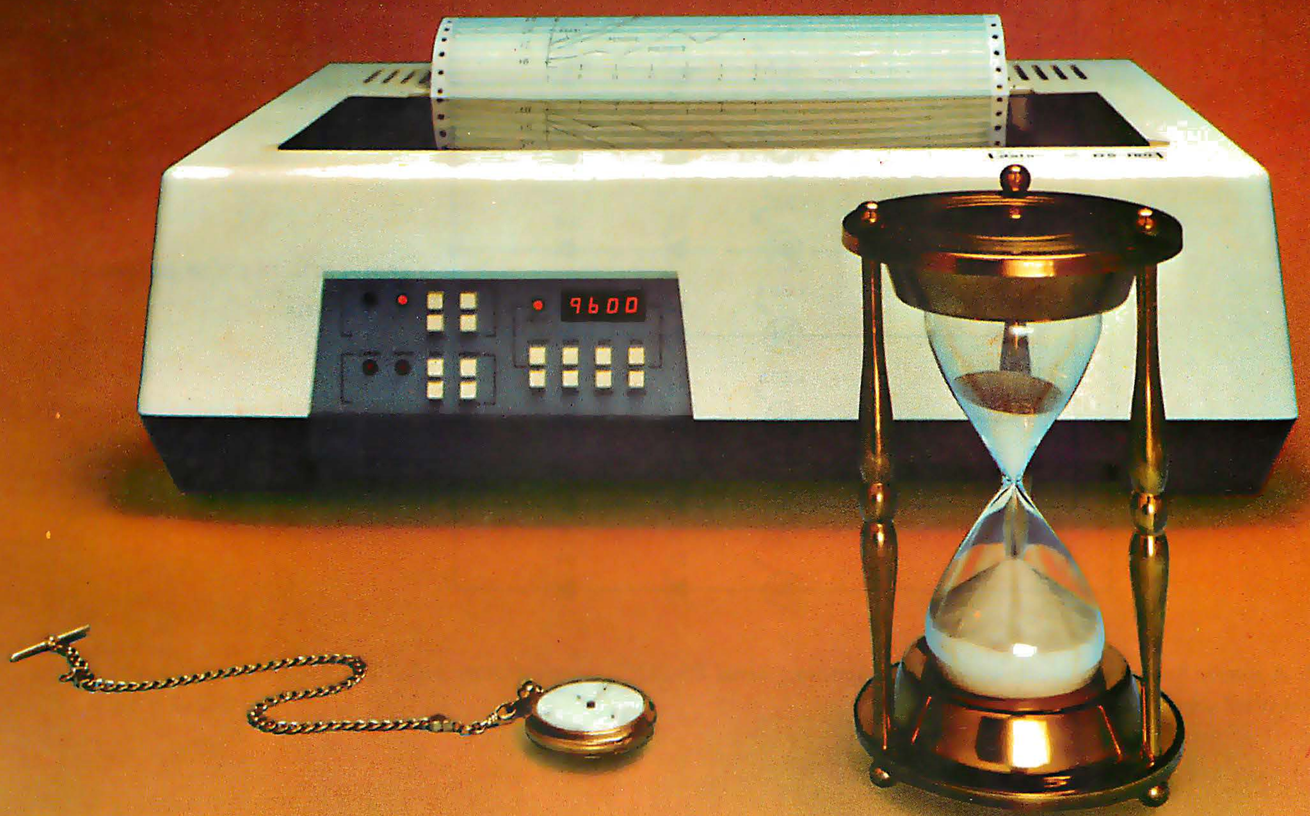
The previous point may have seemed minor, but it leads us to a discussion of better voltage sensors and use of active, rather than passive, monitoring techniques.

Figure 3 on page 38 is the schematic diagram of a much better indicator circuit for sensing RS-232C voltage levels. Using its own op amp to reduce signal loading, this bilevel monitor lights up in red for positive voltages and green for negative voltages. The feedback and gain-setting resistors are chosen so that the LEDs trigger at approximately +3 V and −3 V, respectively (internal current-limiting provides a relatively constant light level and protects the LEDs). Voltages between those values or open circuits light neither LED.

The indicator-circuit sections, one for every signal line, each use one section of an LM324 quad op amp. They present a virtually unnoticeable 100-kilohm load to the signal lines, can operate on any voltage with an absolute value between 4.5 V and 18 V, and can be powered easily from a battery of 6 AA cells for portability. I chose to use integrated two-color LEDs, but two regular LEDs (one red and one green) can be wired anode-to-cathode in parallel.

My idea of a reasonably useful breakout box is shown in figure 4. It combines the 24-switch-and-header portion of the commercial breakout boxes with the sensitive bilevel monitoring circuits just described.

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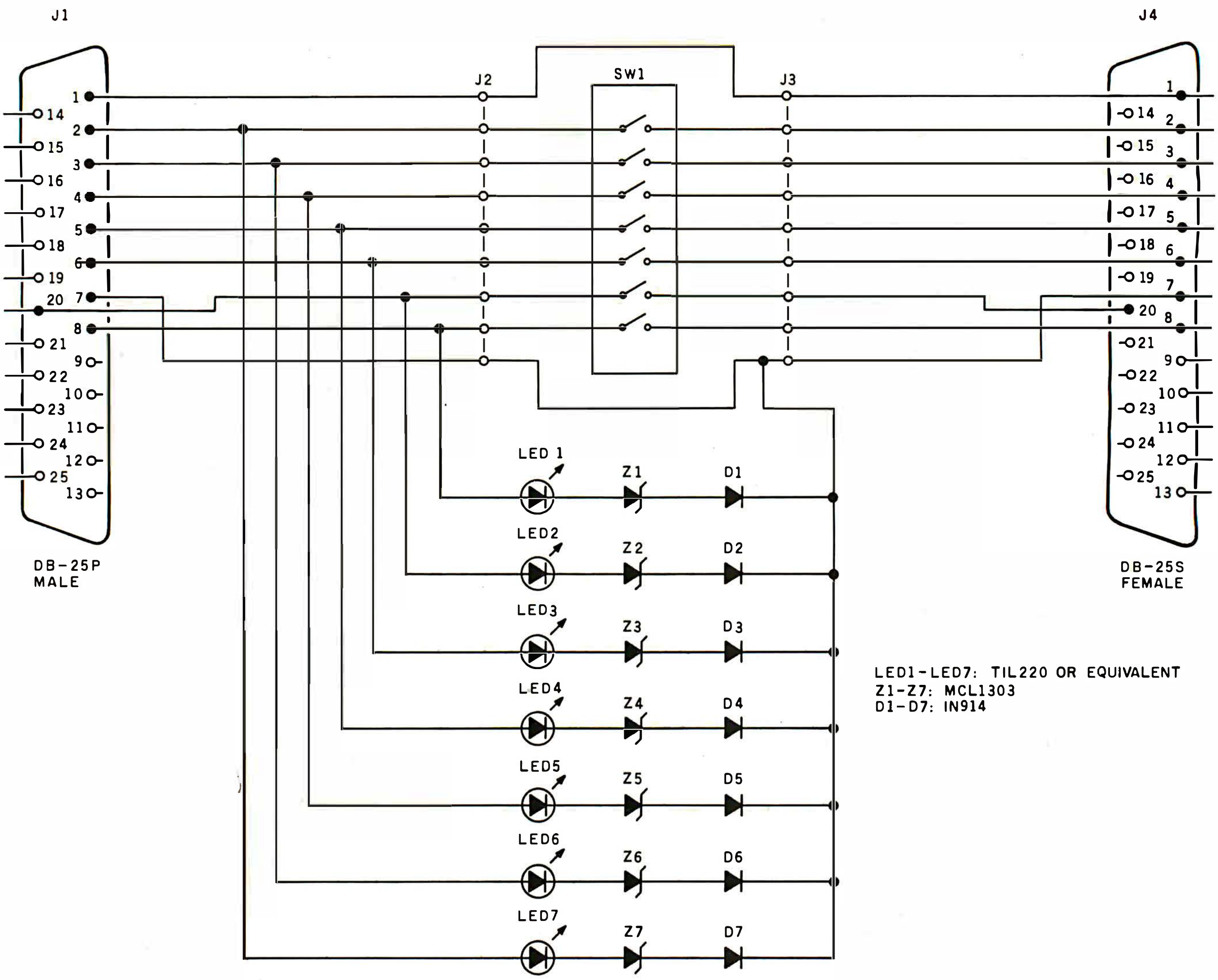


Figure 2: *A simple homebrew breakout box for diagnosing serial RS-232C communication links. The 9 lines connected here are the ones most often used.*

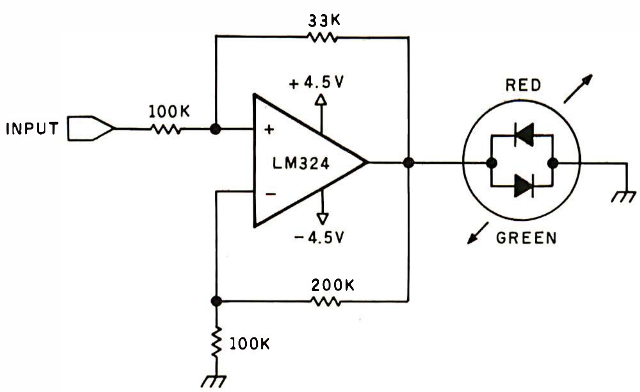


Figure 3: *A line-state status indicator that incorporates an op amp to keep line loading to a minimum. The dual-LED component will glow red for positive voltages and green for negative.*

Voltage indicators are hard-wired on the 11 most frequently used signal lines (2, 3, 4, 5, 6, 8, 15, 17, 20, 21, and 22), and the twelfth sensor can be connected to any line. A prototype of this circuit is shown in photo 1.

A Decade Voltage-Level Indicator

If you think back to my experience at the convention, you'll see that the problem was eventually detected as being voltage-related. It was undetectable with the cheap LED circuit, but it would have been caught by the circuit of figure 4. However, on some occasions even two levels are inadequate, and more precise measurements are necessary.

One extra indicator section was

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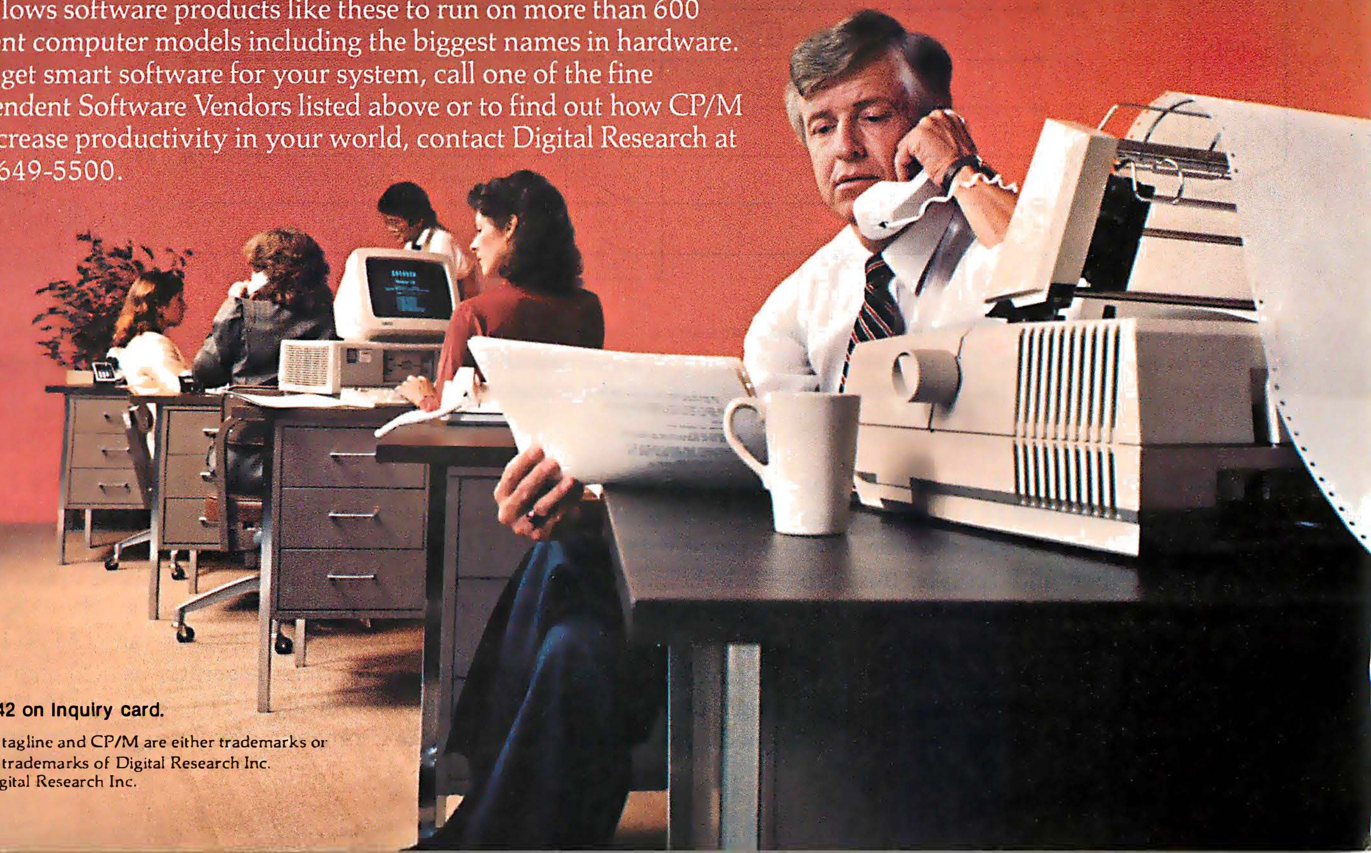
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(4a)

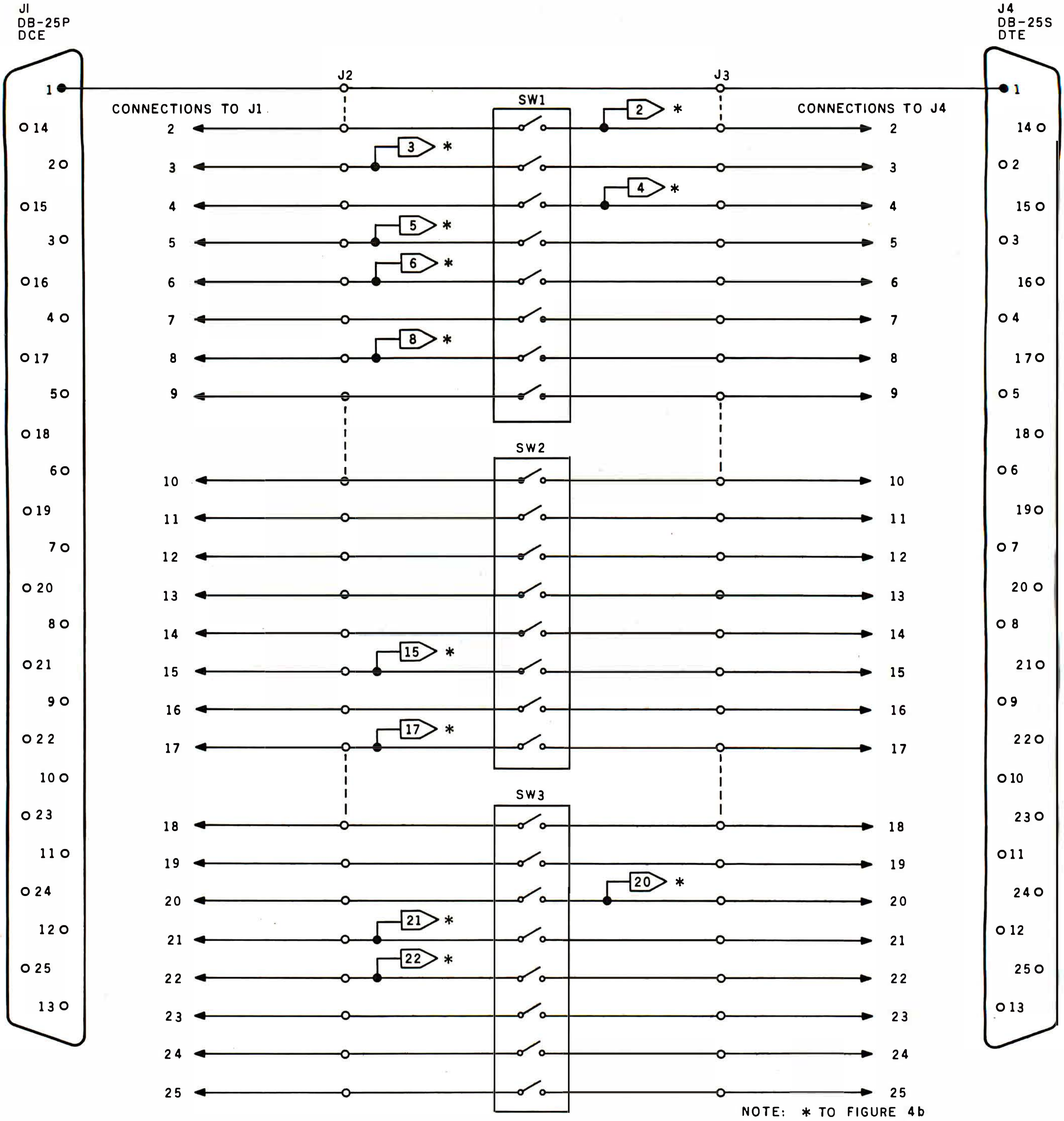
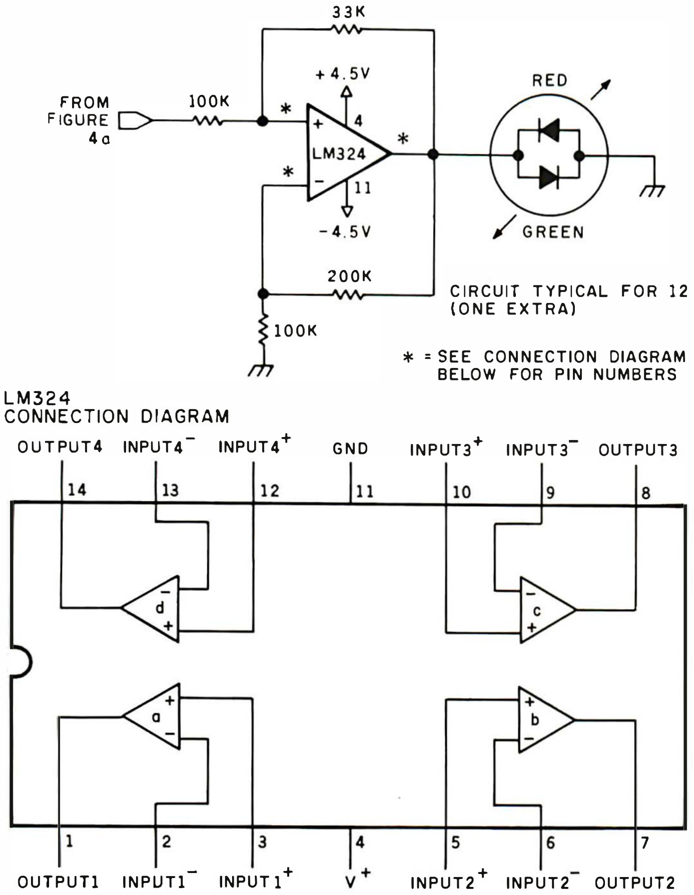


Figure 4: *Schematic diagram (4a) of a breakout box that allows constant monitoring of the 11 most used lines, plus another line selectable by a jumper connection. The indicator circuit of figure 4b is reproduced 12 times; three LM324 packages, each containing 4 op-amp sections, are needed. The connections for each section are also shown in figure 4b.*

provided in the circuit of figure 4 so that it could be attached to any of the 25 input pins. If we expand this concept a bit further and replace this bipolar sensor with something having a little more resolution, we could take a better reading of voltage excursion. Granted, a DVM could be used, but such instruments are expensive and are much more elaborate than required. Because of the RS-232C voltage range of −15 V to +15 V (−3 V to +3 V being no-man's-land), the resolution need be only about 3 volts at best.

The circuit in figure 5 on page 44 is a single-digit decade voltmeter. Designed for installation in the breakout box in place of the floating sensor, it has a higher resolution than the bilevel monitor, and it can be used in place of a DVM in less critical applications such as RS-232C level sensing. It uses an LM3914 LED dot/bar generator as a 10-step analog indicator. The 30-V (±15-V) input range is divided into 10 incremental

(4b)



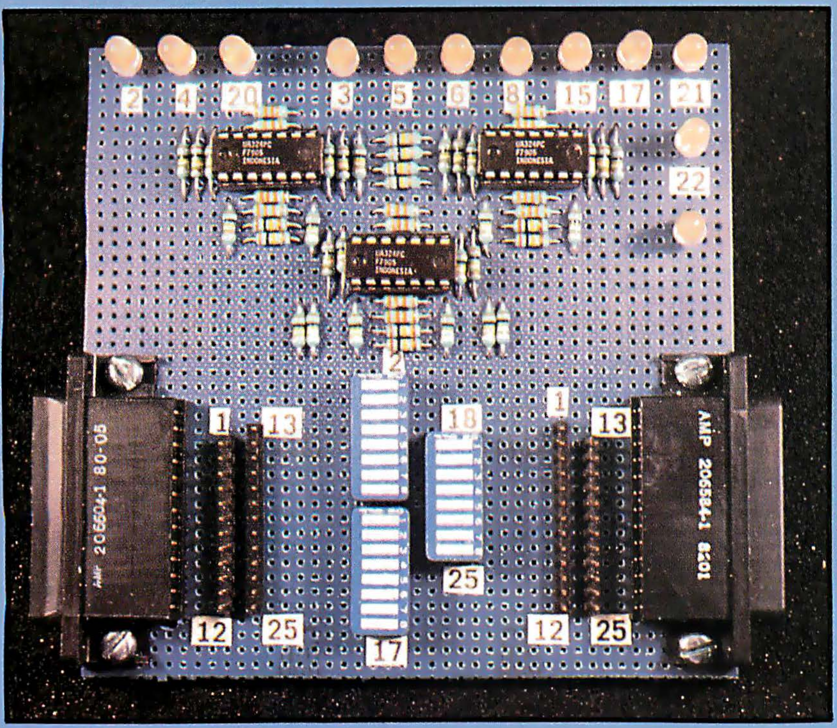


Photo 1: *Breadboard prototype of the simple breakout box of figure 4.*

steps of 3 V. Different-color LEDs provide a quick visual indication of relative magnitude and polarity of the line states. A prototype of the circuit is shown in photo 2.

The decade-voltmeter circuit uses 2 or 3 integrated circuits. IC1a (an LM324 op amp section) scales the input voltage range from ±15 V to ±2.5 V (adjust potentiometer R1 to set the gain for 1/6). Another section, IC1b, shifts the resulting ±2.5 V scaled signal to a 0-V to +5-V range at its output (adjust R2 for the proper shift magnitude). IC2, the LM3914 dot/bar generator, is configured to respond to a range of 0 V to +5 V.

When −15 V is applied to the circuit's input, LED1 lights; when +15 V is applied, LED10 lights. For an intermediate active voltage, such as +9 V, LED8 will light up. In the range of from −3 V to +3 V, which includes ground or open states, LED5 or LED6 will be lit. Using the same color convention as in figure 4, voltages greater than +3 V are shown on red LEDs, those less than −3 V are on green LEDs; in the inactive area between +3 V and −3 V, I used yellow. Any single input signal that swings between a red and green indicator is therefore at valid levels.

The decade-voltmeter circuit requires power at about +7.5 V (or greater) and −5 V (or less) for operation. Two 9-V battery cells (to provide ±9 V) work very nicely. Or using a single +7.5-V source and the ICL7660 voltage inverter (IC3) allows the unit to be battery-operated (for some reason, the 7660 didn't seem to like inverting +9 V when I tried it).

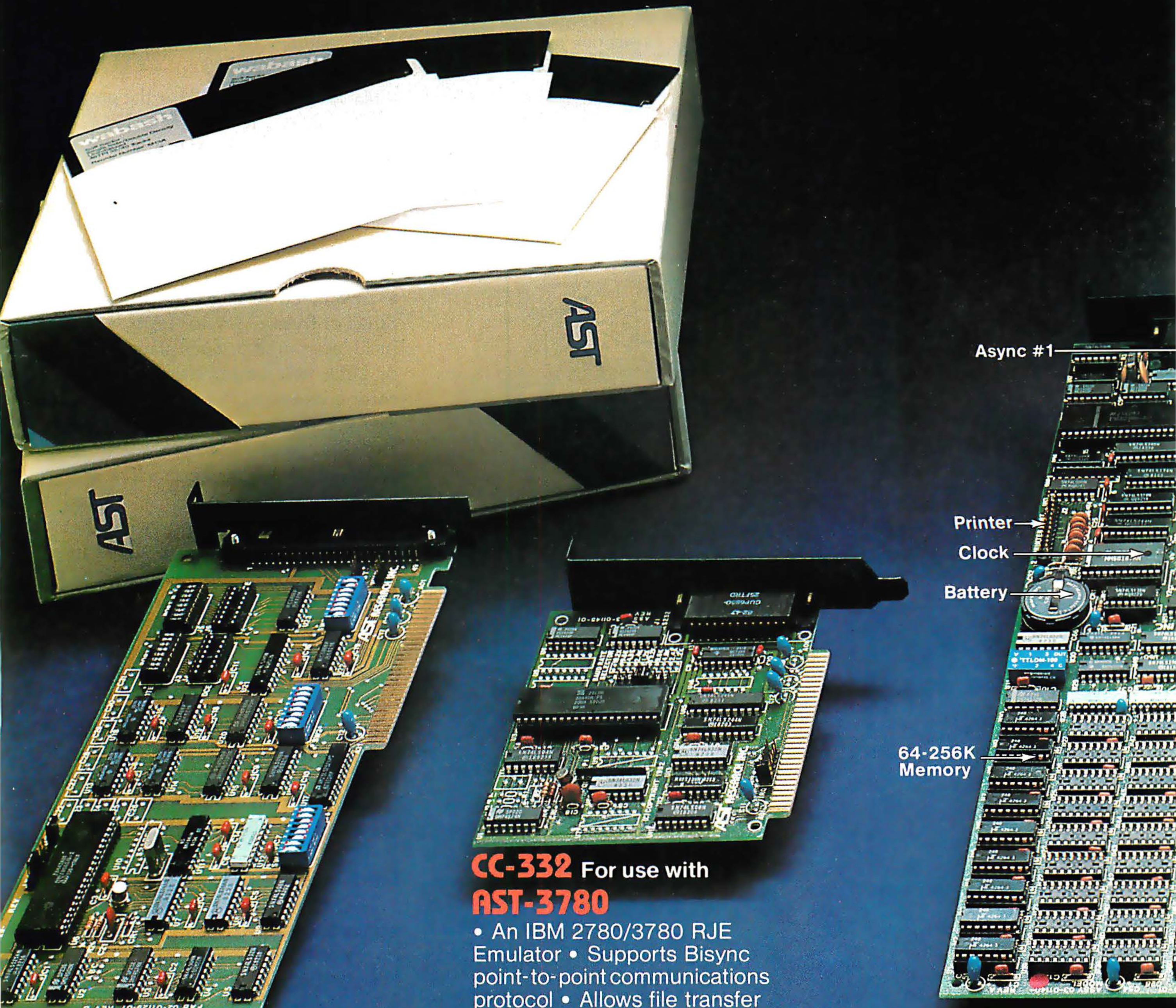
Build a Terminal Simulator

The final thing to check when testing an RS-232C serial link is the existence of properly formatted data bits coming over the wire at the correct data rate. Voltage-level indicators make only quantitative measurements. It is necessary to take a *qualitative* measurement if the integrity of the transmission is in question. Most often the quality of the link can be ascertained with the transmission and reception of a single character.

One way of testing a suspect communication line is to drag around a

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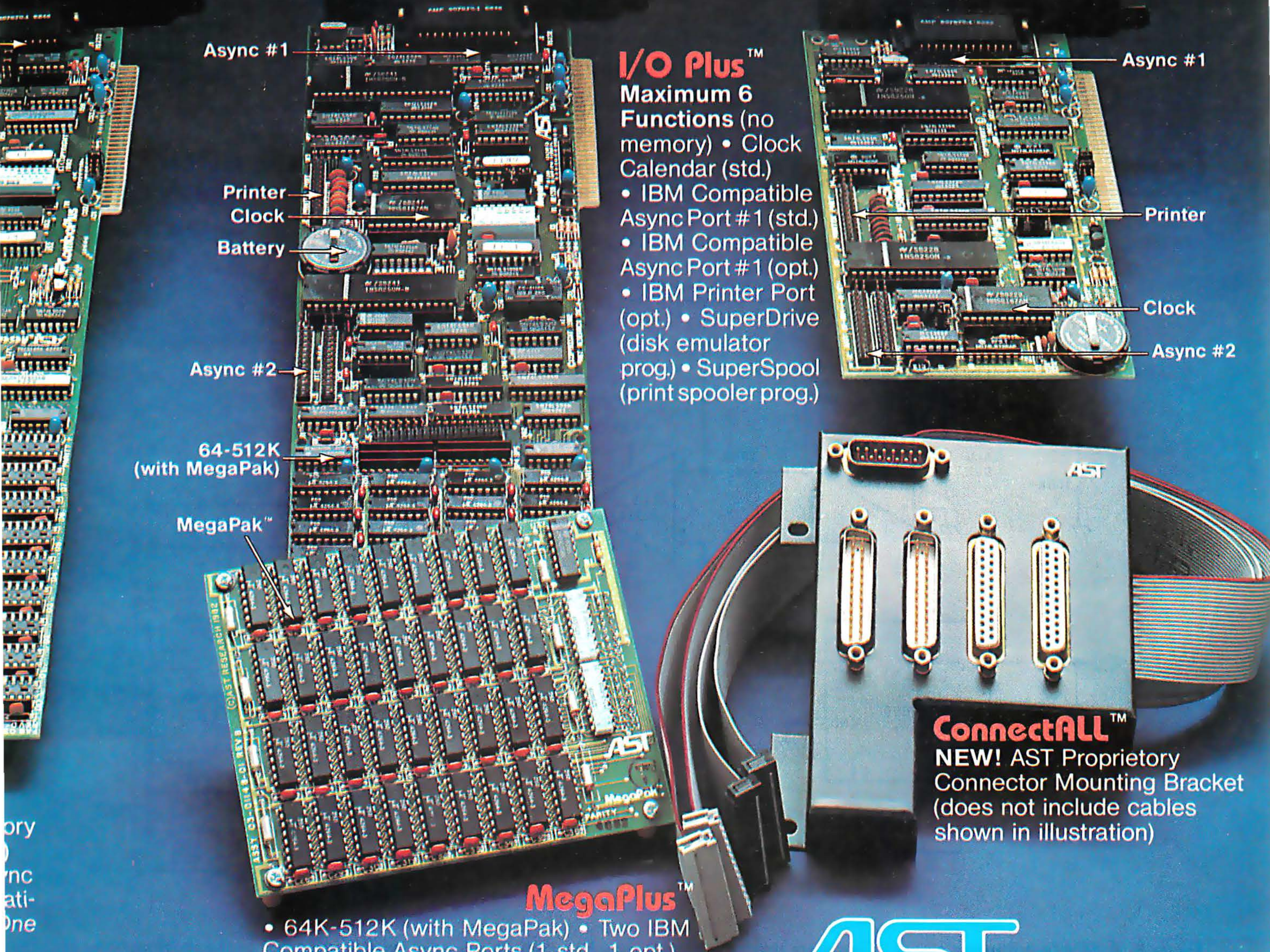
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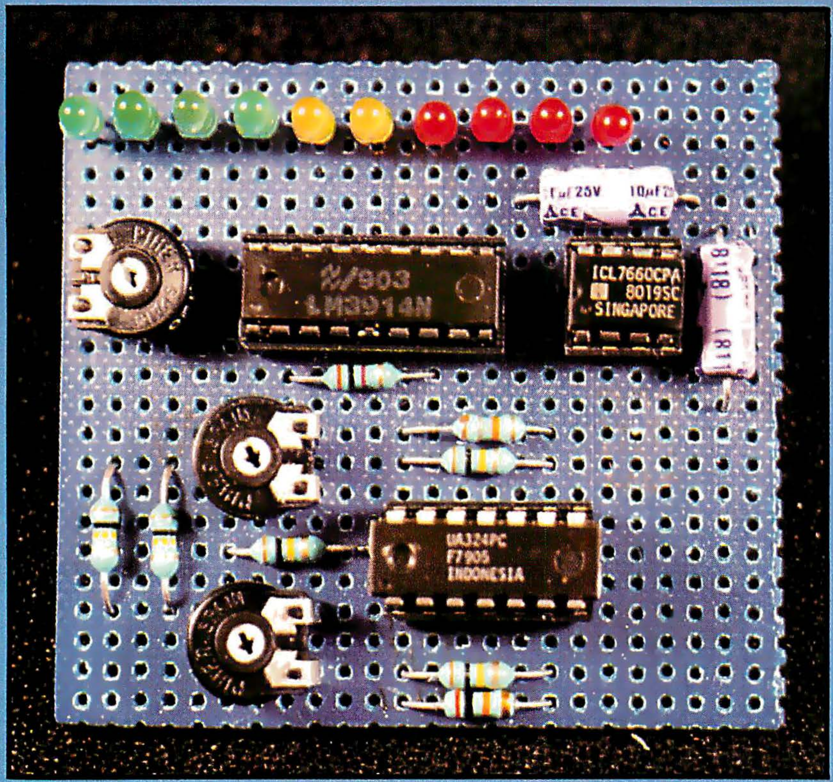


Photo 2: *Prototype of the decade-voltmeter indicator used for precise diagnosis of the state of an RS-232C line.*

big video-display terminal. Also the idea of adapting the single-chip terminal from the February article did occur to me. However, that was a relatively expensive item for a tester, and it couldn't cover all the data rates in common use, so I did some head-scratching and invented yet another circuit.

Figure 6 is the schematic diagram of my single-character terminal simulator. The prototype is shown in photo 3 on page 48. Using 5 chips, it can send, receive, and display (in hexadecimal form) single ASCII characters at any of the 16 commonly used data rates between 50 and 9600 bps (bits per second). By switching pins 2 and 3, you can set it to appear on the line as either a DTE or DCE device. Have you got a suspect device on the line? Set your data rate and desired character code on the DIP switches and then press a button each time you want the character transmitted. Granted, a video-display terminal might be faster, but my simulator circuit is a lot lighter.

The terminal simulator uses a UART (universal asynchronous re-

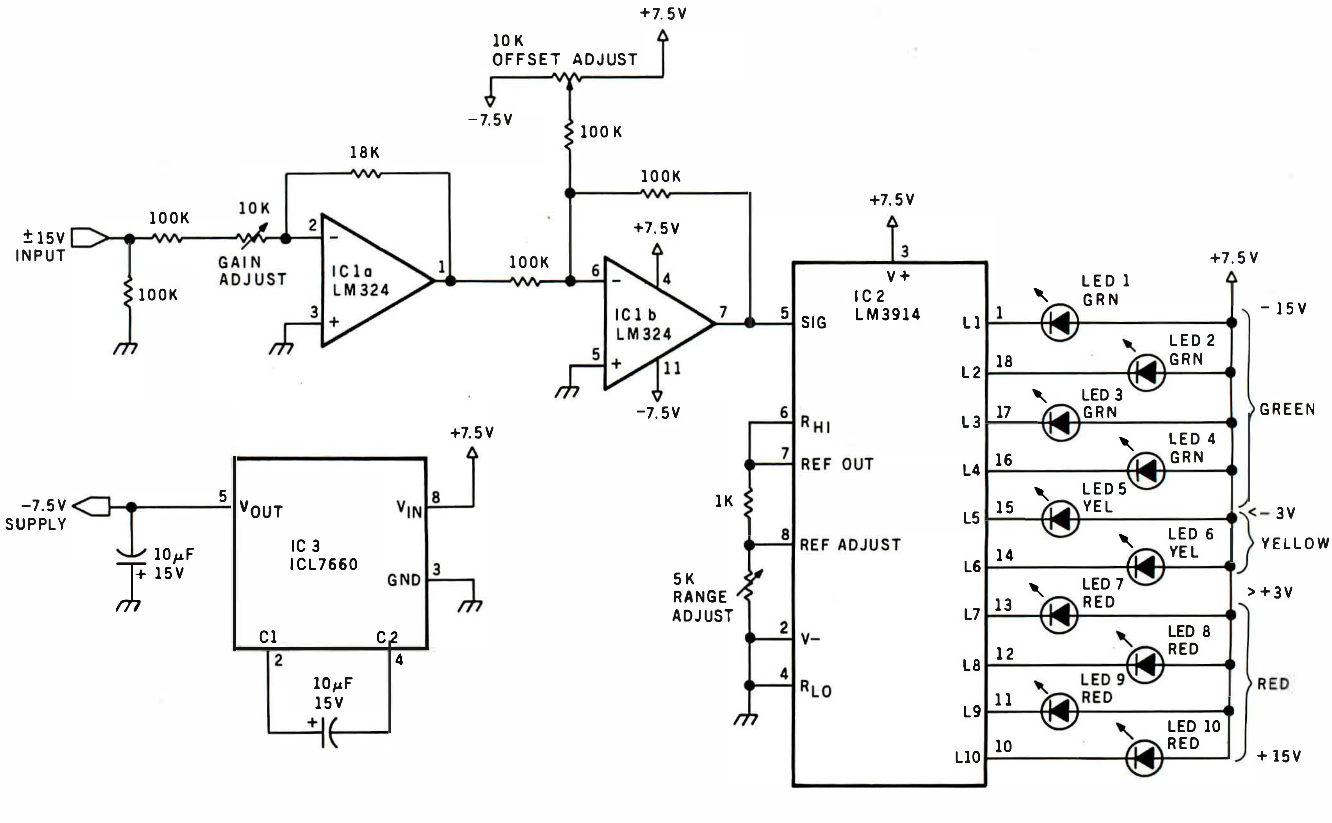
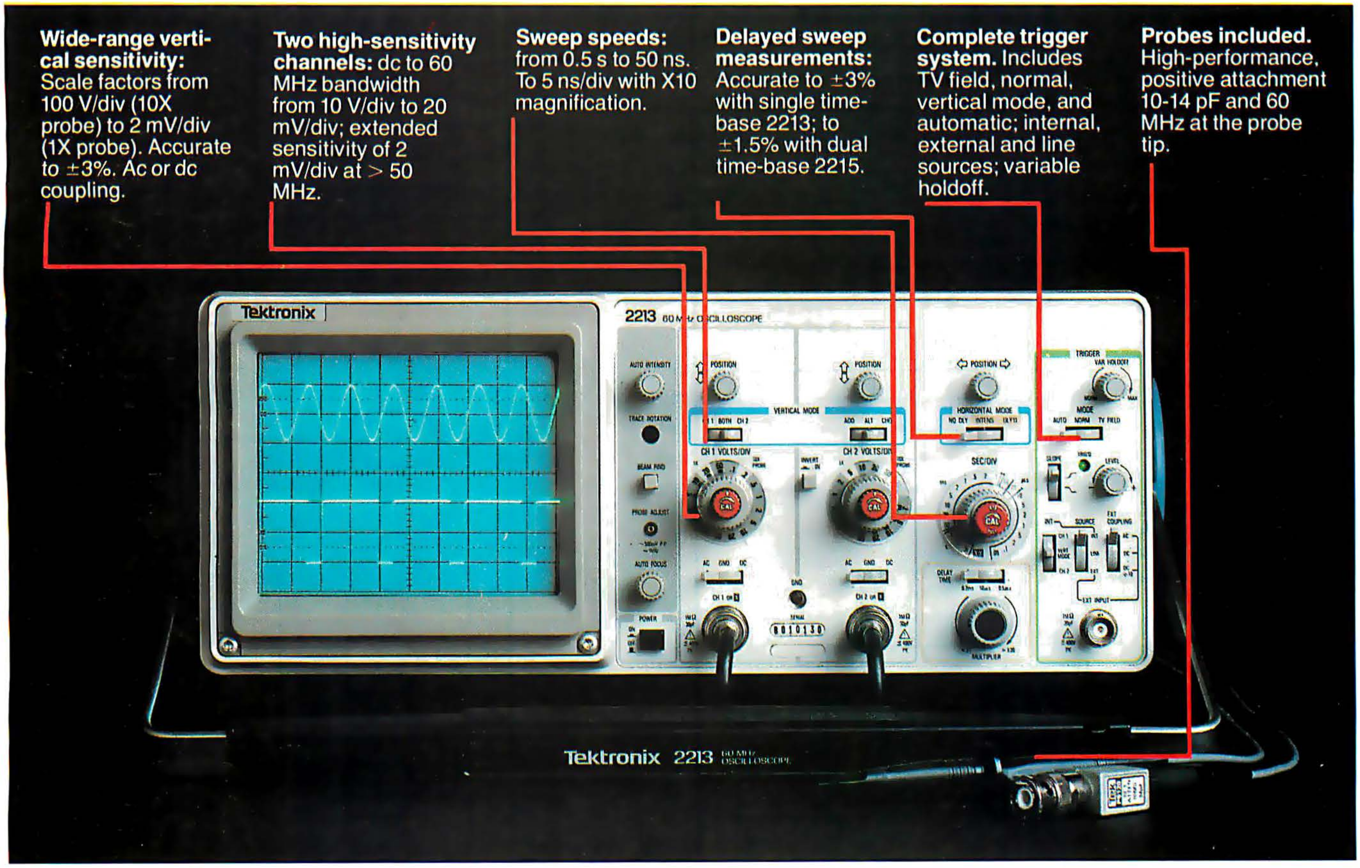


Figure 5: *A decade-voltmeter circuit. This more precise indicator may be substituted for the twelfth indicator in the breakout box of figure 4a. It lights up in one of three colors depending on the voltage present on its input.*

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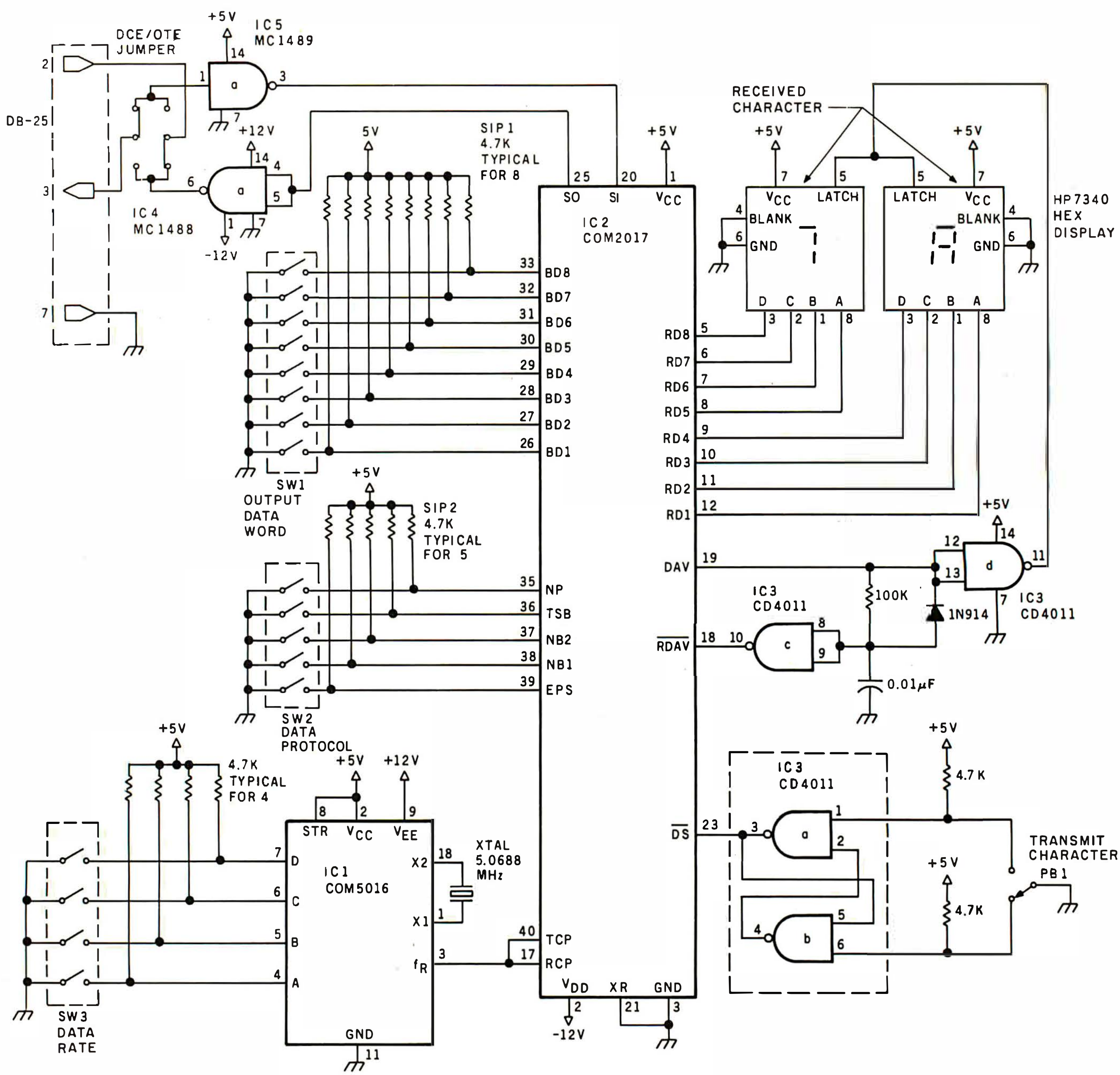


Figure 6: *A terminal-simulator circuit used to test the functioning of an RS-232C communication link. This simple-minded device transmits a single, switch-selected ASCII character on demand or receives a single character for display in hexadecimal form.*

ceiver/transmitter), IC2, to generate and accept data on the RS-232C line. (Because I have written elsewhere about the functioning of UARTs, I won't take the time now. See reference 2 for more information.) IC1 is a crystal-controlled data-rate generator. Depending on the settings of SW3, the clock rate of the UART will be set for one of the 16 data rates. Both the transmitter and receiver are set to the same rate.

The transmitter section is very simple. SW2 sets the status inputs to the UART for parity, word length, and stop bits. The character to be transmitted is set on SW1 (the most significant bit is BD8) in hexadecimal or binary format. It is transmitted each time pushbutton switch PB1 is pressed.

Data reception is just as easy. When a character has been received, the DAV (data available) output line of the UART goes high, and the received character can be read from the output lines RD1 through RD8. The DAV signal is delayed, inverted and used to reset itself through the RDAV input. This same logic signal is used to latch the 8 data bits onto a 2-digit hexadecimal LED display. Each time a character is received, the display will be updated, although you won't be able to read a continuous data stream.

Of course, more sophisticated commercial terminal simulators exist that incorporate some processing power,

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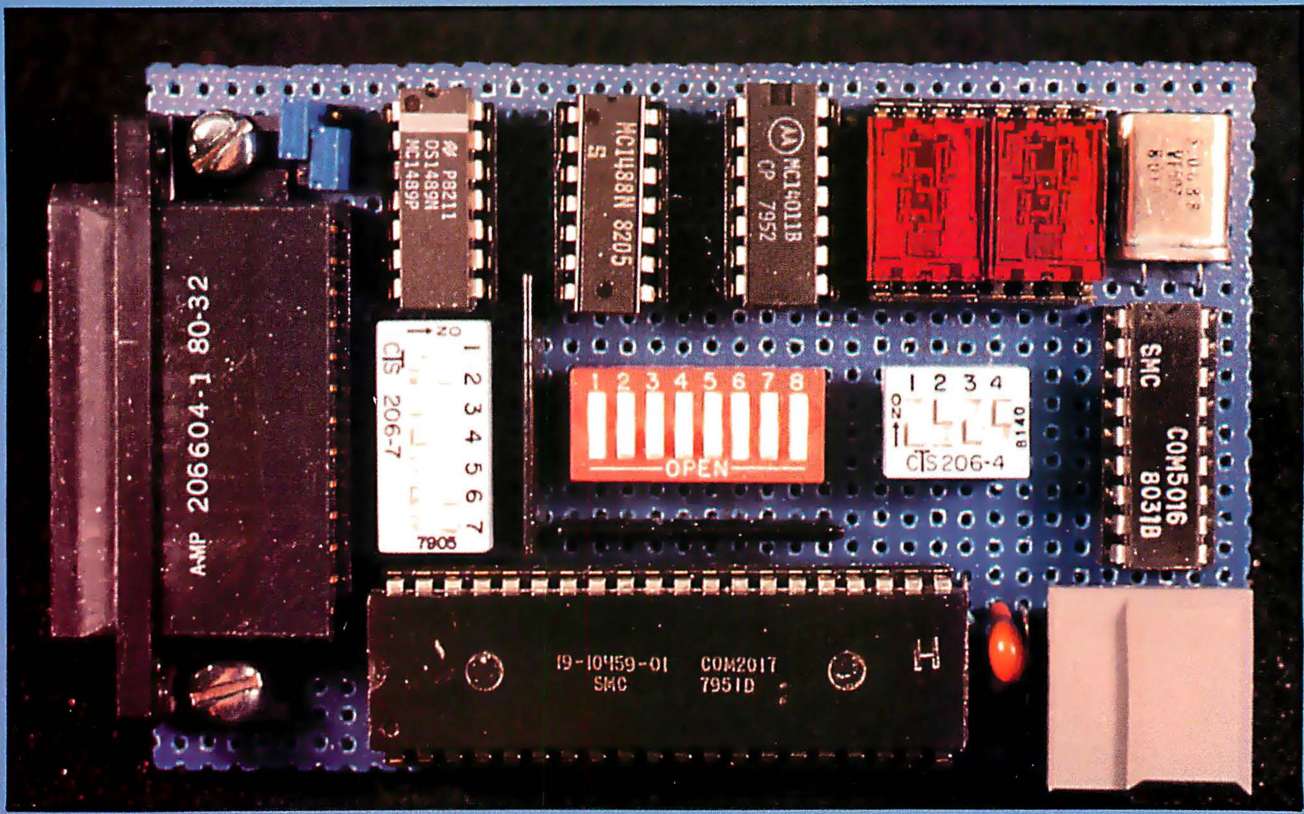


Photo 3: *Prototype of the terminal simulator of figure 6.*

but this one is simple enough to build yourself. Practically speaking, if I need more capability than this, I generally use a video terminal.

In Conclusion

This has been a rather long soliloquy on a rather oblique problem. I helped our shopping-bag computer hacker understand a little more about RS-232C, but a similar disaster might happen to him the next time he attempts to attach two serial devices.

As Dr. Witten has observed, most of the problems we find in using the RS-232C interface result from its being employed in ways never intended when it was invented.

For some of us, however, there's a light-emitting diode at the end of the tunnel. We can just whip out our little breakout boxes with all the pretty lights, decipher what's in or out, simulate all the handshaking signals, jumper everything to everything else, and make it communicate by brute force.

I'll probably still spend a few hours hooking up the Daisywriter 2000 I just got for my MPX-16. Nonetheless, maybe using some of the circuits I've presented will help cut down your frustration with RS-232C interconnections.

Next Month:

Build an RS-232C code-activated peripheral-device switch. ■

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Ciarcia's Circuit Cellar, Volume I, *covers articles that appeared in BYTE from September 1977 through November 1978.* Ciarcia's Circuit Cellar, Volume II, *contains articles from December 1978 through June 1980.* Ciarcia's Circuit Cellar, Volume III, *contains the articles that were published from July 1980 through December 1981.*

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The National Semiconductor NS16000 Microprocessor Family

The NS16000 family offers features formerly available only in much larger systems, but in a combination not available on any one system.

Glenn Leedy
National Semiconductor
Microprocessor Systems Division
2900 Semiconductor Drive
Santa Clara, CA 95051

The advent of extremely fast VLSI (very-large-scale integration) technology is quickly eradicating the gap between 8-bit small computer systems and 32-bit mini/mainframes. This decreasing gap means that many users now expect the performance and capacity of a large and costly mainframe to be combined with the flexibilities and economies of a microprocessor. The National Semiconductor Corporation has developed the NS16000 family of 16-/32-bit microprocessors to meet that expectation. (See table 1.)

The NS16000 is the only microprocessor with full 32-bit capability in the arithmetic logic unit (ALU) and internal data paths; the other major microprocessors with 32-bit capability, those in the MC68000 family, have 32-bit registers but a 16-bit arithmetic logic unit and data path.

Virtual memory is the expansion of the computer's capability to include both physical or main memory and external or secondary memory.

The NS16000 fully supports demand-paged virtual memory addressing, totally implemented by memory-management hardware. Transparent to both programmer and user, who see just an extension of the microprocessor instruction set, the NS16000's memory-management unit (MMU), the NS16082, is capable of providing a uniform 16 megabytes of virtual memory per user, eliminating the disadvantages of memory segmentation schemes.

Virtual memory allows you to combine a minimum of expensive primary storage (main memory) with lower-cost secondary memory. In this way, you can take full advantage of extremely large operating-system software and applications programs (now offered on large mainframes) without worrying about the hardware limitations of your system.

The "symmetrical" architecture of the NS16000 means that any data type can be used with any instruction (where appropriate), any addressing mode, and any operand source or destination. Because of this, you may be able to accomplish a given task with fewer instructions than you would with a microprocessor that has a less regular instruction set.

Additionally, the NS16000 has high-level language architecture, which means that it can execute high-level language instructions at speeds and code densities approaching as-

About the Author

Glenn Leedy is the marketing manager of external software products for the National Semiconductor NS16000 family. He has worked as a systems-software development engineer at IBM, Sycor, and Digital Equipment Corporation. At DEC he also served on the VAX software design team and as strategic market planner for low-end and fault-tolerant/high-availability systems.

(1a)

System

• A total 32-bit high-performance computer system with slaved 32-bit and 64-bit floating-point processing and 16-megabyte uniform virtual-memory management

• This family of chips will be offered at 6-MHz and 10-MHz processing rates during 1983, and 12-MHz and 14-MHz in 1984

Hardware

Central Processing Unit

- True 32-bit instruction (registers, arithmetic logic unit, and data paths)
- Symmetrical architecture
- High-level language support
- Modular programming support
- Powerful instruction set:
  - Over 100 instructions
  - Addressing modes optimized for high-level language references
  - General two-address capability
  - Expansion via slave processors
- 48-pin package

NS16082 Memory-Management Unit

- Full hardware support for 16-megabyte uniform demand-paged virtual memory
- Dynamic address translation
- 32-entry translation cache
- Automatic instruction "abort" and "retry"
- Program debugging support:
  - Program-flow traceback
  - Two breakpoint registers
  - Break-on-branch mode
- Security implemented through access-level checking and dual-system and user address-space mapping
- 48-pin package

NS16081 Floating-Point Unit

- Both 32-bit and 64-bit operation
- 8 general-purpose 32-bit registers
- Direct memory-to-memory operation
- High-speed instruction execution:

	32 bit	64 bit
Add	7.4 μs	7.4 μs
Multiply	4.8 μs	6.2 μs
Divide	8.9 μs	11.8 μs

- Conforms to IEEE FPU format
- 24-pin package

sembly language. [*This is an ambitious claim that will be verified only after advanced compilers have been written for this microprocessor and benchmarked. . . .* **G. W.**] Traditionally, high-level language programs have taken up to three times longer or more to execute than assembly-language programs and have required substantially larger memory space. Information from users of NS16000-based systems leads us to believe that code produced by NS16000-based compilers averages 40 percent longer than that produced by a human assembly-language programmer. We have also found that such code is considerably more compact and runs faster than that produced by compilers for the other major microprocessors.

Consistent with its high-level language capability, the NS16000 family supports modular programming techniques that allow you to divide complex programs into simpler, independent tasks and routines, each of which you can easily link for maximum efficiency. The NS16000 microprocessors even let you dynamically reconfigure and link together ROM-based software modules meant for any NS16000-based system. This can be done by using the NS16000 *link table* facility (to access both external software modules and global variables) along with the "external" addressing mode available to all NS16000 instructions.

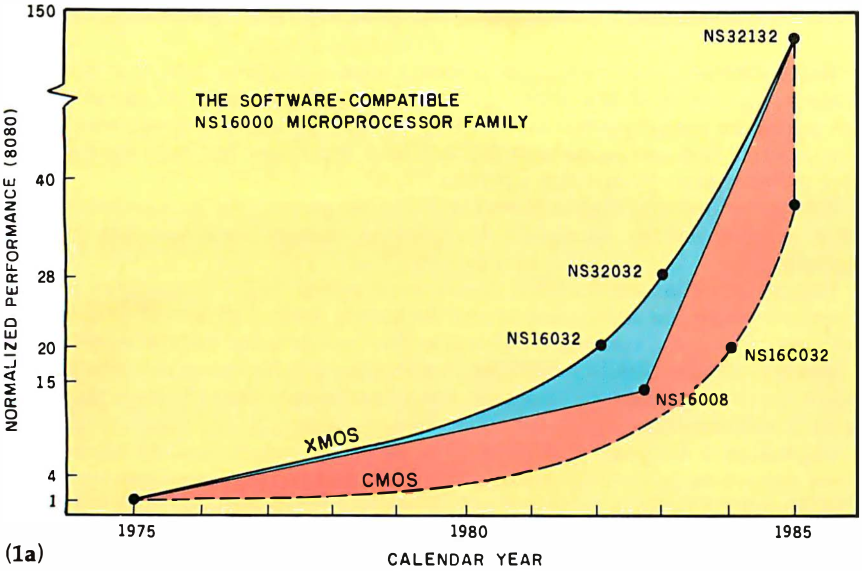
For more powerful performance in using high-level language programs,

(1b)

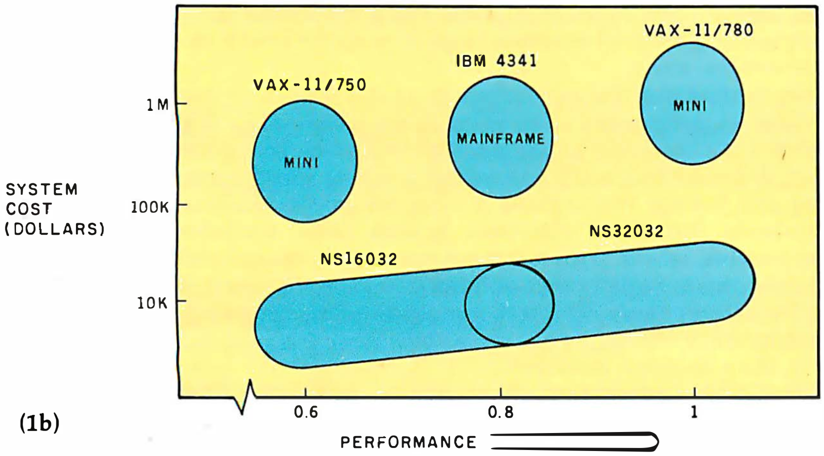
Microprocessor Characteristics

	NS16008	NS16032	NS16C032	NS32032	NS32132
registers	32 bit	32 bit	(low-power	32 bit	32 bit
arithmetic logic unit	32 bit	32 bit	CMOS	32 bit	32 bit
internal data path	32 bit	32 bit	version	32 bit	32 bit
external data path	8 bit	16 bit	of	32 bit	32 bit
real memory address	24 bit	24 bit	NS16032	24 bit	29 bit
virtual memory capabilities (with MMU support)	none	24 bit address (16 megabytes)	with same characteristics)	24 bit address (16 megabytes)	32 bit address (4 gigabytes)

Table 1: *An overview of the NS16000 family hardware (table 1a) and various configurations of the microprocessor (table 1b).*



(1a)



(1b)

Figure 1: *The NS16000 family facts and performance. Figure 1a shows the performance of various members of the NS16000 family, while figure 1b compares the performance of the NS16032 and NS32032 with that of several minicomputers and mainframes.*

the NS16000 features an instruction set with over 100 instructions, each of which is able to operate on up to five operand types. There are nine addressing modes, five of which enhance the use of high-level languages. In addition, all the code produced by the NS16000 instruction set is totally relocatable.

The NS16000 can execute operations (including all shift, logical, and arithmetic instructions) with both values in memory—known as a "two-address" capability. Combined with such features as multiple-way branching, a check instruction (to see if a value is within given limits), and string instructions, it becomes easy to write compact programs in both high-level and assembly languages.

To carry out floating-point processing, memory management, or any other customized function for that matter, the NS16000 gives these operations to dedicated hardware. Such operations are made even faster by the use of special control and status lines that allow multiplexed inter-processor communication at speeds above normal processor-peripheral data-interchange rates. For example, the NS16081 floating-point unit (FPU) can carry out a divide operation in only 8.9 microseconds (32-bit) and 11.8 microseconds (double-precision 64 bit) at 10 MHz, from 3 to 10 times faster than competitive units now on the market.

A comparison of the NS16000 family with popular minicomputers and mainframes now on the market shows how you can benefit from the high price/performance ratio of these microcomputers (see figure 1).

True Mainframe Performance

In order for a small microprocessor system to expand to the full capability of a mainframe, its architecture—the interface between the computer and its software—must optimize performance without compromising user protection. The system must accommodate the largest of user applications and yet remain cost-effective. Above all, it must be able to use the enormous software inventory now available on mainframes to avoid obsolescence and minimize cost. At National Semiconductor, we decided that the most effective way to achieve these design criteria was by implementing the following features: a highly symmetrical architecture, high-level language support, modular software support; a powerful instruction set, demand-paged virtual-memory support, and a memory-management unit.

Symmetrical Architecture

In the context of machine architecture, *symmetry* is the degree to which any data type can be used with any instruction, with any addressing mode, and with any operand source or destination. Symmetry is of paramount importance when implementing space- and time-efficient high-level languages.

High-Level Language Support

Programming in a high-level language (C, Pascal, PL/I, BASIC, FORTRAN, and COBOL, for example) is far more productive than programming in assembly language, which can be extremely tedious and time-consuming. A high-level language programmer often can produce the same number of debugged lines of code per day as an assembly language programmer; however, a line of high-

level language code usually performs a far more complex operation than a line of assembly-language code.

In the past, code generated by high-level languages required larger amounts of memory and took longer to execute. Depending on the compiler, computer, and applications, a compiled program might be well over three times longer and slower than the best assembly-language program. The basic reason: most contemporary architectures were not designed to support compilers.

The NS16000 family, with its symmetrical architecture, general-purpose registers, and other features, has eliminated these architectural deficiencies. Designed specifically to support high-level language compilers, the NS16000 family enables even relatively unsophisticated compilers to produce efficient code.

Because they can more efficiently translate high-level languages, compilers on the NS16000 can actually generate instruction-code densities approaching those of assembly language.

Another feature of the NS16000 is its *expanded addressing* capability. In addition to four standard addressing modes common to other microprocessors—register, immediate, absolute, and register relative—the new NS16000 has an additional five unique addressing modes oriented toward high-level languages: top-of-stack, memory, memory-relative, external, and scaled-index.

The *top-of-stack (TOS) mode* is useful for evaluating arithmetic expressions in a high-level language quickly and with a minimum number of instruction bytes. Any operand, or both operands, of an instruction may be referred to by the top-of-stack addressing mode. The operand is pushed onto the current stack, popped from it, or referenced without modifying the stack pointer. Most other microprocessors, which limit top-of-stack addressing to a small number of instructions, require several instructions to achieve the same result as one NS16000 family instruction.

The *memory mode* is similar to the standard register-relative mode, which allows memory to be accessed relative to one of four special-purpose registers. This mode simplifies many constructs needed by high-level language interpreters and compilers.

The *memory-relative mode* is used to manipulate fields in a record and allows pointers located in memory to be used directly without having to be loaded into registers, as with other microprocessors.

The *external mode*, unique to the NS16000, supports a modular software concept (to be explained later), allowing modules to be relocated without traditional code modification in linkage editing.

The *scaled-index mode* is used to access elements in byte, word, double-word, or quadruple-word arrays. It computes the operand address from one of the general-purpose registers and a second addressing mode, which allows automatic indexing into tables of 1-, 2-, 4-, or 8-byte entries.

Move instructions *(5 instruction groups, 3 single instructions; total 18 instructions):* These instructions move data among memory locations and registers. As with all instruction groups, the instructions that are part of an instruction group have three forms: byte (8 bits), word (16 bits), and double word (32 bits). Here, this means that many move instructions will work on 8-, 16-, or 32-bit quantities.

Integer arithmetic instructions *(14 instruction groups; total 42 instructions):* This group includes addition, subtraction, multiplication, division, remainder, and modulus operations.

Packed decimal instructions *(2 instruction groups; total 6 instructions):* The two operations are packed addition and packed subtraction. When used with 32-bit operands, this gives addition and subtraction instructions that work on 8-digit decimal numbers.

Integer comparison instructions *(3 instruction groups; total 9 instructions):* One instruction allows a comparison of a value with a 4-bit constant; normally, operands can be 8, 16, or 43 bits wide.

Logical and Boolean instructions *(7 instruction groups; total 21 instructions):* These instructions perform logical and, or, xor (exclusive or), and complement functions.

Shift instructions *(3 instruction groups; total 9 instructions):* This group includes a rotate instruction and both arithmetic and logical shift instructions.

Bit-manipulation instructions *(7 instruction groups, total 21 instructions):* This group includes various test, set, clear, and invert operations.

Bit-field instructions *(4 instruction groups, 1 single instruction; total 13 instructions):* This is a very useful group of instructions that allows you to interpret a series of bytes as a record of bits and manipulate arbitrarily placed subfields within this record.

Array instructions *(2 instruction groups; total 6 instructions):* One instruction checks a value to see if it is within an acceptable range of values; the other is used to help index into multidimensional arrays.

String instructions *(3 instruction groups, 3 single instructions; total 12 instructions):* This versatile set of instructions allows you to compare, skip over, or move strings. Various options allow the operations to take place starting at the end of the strings, working backward, and to continue until a match either occurs or doesn't occur.

Jump and linkage instructions *(2 instruction groups, 16 single instructions; total 20 instructions):* This set of instructions includes jumps, subroutine calls, case-like multiway branches, returns, jumps to external routines, and debugging-related instructions.

Microprocessor register instructions *(5 instruction groups, 3 single instructions; total 18 instructions):* These instructions manipulate the microprocessor's registers.

Miscellaneous instructions *(3 single instructions):* This group includes a wait, a no-operation, and a diagnostic instruction.

Floating-point instructions *(4 instruction groups of 6 instructions each, 8 instruction groups of 3 instructions each, 4 single instructions; total 52 instructions):* This group includes various floating-point arithmetic operations and instructions to convert to other forms. These instructions are available only if the NS16081 floating-point unit is connected.

Memory-management instructions *(2 instruction groups, 4 single instructions; total 10 instructions):* These instructions are available only if the NS16082 memory-management unit is connected.

Custom slave instructions *(20 instruction types, most with more than one form):* These open-ended instructions allow you to interact with an unspecified "slave" processor connected to the NS16000 family microprocessor. This scheme allows the NS16000 family to interact with performance-enhancing processors yet to be designed.

Table 2: *An overview of the NS16000 family instruction set.*

In general, high-level language programs reduce software obsolescence, one of the major problems facing the computer user, because these programs can be used on other systems with different architectures. In contrast, assembly languages are tailored to a specific computer instruction set and are rarely transportable.

Modular Software Support

Because the very complexity of large programs is one of the major factors contributing to software unreliability, decreasing the complexity increases reliability. Modular programming accomplishes this by dividing complex programming tasks into smaller and simpler subtasks, or modules, each of which performs a well-defined portion of the overall task.

You can develop each module independently of all other modules, without concern for inter-module addressing or *linking*. Using this approach, you can significantly reduce both software development costs and programming time. You can also increase program flexibility and simplify operating-system design.

Until the NS16000, microprocessors could not easily implement the concept of modular programming in ROM (read-only memory) because program code had to be modified to access specific data blocks and external procedures in a system. This significantly limited the use of programs written in ROM, which is unfortunate because if modules *could* be put into ROMs, you could build a very helpful library of ROM-based modules that could be used as needed in various applications.

Software modularity is an important issue because it is included in the structure of many high-level languages. For example, programs in Ada (a new Department of Defense high-level language) are composed of one or more subprograms, packages, or tasks, each of which can be compiled separately. In Pascal, program modules may refer to variables, functions, or procedures contained in another module by the use of extensions to the language.

Modular programs are more likely to be correct and are easier to understand; hence, they are readily modified, maintained, and documented. And because inter-modular communication can be accomplished through well-defined interfaces, the inner operations of a module do not have to be known to another module.

An important part of modular programming, especially to the software designer, is the operating system. National Semiconductor realizes that one operating system, however successful, is not a sufficient software base for a new microprocessor. Because of this, the NS16000 will be supported by several choices in operating systems. The Pick operating system is a generic system already in use at nearly 20,000 facilities on a variety of computer systems. In the future, the following operating systems will also be available for the NS16000 family: Xenix (Microsoft's extended, licensed version of Bell Laboratories' Unix); Oasis-16 (Phase One Systems); CP/M, Concurrent CP/M, and CP/NET (Digital Research Inc.); and the UCSD p-System (Softech Microsystem's version, modified to use the NS16000's larger address space). Through these operating systems, you will have available a variety of application programs and programming languages.

One of the critical decisions made by designers of computer memory organizations concerns the "swapping" of data in and out of main memory.

A Powerful Instruction Set

In addition to symmetrical architecture, modular software, and expanded addressing, high-level languages on the new National Semiconductor microprocessor family are supported by a sophisticated instruction set, which determines computing capability and programming effectiveness.

In the NS16000, there are over 100 instructions (see table 2), all chosen on the basis of their frequency of use, and each able to operate on up to five operand types. Because the set is symmetrical, instructions can be used (where appropriate) with any length operand, in any addressing mode, and with any general-purpose register.

Demand-Paged Virtual-Memory Support

While large-address-space programs and multitask/multiuser environments have always existed, microprocessors have had a hard time servicing them. Developed over a decade ago, the microprocessor was designed as a general-purpose device that was software programmable and therefore an alternative to a prohibitively expensive special-purpose chip. In addition, early microprocessors were rarely capable of exceeding a memory address of 16K bytes. Even today, many microprocessor systems are limited to 64K bytes of total memory or memory segments.

Basically, there are three aspects of memory organization: the entire memory structure, which is how the logical memory looks to the user and program; the mapping of logical memory to actual (physical) memory, called *address translation*; and finally, *virtual memory*, which is the expansion of the computer's capability to include both physical or main memory and external secondary memory such as disk-drive systems, with switching between the two being handled automatically.

The NS16000 uses a virtual memory organization. This organization solves two problems: the need for logical address spaces larger than physical memory, and the expense incurred by adding main memory. With virtual memory, the NS16000 stores only a minimum of logical-address information in physical memory, with the remainder located in low-cost disk memory until that information is needed to carry out a program instruction.

The architecture of this memory

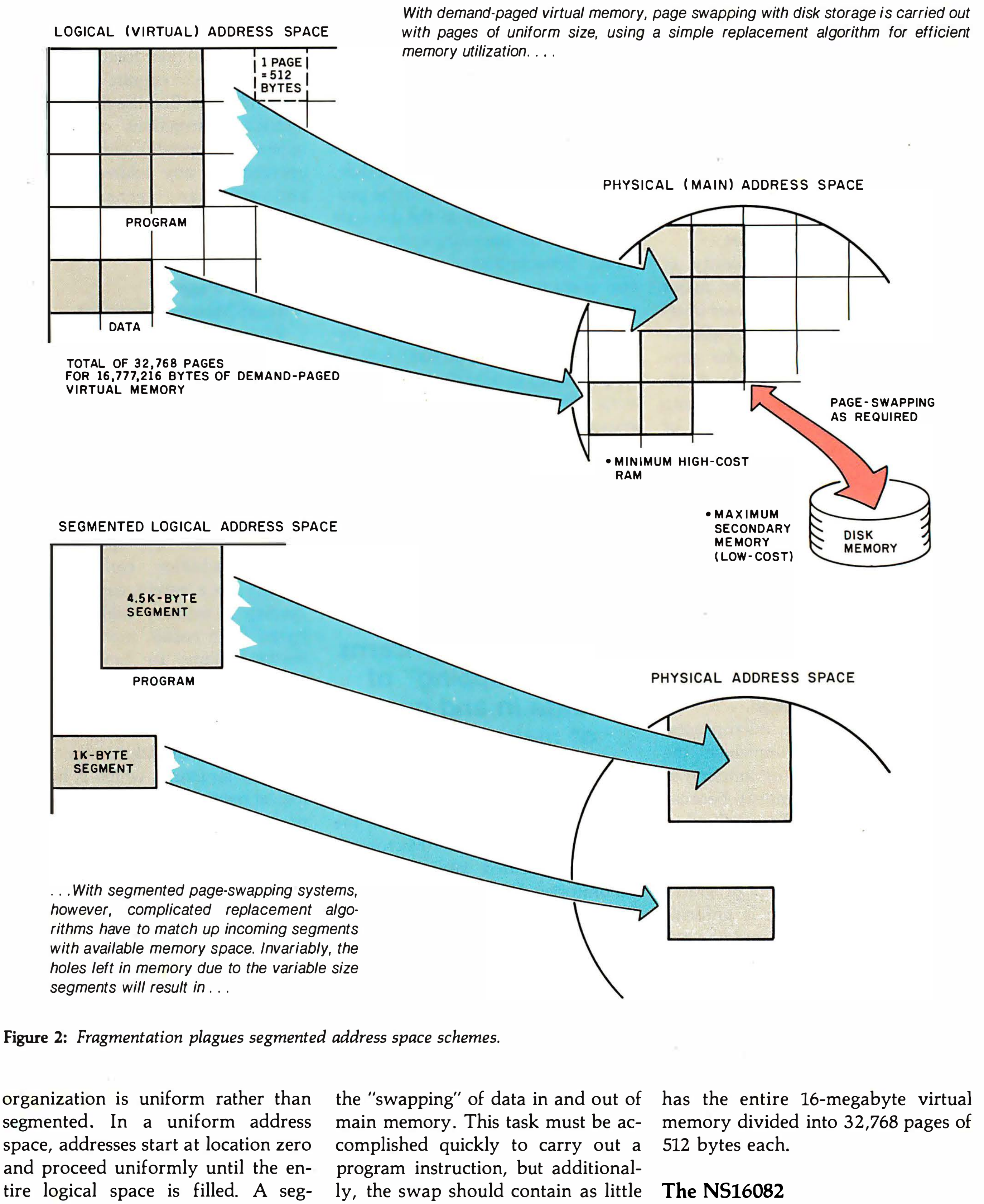


Figure 2: *Fragmentation plagues segmented address space schemes.*

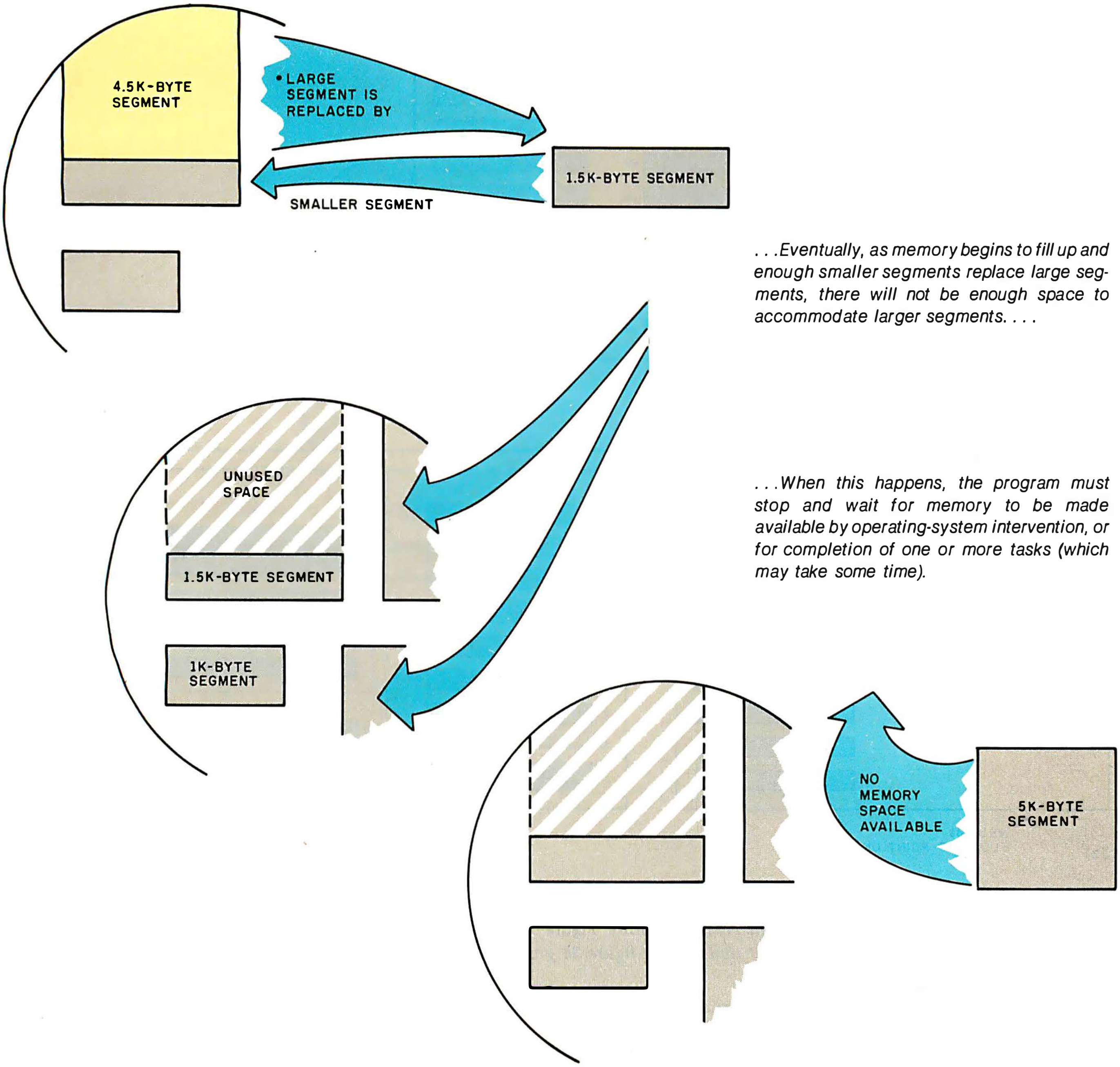
organization is uniform rather than segmented. In a uniform address space, addresses start at location zero and proceed uniformly until the entire logical space is filled. A segmented address space consists of a collection of smaller uniform address spaces. (See figure 2 for some of the problems with segmented address space schemes.) One of the critical decisions made by designers of computer memory organizations concerns the "swapping" of data in and out of main memory. This task must be accomplished quickly to carry out a program instruction, but additionally, the swap should contain as little unusable data as possible. The size of this swap is called a page, and in a uniform memory space, it can be any size the designer wants it to be. In a segmented memory system, the size of the swap is already determined by the size of the segment. The NS16000 has the entire 16-megabyte virtual memory divided into 32,768 pages of 512 bytes each.

The NS16082 Memory-Management Unit

Successful management of the virtual-memory system is the function of the NS16082 memory-management unit. In addition to translating the logical (virtual) addresses generated by the NS16032/NS16C032/NS32032

SEGMENTED
PHYSICAL ADDRESS SPACE

. . .fragmentation. This occurs when—as page segments are swapped—larger segments begin to be replaced by smaller segments, creating unused free space. . . .



. . .Eventually, as memory begins to fill up and enough smaller segments replace large segments, there will not be enough space to accommodate larger segments. . . .

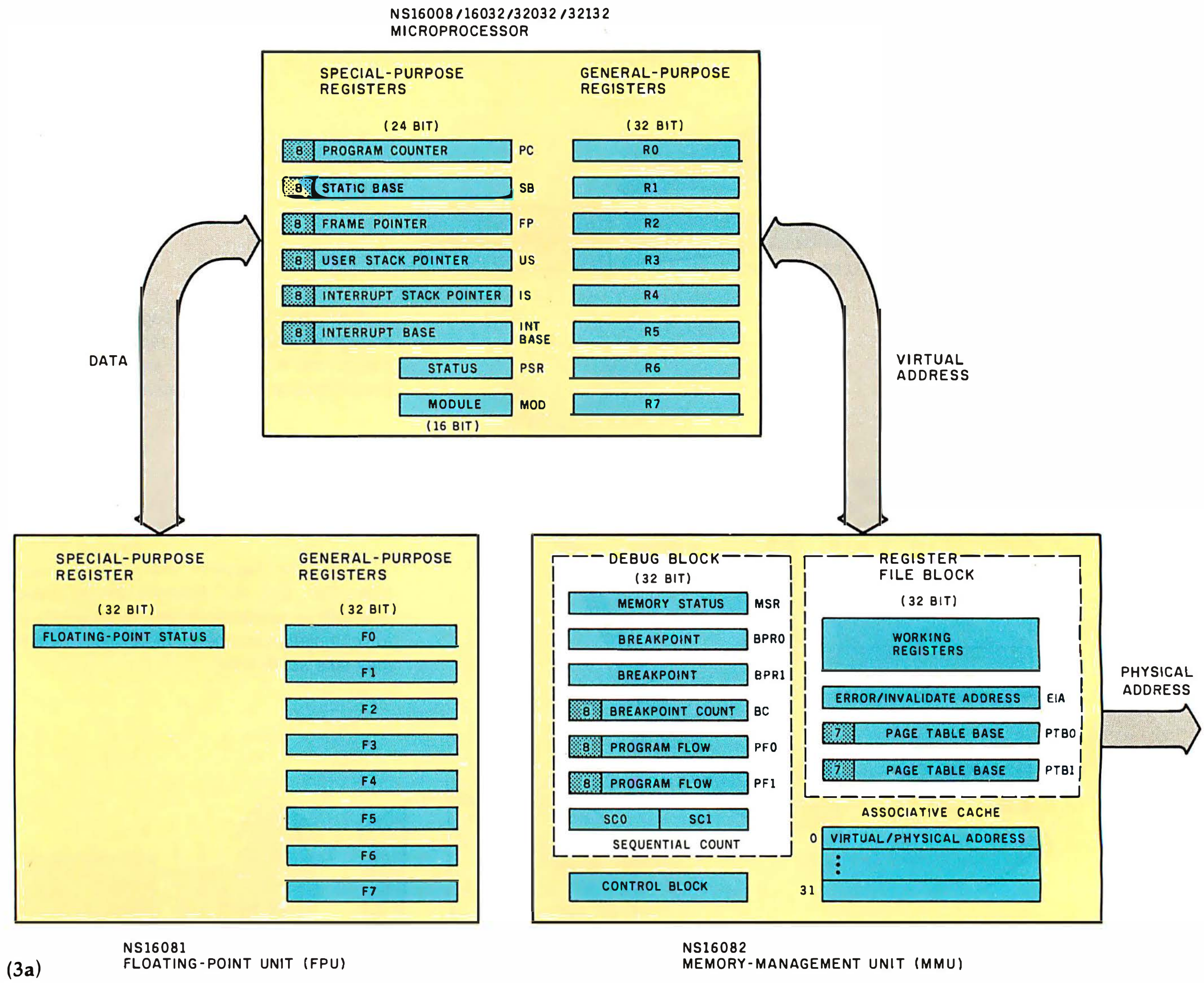
. . .When this happens, the program must stop and wait for memory to be made available by operating-system intervention, or for completion of one or more tasks (which may take some time).

Figure 2 continued

microprocessors into physical addresses, the memory-management unit can abort an instruction during execution by the microprocessor to load a nonmemory resident page and retry the same instruction immediately afterward. This feature is unique to the NS16000 system and is fully implemented in hardware.

Figures 3a and 3b give the logical and physical interconnections of the microprocessor and its memory-management and floating-point units. Important functions carried out by the memory-management unit are dynamic address translation using memory-page tables, on-chip cache for most recently used page-table entries, instruction abort and retry, and system debugging.

In *dynamic address translation,* the memory-management unit keeps track of the logical address requested by the microprocessor and its corresponding values in physical memory at all times. To do this, it uses page tables containing pointers that indicate where to go in physical memory (see figure 4). Surprisingly, both page and pointer tables do not require large amounts of memory. An entire 16-megabyte virtual-memory map will use only one 1024-byte page table to point to 256 pointer tables of 512 bytes each for a total of 132,096 bytes devoted to mapping, or approximate-



(3a)

Figure 3: *Component interconnection in the NS16000 family. Figure 3a shows the logical interconnection of the microprocessor and its memory-management and floating-point units, while figure 3b gives an overview of the physical interconnections.*

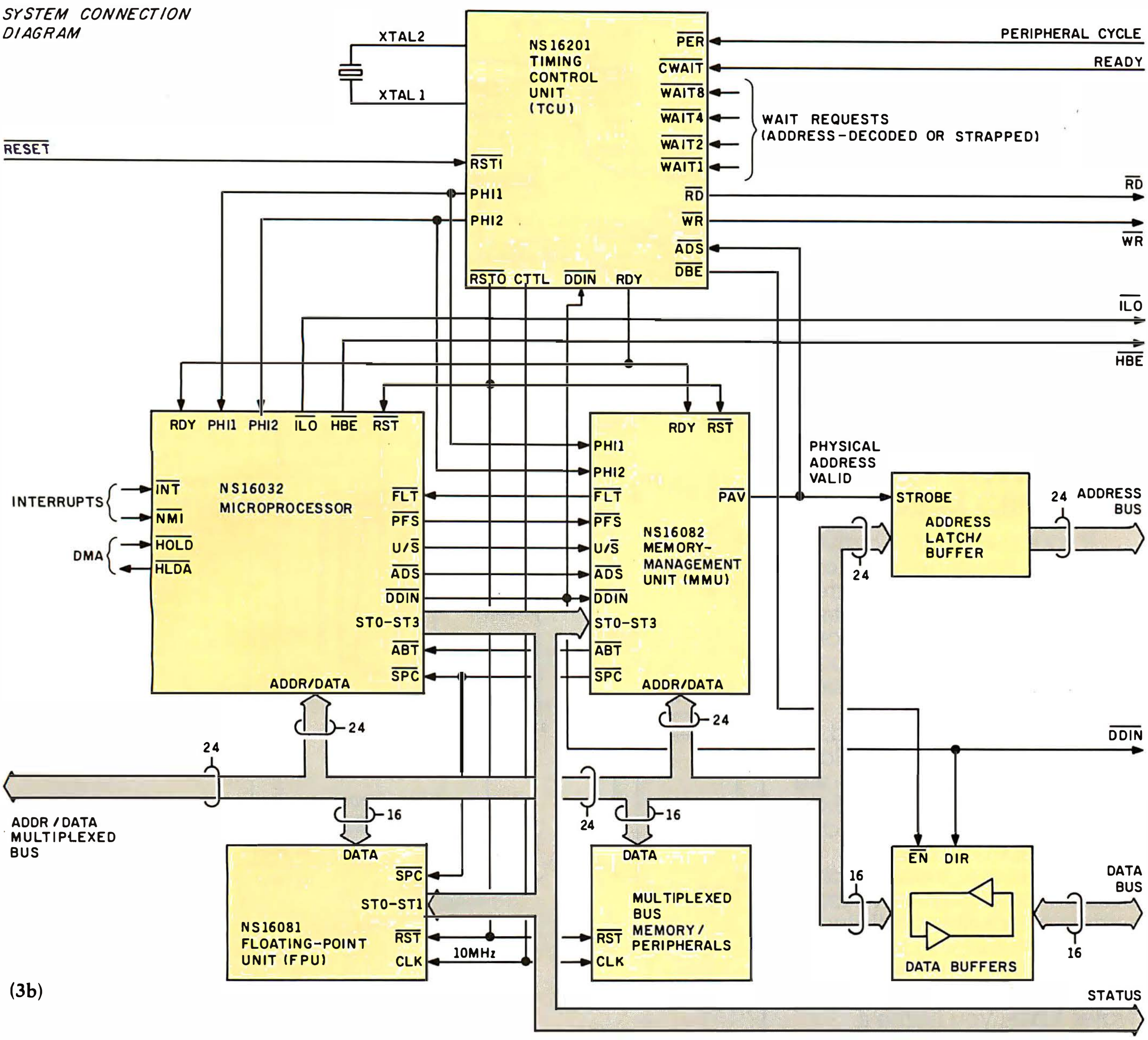
ly 0.8 percent memory overhead. The memory-management unit NS16082 provides an entire 16-megabyte virtual address space for each user.

The address space itself is divided into fixed pages of 512 bytes each, which enables the NS16000 to transfer data into and out of memory quickly.

When the microprocessor passes a virtual address to the memory-management unit, the latter first attemps to match it with a special *associative cache* contained on the chip. This cache contains the 32 most recently accessed virtual addresses, as well as their translated physical addresses. If the address requested by the microprocessor matches one of the 32 cache entries, the microprocessor is allowed access to the physical address immediately (see figure 5a). This virtual-to-physical address translation can occur in just one clock cycle, or 100 nanoseconds with a 10-MHz microprocessor clock. However, if the requested address is not present in the cache, the memory-management unit must fetch both page and pointer table entries from memory before address translation can be performed (see figure 5b). This can take up to 20 clock cycles, or 2 microseconds with a 10-MHz microprocessor clock.

The memory-management unit's associative cache, which operates transparently to the user, is an extraordinarily powerful tool in enhancing processing speeds. We have calculated that an address will be present in the cache about 97 percent of the time. This means that 97 percent of the data can be addressed with a typical virtual delay overhead of only one clock cycle.

The memory-management unit's *instruction abort and retry* features are perhaps its most significant. After fetching and decoding an instruction, the microprocessor sends the virtual addresses of the operand to the mem-



(3b)

ory-management unit. If the memory-management unit decides that the information resides in main memory, it translates the virtual address to the physical address directly, allowing the microprocessor to operate directly on the memory.

However, if the data does not reside in one of the pages of main memory, the memory-management unit will initiate a *page fault* and send a signal to the microprocessor to abort its instruction. (A memory-access abort will also occur if the microprocessor tries to access a protected section of memory.) Once the instruction has been stopped, any register that had been altered by the instruction will be returned to its original state.

A page fault is a hardware-generated trap that, in essence, tells the operating system to bring in the missing page containing the data from disk memory. (To signal whether a page or pointer-table entry is present in main memory or not, the page entry contains a "valid bit" for that purpose.)

Once a page fault is detected and an instruction aborted, the microprocessor then calls up the virtual-memory operating system routine, which locates the proper page containing the data in peripheral memory and loads it into main memory (see figure 5c). If no room exists in main memory, it is swapped with a page that is determined to be the most expendable (or least likely to be recalled). If the operating system can do multitasking, it is free to do other tasks while pages are being loaded. When the operating system has completed its page swap, it executes a "return from trap" instruction and the aborted instruction resumes.

Debugging is handled by the memory-management unit with *breakpointing* and *flow-tracing* techniques. Breakpointing is a tool used to test if

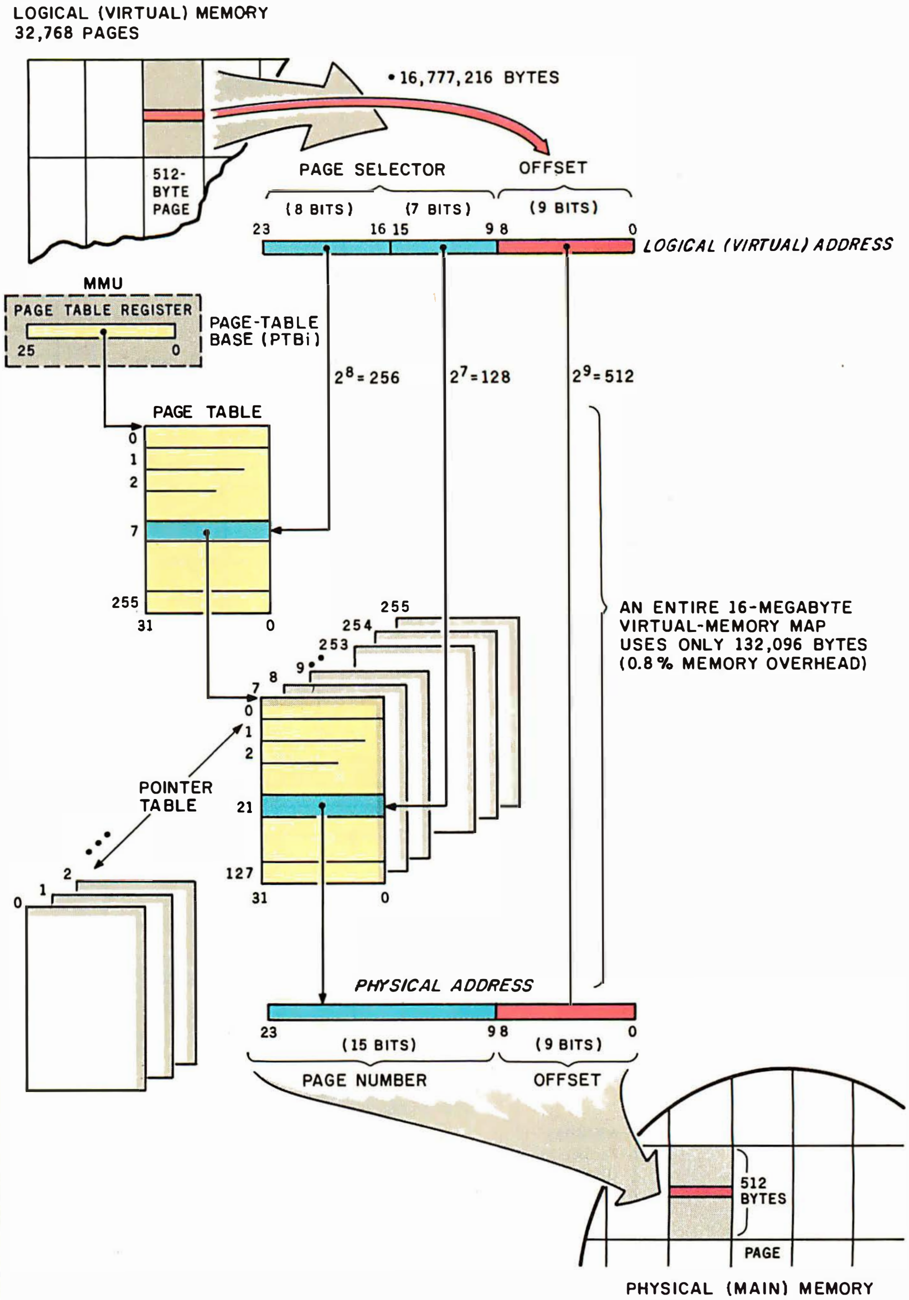


Figure 4: *Dynamic address translation in the NS16000 family.*

program execution is proceeding as planned. It can also be used to monitor data access. Often, a programming error may cause control to pass to a known location for some unknown reason. By using program flow tracing, the memory management unit follows the chronology of a program so that you can determine what went wrong. And because the memory-management unit's debugging facilities use hardware rather than software, they do not add to program execution time; therefore, these facilities can be used in a production and a development environment.

The NS16081 Floating-Point Unit

To understand how a floating-point unit can enhance an application area, you must first realize the advantages a floating-point unit brings to a microprocessor. First, all floating-point units allow a microprocessor system the flexibility of handling a great numeric range (either large or small) beyond the normal range of a microprocessor's registers.

Several factors must be considered

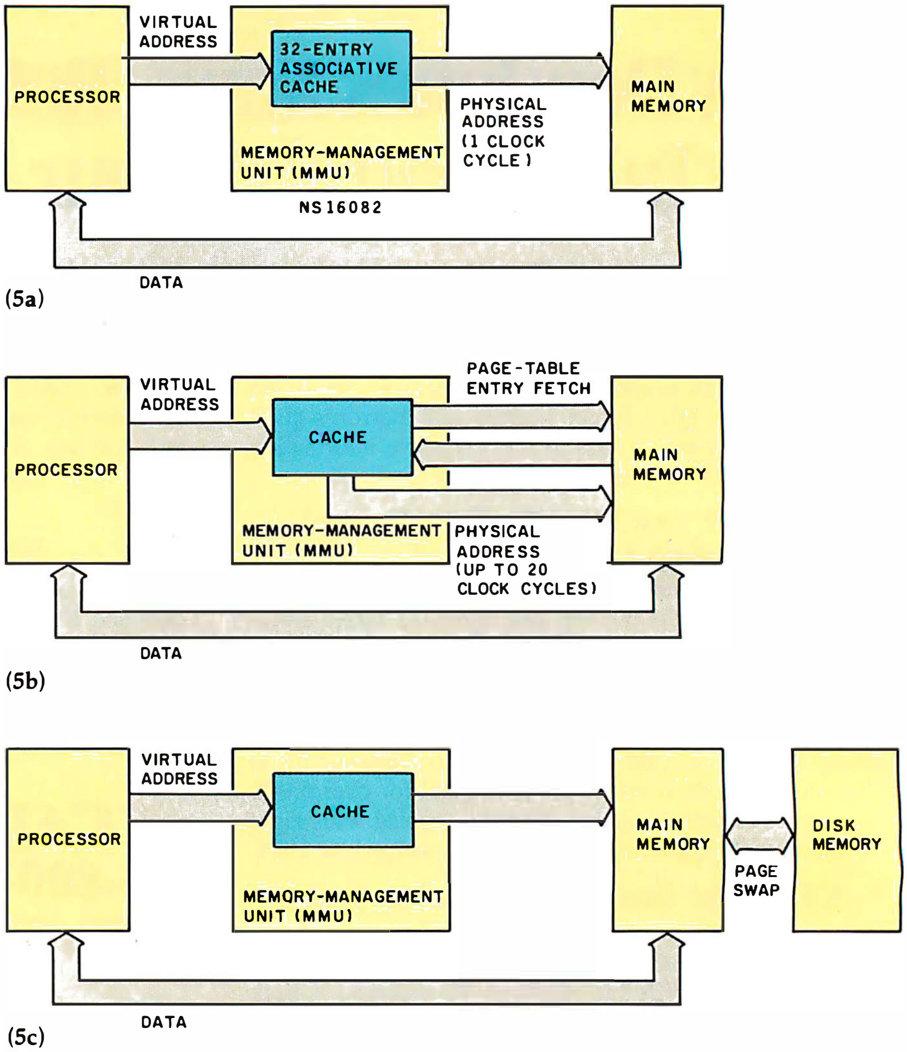


Figure 5: *Memory access through the NS16082 memory-management unit. If the page-table entry (PTE) is in the cache memory of the memory-management unit and the program page is in memory (figure 5a), data addressing is completed in only one clock cycle (100 nanoseconds with a 10 MHz system clock). If the page is resident in main memory but the PTE is not in the cache memory, a page-table entry must be fetched from main memory (figure 5b), normally requiring up to 20 clock cycles (2 microseconds). If the page is resident in disk memory, it must first be swapped into main memory (figure 5c), after which it is treated as in figure 5b.*

when designing a floating-point unit into a system. These include the method for handling a specific operation or instruction, the permissable length of actual data (operands), the amount of support that the floating-point unit expects from the rest of the system, and the interconnection schemes to enhance data communications to and from the chip.

The design of the NS16000 family fully supports 32-bit and 64-bit precision floating-point calculations through its NS16081 floating-point unit (FPU); the unaugmented microprocessor will handle 8-, 16-, and 32-bit fixed-point calculations. The NS16081 contains eight general-purpose onboard 32-bit registers, which you may use to provide either a single-precision (32-bit) or double-precision (64-bit) number (see figure 6).

While the eight general-purpose registers are reserved for actual data, a ninth 32-bit status register holds both control and error information. *Control* options include enabling microprocessor traps and floating-point error conditions and setting the operand rounding mode. *Error* conditions include traps for overflow, underflow, illegal division (division

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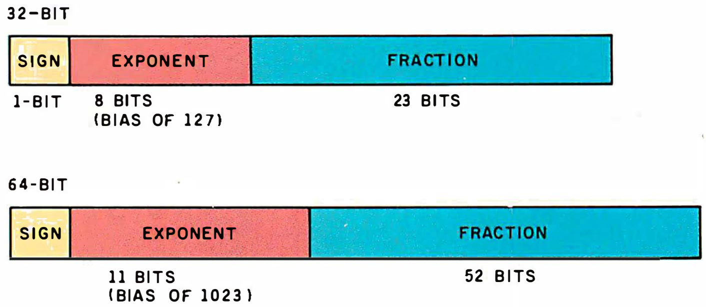


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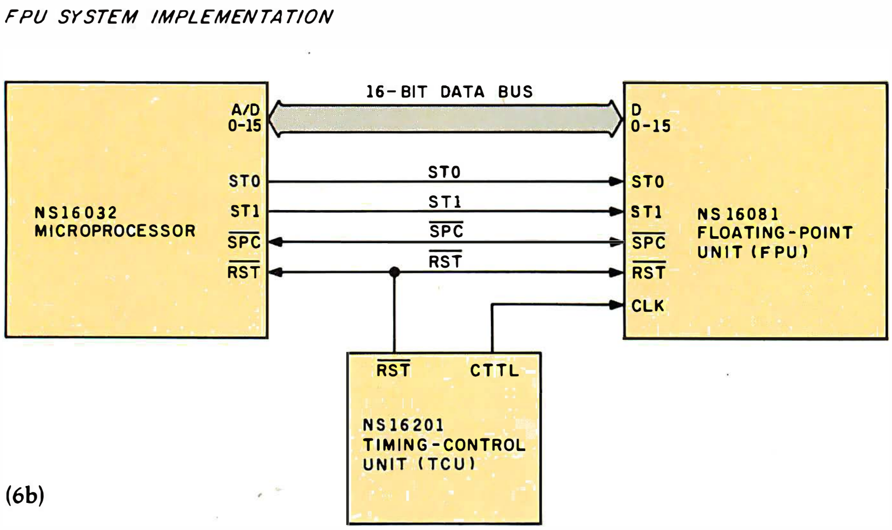
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(6a)



(6b)

Figure 6: *Floating-point numbers in the NS16000 family. Figure 6a shows the NS16000 format for standard (32-bit) and long (64-bit) floating-point numbers. Figure 6b shows an overview of the physical interconnection between the microprocessor and the floating-point unit.*

by zero), illegal instructions, inexact results, and undefined operand (for example, all-zero or all-one exponents). The programmer can individually enable or disable all the traps.

Unlike other microprocessor systems that support floating-point operations, the NS16000 architecture makes available to the floating-point unit all the system addressing modes, which aids efficient data handling. For example, in a scaled-index mode, an entry in a large array of floating-point data elements may be addressed by its logical index rather than by its physical address. This not only facilitates finding the data, but eliminates wasting time with unnecessary programming schemes.

Used in conjunction with the NS16082 memory management unit to simplify large-memory management and data retrieval, the NS16081 floating-point unit becomes an even faster and more efficient data cruncher. For example, not only are a full 16 megabytes of virtual memory available for data storage, but all of the data-retrieval, dynamic-address, and memory-protection capabilities of the memory management unit become part of floating-point routines.

The instruction set of the NS16081 floating-point unit is compatible with the proposed IEEE floating-point standard; its instruction set is summarized in table 2. The floating-point instructions use the same addressing modes as the other NS16000 instructions.

For greater speed, separate processors in the floating-point unit operate on each of the three principal segments of a number residing in either a 32-bit or 64-bit register—all under control of microcode. The first segment (containing 1 bit) is reserved for the sign, the second segment (8 or 11 bits) for the exponent, and the third segment (23 or 52 bits) for the fraction or mantissa.

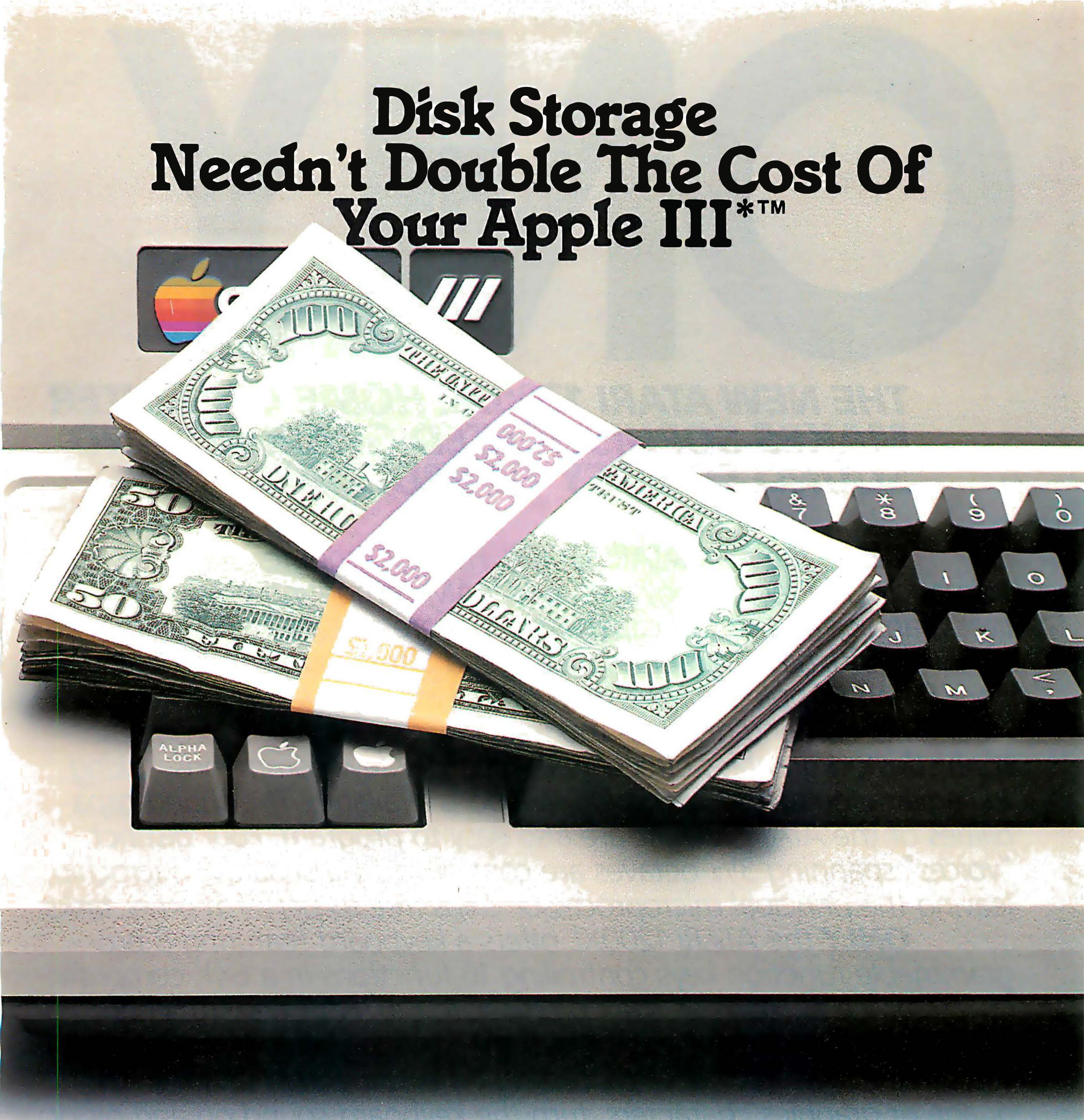
Conclusions

The simplicity and efficiency of some of the concepts discussed here might lead you to believe that popular large computer systems would have integrated these features into their designs long ago. Not so. The IBM 360, 370, 43xx, and 30xx, for example, well known for their number-crunching abilities, do not possess symmetrical architectures, nor do they show much support of high-level languages and modular software. And—despite their high cost—these large systems currently offer no more than 16 megabytes of virtual memory. In these systems, sophisticated functions are carried out by slow, complex software, with lost time being made up by speedy (and costly) parallel-processing hardware techniques.

Digital Equipment Corporation's VAX minicomputer systems, on the other hand, do have a high degree of symmetrical architecture and support virtual memory. As a result, they offer a full 32-bit, 4-gigabyte virtual memory but at a cost some 20 to 30 times that expected for systems now being developed by manufacturers using National Semiconductor's new 16-/32-bit NS16000 family.

In short, the NS16000 family offers features formerly available only in much larger systems but in a combination not available on any one system. This family of microprocessors promises to be the foundation of a new generation of high-performance, low-cost computers. ■

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Design Philosophy Behind Motorola's MC68000

Part 1: A 16-bit processor with multiple 32-bit registers.

Thomas W. Starnes
Motorola Inc., Microprocessor Division
3501 Ed Bluestein Blvd.
Austin, TX 78721

In the mid 1970s at Motorola, a new idea was taking shape. As more and more demands were being made on the MC6800 family of microprocessors, the push was on toward developing greater programmability of a 16-bit microprocessor. A project to develop the MC68000, known as Motorola's Advanced Computer System on Silicon (MACSS), was started.

The project team began with the freedom to design this entirely new product to best fit the needs of the microprocessor marketplace. Developers at Motorola explored many possibilities and made many difficult decisions. The result can be seen in the MC68000, viewed by most industry experts as the most powerful, yet easy to program, microprocessor available. In this first of four articles, I will discuss many of the philosophies behind the design choices that were made on the MC68000.

Many criteria can qualify a processor as an 8-, 16-, or 32-bit device. A manufacturer might base its label on the width of the data bus, address bus, data sizes, internal data paths, arithmetic and logic unit (ALU), and/or fundamental operation code (op code). Generally, the data-bus size has determined the processor size, though perhaps the best choice would be based on the size of the op code. I'll talk a bit about these features and then show how the MC68000 is both a 16- and 32-bit microprocessor.

Shaping a Design

Designers must make hundreds of decisions to shape the architecture of a new microprocessor. The needs of the users of the new product must be considered as the most important factors. After all, the users are the ones who really need a functional product, and if they are not happy with the features or performance, they will keep looking for a better alternative.

Unfortunately, it may be impossible to meet all of the needs of the users due to certain design limitations. The design must be inexpensive enough to produce in mass quantity. Also, current technology will permit only certain types and numbers of circuits to be manufactured on a silicon chip. These are the foremost factors that dictate the upper limits of the capabilities of a microprocessor.

In planning the new 16-bit MACSS, designers had to make a decision concerning the general architecture first. What should it look like? A great deal of software written for the MC6800 family already existed. A processor that provides enhancements over an older processor, yet can run all of the programs for the older processor, has a real asset: it can capitalize on the existing software base. This may attract users by ensuring that they won't have to rewrite at least some of their programs.

Unfortunately, architectures, such as the early 8-bit microprocessors, were rather crude. Because they were designed to replace logic circuits, not enough thought was put into the software aspect of the parts. Their instruction set was oriented toward hardware. The designers did not consider carefully the future of these products, their expandability and compatibility. To try to design a microprocessor to be compatible with the older 8-bit parts was limiting.

Designers at Motorola decided that the new MACSS should be the fastest, most flexible processor available. They would design it for programmers, to make their job easier, by providing functions in a way that most programmers could best use them.

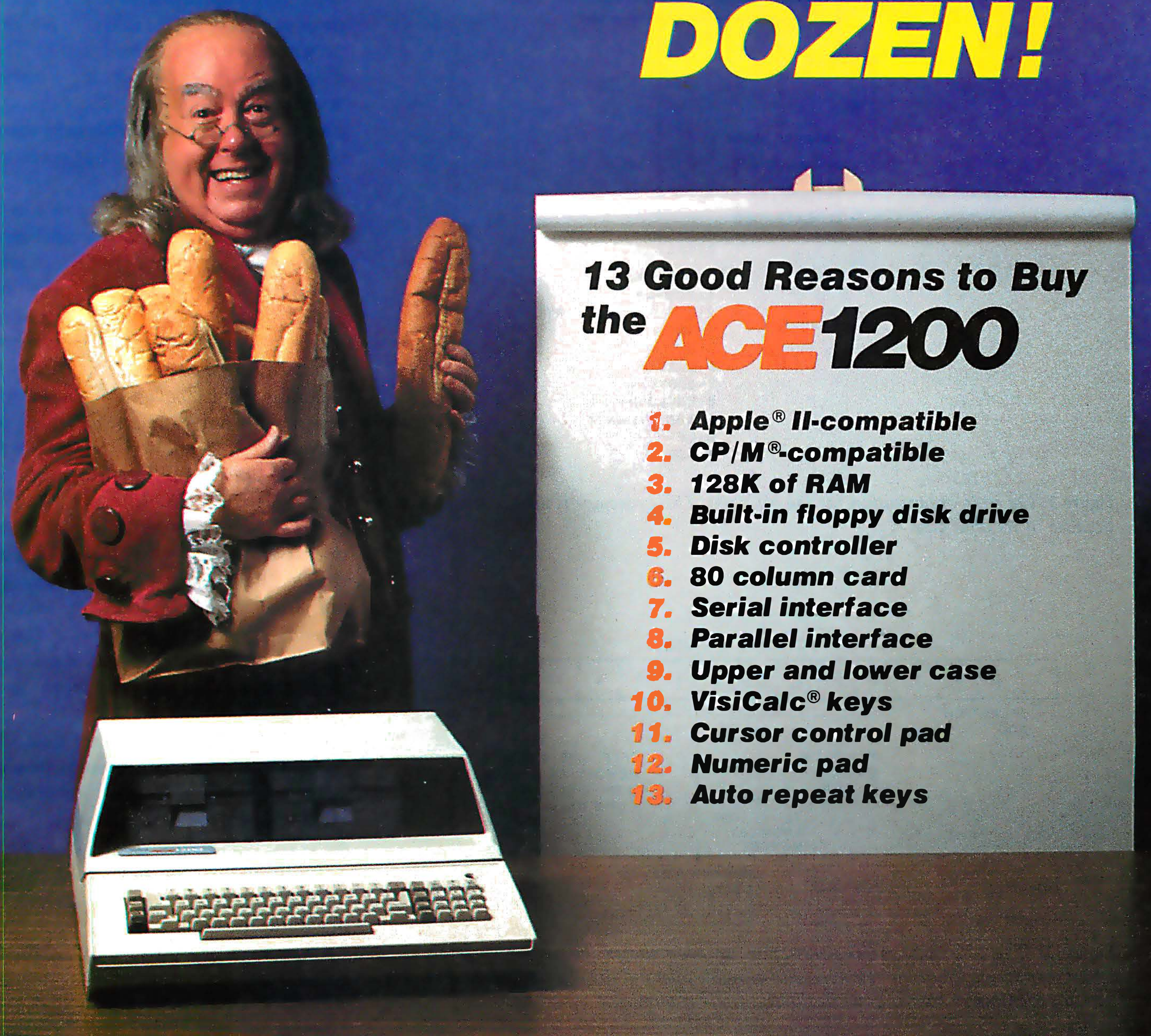
Early on, it appeared that to have a really powerful new generation of microprocessors, a totally new

About the Author

Thomas Starnes is an electrical engineer who has spent the last five years helping to plan the direction of the MC68000 family of processor products for Motorola.

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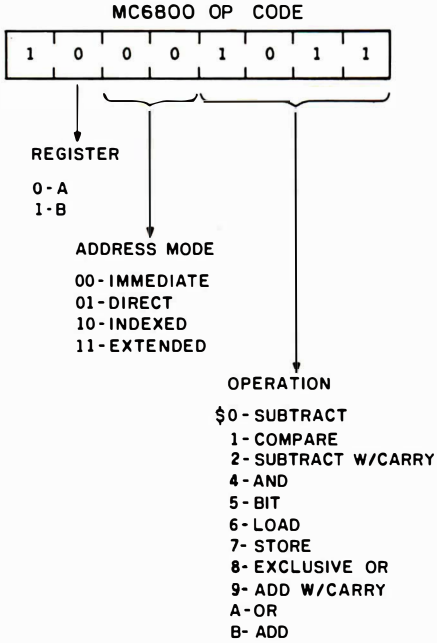


Figure 1: *Op code organization for the MC6800. This processor is limited in its abilities because of its 8-bit size.*

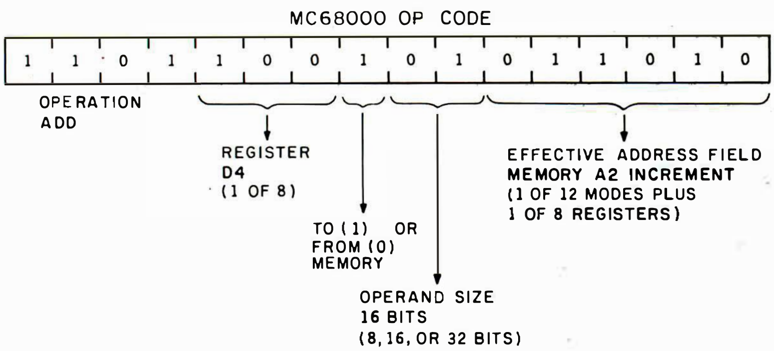


Figure 2: *The MC68000 ADD instruction op code shows the power available with 16-bit operations. Multiple registers with variable operand sizes and a large address field give a programmer tremendous flexibility in programming.*

architecture should be used and that earlier designs should be considered as examples rather than as models. This gave the MC68000 designers the freedom to introduce completely new concepts into microprocessors and to optimize the functionality of the new chip.

The planners decided there was one area in which ties to the 8-bit product family would be advantageous without exception. That area was in peripherals. Motorola decided that this new 16-bit microprocessor would directly interface to the 8-bit collection of MC6800 peripherals. Because so many input/output (I/O) operations are 8-bit oriented, it seemed logical to retain this compatibility even though the 8-bit microprocessor interface would naturally be about half as fast as a comparable 16-bit. Compatability with 8-bit MC6800 peripherals had the added benefit of immediately ensuring support of the new microprocessor with a complete family of peripheral chips, rather than requiring a wait of perhaps years for 16-bit versions to become available.

Expanded Capabilities

A properly designed 16-bit microprocessor has many advantages over the most sophisticated 8-bit microprocessor, especially to the programmer (see figures 1 and 2). The 8 bits of op code for the smaller processor provide only 256 different instruction variations. This may seem to be a lot at first glance, but consider the following.

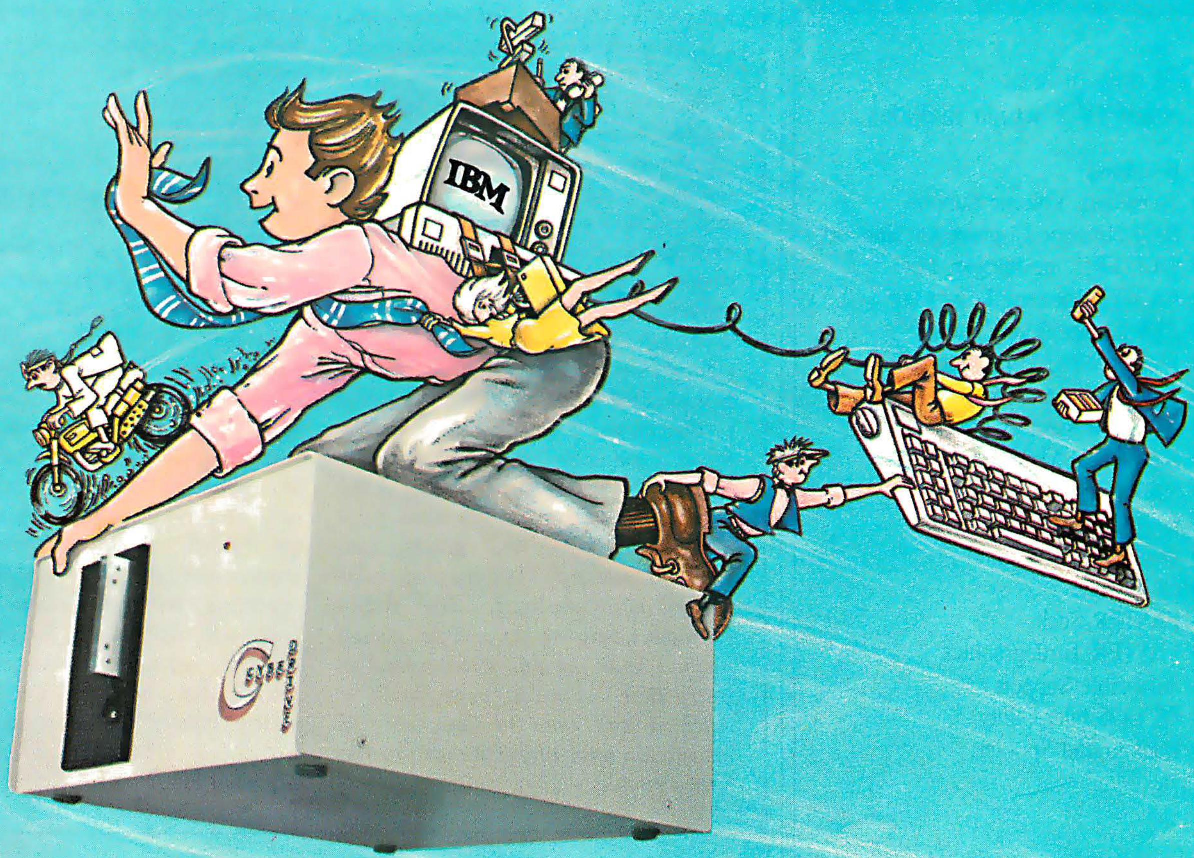
If the microprocessor has two registers from which to move and manipulate data, those two registers require 1 bit for encoding the op code. If four different addressing modes are offered for accessing memory data, these require 2 more bits for encoding. This leaves the microprocessor with only 5 bits with which to encode the operation to be performed. Only 32 different operations can be performed.

Now admittedly this is plenty of operations for most applications, but realize that only two data registers and four memory-addressing modes are not very many to someone doing serious programming. Registers are there for fast data manipulation, and constantly swapping the contents of too few registers is not very fast. A more powerful microprocessor would have many registers, and they would all have to be accessible by the different operations.

Additionally, the more addressing modes you have for accessing memory data, the more efficiently you can get values in memory. Obviously, 8 bits of op code cannot give the microprocessor both the variety and the number of operations that a good 16-bit microprocessor can. With 64,000 different instructions possible in a 16-bit op code, you can perform far more complex operations.

This, then, is the real advantage of 16-bit over 8-bit microprocessors to the programmer. A 16-bit microprocessor will have twice the data-bus width of the 8-bit version. This wider bus allows twice as much information to go in and out of the processor in the same amount of time. This can, with proper internal design, almost double the rate at which operations take place over the rate of a similar 8-bit machine. Sixteen-bit micropro-

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MC68010

Motorola has recently developed an improved version of the MC68000: the MC68010. It is completely compatible with object codes of earlier versions of the 68000 and has added virtual memory support and improved loop instruction execution.

By using virtual memory techniques, the 68010 can appear to access up to 16 megabytes of memory when considerably less physical memory is available to a user. The physical memory can be accessed by the microprocessor while a much larger "virtual" memory is maintained as an image on a secondary storage device such as a floppy disk. When the microprocessor is instructed to access a location in the virtual memory that is not within the physical memory (referred to as a page fault*), the access is suspended while the location and data are retrieved from the floppy disk and placed into physical memory. Then the suspended access is completed. The 68010 provides hardware support for virtual memory with the ability to suspend an instruction when a page fault is detected and then to complete the instruction after physical memory has been updated.*

The MC68010 uses instruction continuation rather than instruction restart to support virtual memory. When a page fault occurs, the microprocessor stores its internal state on the supervisor stack. When the page fault has been repaired, the previous internal state is reloaded into the microprocessor, and it continues with the suspended instruction. Instruction continuation has the additional advantage of handling hardware support for virtual I/O devices.

As mentioned in the body of this article, the 68000 uses a prefetch queue to improve the speed of instruction execution. The 68010 goes one step further by making the prefetch queue more intelligent. Detection of a three-word looping instruction will put the microprocessor into a special mode. In this loop mode, the microprocessor will need only to make data transfers on the bus, because it latches up the queue and executes the instruction repeatedly out of the queue. Once the termination condition for the loop is reached, normal operation of the prefetch queue is resumed. This operation is invisible to the programmer and provides efficient execution of program loops.

cessors should give the programmer far greater flexibility in coding and perform similar operations in less than half the time of an 8-bit microprocessor.

Memory Accessing

Users of the 8-bit microprocessors originally had difficulty imagining what kind of programs could fill up 64K bytes of memory. Many systems had no more than 8K bytes of ROM (read-only memory) and RAM (random-access read/write memory). But as time went on and the general software base grew, systems with up to 64K bytes of memory became more prevalent. Either code had to become more efficient or ways of fitting more than 64K bytes of memory in a system had to be developed. Sixteen-bit microprocessors could make code more efficient.

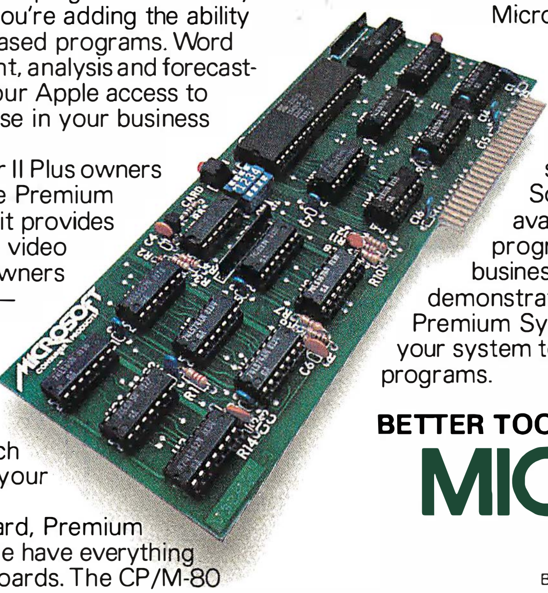
In planning MACSS, designers foresaw that the 16-bit, 64K-byte addressing range of popular 8-bit microprocessors would be quickly outgrown by the newly proposed microprocessor. Each additional bit of address could double the addressing range of the processor.

Look at the techniques of expanding beyond a 16-bit addressing range and analyze the design trade-offs (see figure 3). You could extend the addressing range of early computers and minicomputers simply by appending some additional bits to the most significant of the 16 address bits. These additional bits were usually stored in an additional register, the page register. This method is called *paging*, because you work out of one page at a time. The page is set manually, and the lower 16-bits of address are included in the instruction stream or registers.

Paging has the advantage of being quite simple to implement in the processor. No real circuit change is needed over the straightforward 16-bit addressing, because all the



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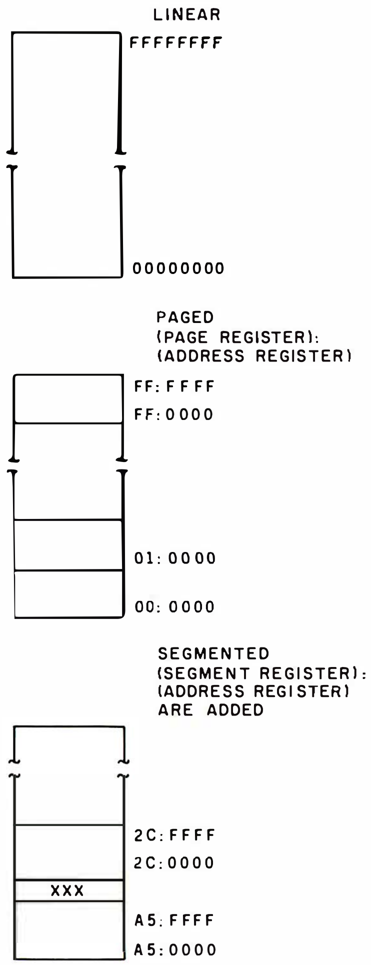


Figure 3: *Three methods of addressing memory. The Linear method arranges a contiguous memory area. The Paged method organizes memory into blocks or pages of a prescribed length. The Segmented method gives each user or program a specific area in memory. Both the Paged and the Segmented method give the programmer access to only a small portion of memory.*

expansion is done simply by appending bits to the core. It also has the advantage of having fairly dense code, because only 16 bits of address are carried around in the instructions.

However, there are many disadvantages to paging. The programmer is limited to accessing only the particular page of memory that happens to be set in the page register. To be assured that the right page is being used requires a check to see what is currently in the page register, possibly saving that page number, and loading the register with the desired page number. This takes time and requires both additional thought by the programmer and additional

Text continued on page 80

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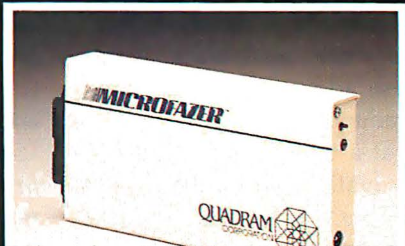
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code in the software. This additional code typically takes up the room saved by carrying around only 16 bits of address.

One way to get around the single-page limitation of paging is to provide many page registers. Other characteristics that determine which register will be active on a particular bus cycle include instruction fetch, data read/write, and stack access. While these additional registers give the programmer access to more than one page at a time, there is still only one page available for each type of access.

Some extensions to paging came out to compensate for some of the losses experienced in paging. *Segmentation*, for example, follows the same general principles of pagination. The key difference in segmentation is that the page number becomes a segment number and the segment number is essentially added to the core 16-bit address. This allows some relocation of the core address but still forces the programmer to check that the desired segment is loaded, and limits the range of any segment to only 64K bytes of memory.

To a programmer, the simplest address technique is a direct addressing of any memory location. This would be without regard for whether the wanted data is near recently accessed data or whether it is miles away. The programmer wants a linear view of data, that is, the ability to specify a very simple, albeit long, address that will access any data.

Now, beyond the processor's memory-addressing method, memory management is sometimes used. With it more sophisticated systems dynamically relocate or control the various blocks of memory. This is done for protection purposes in larger systems. The advantage is that you can protect one user's work space from the devastating effects of another user's poor programs running amuck. To this end, a separate memory management unit (MMU), in conjunction with the operating system, performs some addition to or translation of an address. This technique may sound similar to paging and segmenting memory, but this is done to serve a completely different purpose, and in a different way. The application program writer never sees this memory management and writes code as though the entire memory were available.

To expand the memory space on the MACSS, the best option, though not the easiest to implement on the chip, is a linear address space. This space is not broken up by paging, segmentation, or banking schemes. It is a very simple addressing technique, requiring the least effort by the programmer, while still allowing more advanced operations such as memory management.

A *linear address* is simply a straightforward 32-bit, for example, address. The address space is not broken up into blocks; and it is contiguous. Accessing such an address merely requires the expression of the 32-bits in the instruction or using a single address register. For convenience, if the upper 16 bits of the address are either all 0s

or all 1s, then a shorter, 16-bit form of the address can be sign-extended to automatically provide the correct address. This is the way the MC68000 accesses memory and I/O.

How big an address space should a 16-bit microprocessor address? The natural address sizes greater than 16 bits are 24 and 32 bits, which are 3 and 4 bytes long, respectively. For a 16-bit microprocessor, the odd number of bytes becomes slightly unwieldy. Looking a little further into the future, it seemed that even the 16 megabytes of a 24-bit address might not meet the needs of large systems.

While 32 bits of address, reaching 4 gigabytes of memory, seems tremendous, once the need for more than 16 bits is established, 32 bits is the next most convenient size. It takes exactly two 16-bit bus transfers to move an address into the processor, and once the second transfer is needed, as it would be even for an 18-bit address, it is just as well to use the whole 16 bits brought in. Thus, engineers selected a virtual-memory address space of 32 bits for the MC68000.

Now, from a practical packaging standpoint, 32 address signal lines are quite a few. The placement of integrated circuits (ICs) in dual inline packages (DIPs) with greater than 40 leads was rare before 1980. With only a few systems in the early '80s requiring more than 16 megabytes of memory, it seemed a reasonable trade-off to bring only the 24 least significant address bits to the outside world. That way fewer pins would be required, and MACSS could fit within a 64-pin DIP. Still, all 32 bits of address are maintained within the processor, and there are simple means of determining the upper 8 bits' values.

Multiple Registers

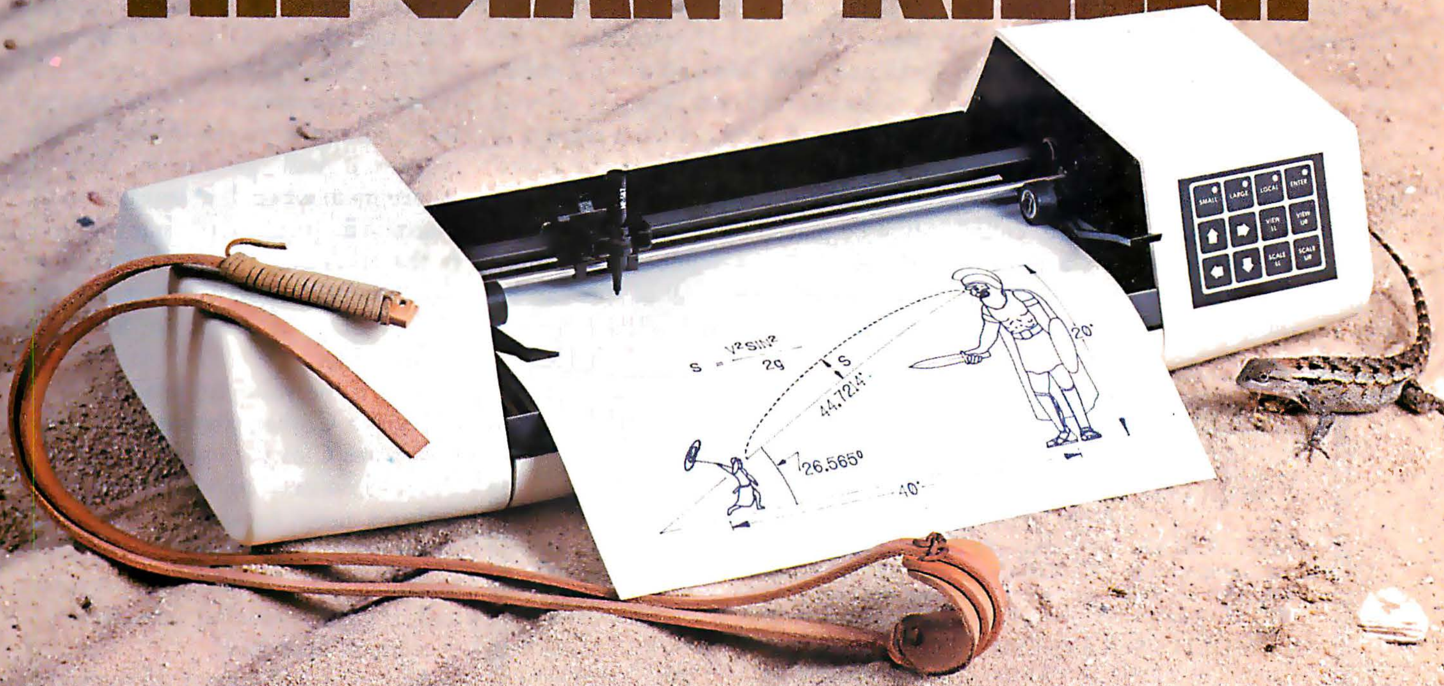
With the size of the memory address space determined, it was easier to settle on the register scheme of the new processor. The size and the number of registers had to be decided.

Designers originally envisioned onboard registers for a processor because operating on memory data requires a time-consuming transfer across the external bus. It just happens that in programming most data is operated on a number of times in succession before a result is obtained. Often many combinations with many different data pieces are used. The merging of these two observations leads to onboard or on-chip registers for fast manipulation of frequently used data.

It seems that from the day registers were brought into the processor, programmers have wanted more registers for their use. The goal, then, when designing processors, is to provide as many registers as possible for the programmer. In the MC6800, only two registers (A and B) were available for data manipulation, and one index register (X) to point to non-stack data. These few registers are being loaded and saved almost as often as the data within them is manipulated.

The loading and saving of registers is usually wasted time. The amount of time spent bringing data into on-chip registers for fast manipulation

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depends upon the exact use of that data. However, the more registers available, the more likely it is that a register will not have to be saved just so that some other data can be operated on in that register.

The design of the internal execution of instructions through a microprocessor will determine many things about the suitability of the chip for programming. Instructions may operate either on what are called *dedicated registers* or on a *general register set*. Each of these methods has advantages and disadvantages.

In a microprocessor that uses dedicated registers, an instruction includes the address of the data to be worked on in specific registers. These registers are inherent in the instruction. The ADD instruction, for example, will add only from a memory location to, say, register A—not to register B, and not from register A to memory. If the value to be added to is not already in register A, it must first be placed there. Before it can be placed there, a number in A may have to be saved. All of this can be quite troublesome. This is not very different from the situation in which there simply are not enough registers.

Contrast this with the example of a processor that uses true general-purpose registers. In a general-register machine, the ADD instruction may add data from memory to any of the internal registers. The instruction must contain information on which register it will operate on. This is determined when the instruction is assembled. If there were four registers in the processor, the ADD operation could be performed in register A, B, C, or D, as selected by the programmer.

Now if the value to be added to is in register C, the programmer simply designates C as the operand register. There is no need to shuffle registers and no need to save any register contents. The general-register machine, then, is easier to program and typically requires less time to execute an operation.

As it always happens, this ease of programming does not come free. You will see later that allowing a selection of registers requires bits in the op code for encoding and, therefore, more bits of the op code. Also, it is typically more difficult for the microprocessor designer to implement the circuitry that incorporates various registers because it takes time to determine which register is to be used and to activate that register. Streamlining internal operations so that this time is not detectable requires quite a bit of planning.

So while fewer registers or dedicated registers may be easier for the microprocessor designer to implement, they make programming the new chip more cumbersome and less flexible. But the extra time, effort, and expense of implementing general-register principles pays off by easing the programming of these devices.

Therefore, the MC68000 was designed with general-purpose registers. Any instruction may select any register for use as a source or destination operand or as a pointer in any allowable addressing mode. This tremendous flexibility gives programmers the ultimate in data and pointer placement.

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registers indicates they usually have one of two purposes: they may retain data for manipulation, or they may contain an address that points to a memory location. The use of a register for each of these purposes is quite different.

When data is moved into or out of a register or is manipulated within the register, all types of conditional information from the operation are important. Thus, you typically would like all condition codes to be properly set after a data operation. This way these condition codes may be used to branch or with other data operations.

On the other hand, an address might be placed in or taken from a register, or modified by incrementing or decrementing. Rarely is it important whether a carry comes out of the ALU or whether the result is negative (i.e., has a 1 in the most significant bit). In fact, a programmer would prefer manipulation of an address to have no effect on the condition codes. Often in the middle of a complex data operation, you must bring in a new address or increment an address. To have this operation modify the condition codes most of the time will foul up the data operation in progress, and so is undesirable.

Therefore, two generic register types emerge: a data register (D0 through D7) and an address register (A0 through A7). The MC68000 has both types. In a data register, any operation will affect the condition codes of the microprocessor as is appropriate for the operation and the data used. However, in an address-register operation, condition codes will not be changed, but the codes from previous data operations will be retained. This way you can have address and index pointer changes made, without affecting the accuracy of the results, in the middle of a complex data operation that requires many instructions and transfers from memory.

What size and how many of each type of register should be included in the microprocessor? The more registers there are, the better it is for the programmer. Unfortunately, the more register and control circuits in the chip, the more expensive it is. A good balance must be attained.

Two registers are too few, four are nice, but it is difficult to imagine even a complex routine requiring more than eight different memory pointers. The encoding of eight registers requires an even three bits. Because it seemed that eight was a good upper bound, the MC68000 has eight address registers and also eight data registers.

With 16 registers available, divided half and half for data and address, almost any sizable routine will never require the temporary storing of a value in a register just so that the register can be used for something else. And, within the routine, manipulations of memory pointers in address registers will not interfere with an ongoing data calculation,

because of the distinction of how the condition codes work for the different register types. It is easy to see how the MC68000 is easier to program.

Earlier I explained that MACSS would handle all of its addresses as 32-bit quantities. Anyone who has ever programmed 8-bit microprocessors, which have 8-bit accumulators and 16-bit index registers, has seen the difficulty with the two different sizes. Once programmers figure out how to put the 16-bit value in both 8-bit accumulators, things get tougher when they try to get arithmetic carries from the lower half to the upper half of the value.

A little of this experience led the MC68000 designers to decide that using data that is the same size as the address register could make some software design significantly easier. In order to handle a linear 32-bit virtual-address space, the MC68000 needed to have 32-bit address registers. How would 32-bit data registers fit into a 16-bit microprocessor?

You would expect a 16-bit microprocessor to process 8- and 16-bit data, but does it make sense for it to also process 32-bit data? Obviously, the addresses will have to be handled in that size. Designers recognized that in 8-bit microprocessors the ability to handle 16-bit data came in quite handy for more advanced applications. The 8-bit processors soon had to be upgraded to handle 16-bit operands, and users of 16-bit minicomputers needed 32-bit operations.

Once a few 32-bit operations become necessary in a microprocessor, you need a whole array of operations. If a multiplication operation generates a 32-bit result, in order to do anything with that result, other 32-bit operations are needed. For consistency, again, Motorola decided that the data registers would be 32 bits wide and operations on all 32 bits could take place with a single instruction.

Three Arithmetic Units

The exact manner of processing data and addresses through the MC68000 came about later, with careful analysis of the internal architecture and the need for address and data in the sequence of instructions. The chip ended up with three separate arithmetic units, which could work in parallel. I'll describe their purpose to give some insight into how the machine works.

The MC68000 has a 16-bit-wide ALU that essentially performs all data calculations and provides single-pass evaluation of the 16-bit data, for which the MC68000 is primarily designed. There are also two other internal arithmetic units. Both are 16 bits wide and are generally used in conjunction with each other to perform the various address calculations associated with operand effective addresses. This makes sense because all addresses are 32 bits wide. An effective address (EA) is the calculated result based on a selected addressing mode of the processor. In the MC6800, for instance, if an "index-register-plus-offset" address mode were used, the EA would be the result of adding the contents of X with the given offset. Because EA evaluation takes time and can be a significant portion of the instruction, it is important to perform this quickly.

At one time, then, one 32-bit address and one 16-bit data calcula-

tion can take place within the MC68000. This speeds instruction execution time considerably by processing addresses and data in parallel. The MC68000 also operates on 32-bit data. This is usually done by taking two passes of 16-bit data, one for the lower word and one for the upper word. This is reflected in the execution time of many 16- and 32-bit instructions.

Prefetch Queue

Another way designers made the MACSS faster was to include what is called a *prefetch queue*. This prefetch queue is more intelligent than other microprocessor queues; its control varies according to the instruction stream contents.

The prefetch queue is a very effective means of increasing microprocessor performance; it attempts to have as much instruction information as possible available before a particular instruction begins execution. The microprocessor uses an otherwise idle data bus to prefetch from the instruction stream. This keeps the bus active more of the time, increasing performance because processing of instructions is often limited by the time it takes to get all the relevant information into the processor.

The part of memory from which instructions are fetched, the program space, contains op codes and addressing information. The prefetch queue can contain enough information to execute one instruction, decode the next instruction, and fetch the following instruction from memory—all at the same time.

Exactly what is in the queue is very dependent upon the exact instruction sequences. The queue is intelligent enough to stay fairly full without being too wasteful.

For instance, when a conditional branching instruction is detected, the prefetch is ready to either branch or not by the time a decision is made. The queue tries to fetch both the op code following the branch instruction and the op code at the calculated branch location. Then, when the condition codes are compared and a decision is made whether to branch, the processor can begin immediate decoding of either instruction. The other unnecessary op code is ignored.

You can use the prefetch queue in many other special ways as well. One example is in speeding up the repetitious Move Multiple Registers instruction, where it is used to accelerate successive data transfers. The prefetch queue allows many frequently used instructions to execute in exactly the time it takes to fetch the op code (actually, the time to prefetch the next op code).

Microcoding

One other significant implementation feature from the MACSS project emerged from the choice between a *random logic design* versus a *microcoded design*. Both techniques have advantages and disadvantages. Earlier microprocessors were largely of random logic design. Advanced techniques of very large scale integration (VLSI) and the increasing complexity of the chips have made microcoding more attractive.

Random logic design of a microprocessor or other logic device is the building of the device from discrete components—gates, buffers, and transistors. This limits the components to those that are essential. There are no unused gates, duplicated circuits, or clever uses of otherwise unused components. The design is usually packed as tightly as possible and is quite fast.

The difficulty is that, as the design becomes more and more complex, as VLSI has, the planning and layout of the components and signal traces become exponentially more difficult and often impossibly so. This means that it takes exorbitant amounts of time to design the circuits.

Another problem with the use of random logic in very complex circuits occurs in modeling and testing. Before such circuits are finally placed in silicon, they must be modeled and simulated on computers because of the great difficulty in running down

bugs once the chip is in silicon compared to debugging a wire-wrap board. The entire circuit must be modeled all at once to ensure that one combination of signals affects only the expected section of the device.

Similarly, once the circuit is in silicon, the pass/fail testing of the components in a random logic chip is quite difficult. You typically have only a few lines to send sequences of patterns through for testing. Because a particular section of the circuit may be exercised only by a very few given inputs, a normal test may not detect a stuck gate or other error caused by some strange combination of inputs.

On the other hand, in much the same way that microprocessors made designing systems with medium-scale integration/large-scale integration (MSI/LSI) easier, microprogramming has come to ease the complications in the design of microprocessors. Microprogramming is to a microprocessor what a microprocessor is to a logic design of a system. A microprocessor has central components that can be considered black boxes with inputs and outputs. For each given operation (instruction, interrupt condition, etc.), the microprocessor can route certain information to these black boxes as inputs, and the outputs can be routed to other components. The control of this routing is performed by a microcontroller or microsequencer.

Similar to a microprocessor, the microsequencer directs the flow of data through the various components (ALU, registers, condition flags, shifters, buses, etc.) according to microprogrammed instructions. Each instruction has its own microroutine, or sequence of microwords, which routes the associated data to the proper component in the proper order. Conditions and branches may redirect the microroutines.

Microcoding a complex circuit simplifies design mostly because it makes the circuit modular. It takes a controller, a block of microprogram, and the components through which data is to flow. Each of these elements may be modeled, built, and tested with individual inputs and outputs. Microcoding is a big step toward simplifying the design process because it breaks up the design into manageable blocks, thereby easing the testing of the finished product.

Another advantage of microcoding is that it allows tremendous flexibility in the exact operation of the circuit. Its microwords allow more combinations of the inputs through the components than most random logic would allow. Microcoding's programmability makes it especially attractive to silicon designers because random logic in silicon is not easily changed.

Last-Minute Changes Possible

You can change the microROM of the microcoded device right up to the minute before the masks for the device are processed. To change a small facet of an operation may mean altering a few bits in the microROM, but this changes only whether or not there is a gate on the bit's transistor—a simple alteration. Similarly, after the silicon is cast, should a change be necessary, it will likely be just a microcode change, which would be much easier than random logic modification in silicon.

The disadvantage of a microcoded circuit lies primarily in its generality. Because it is made up of modules and is programmed, the microcoded circuit is more wasteful of transistors and therefore makes a larger circuit. This may add up to 20 percent more board space or chip area than a tight random logic design. But microcoding has advantages that make up for this disadvantage, making it the design choice for modern VLSI circuits.

There are two types of microprogramming, horizontal and vertical (see figure 4). *Horizontal microcoding* is the more direct form. It is unencoded, so that, for instance, 1 bit in each microword would enable each register. For 16 registers, then, 16 bits of microcode must be dedicated. Horizontal microwords tend to be quite long, and because the size of the microcode directly affects chip size, they can quickly increase chip cost.



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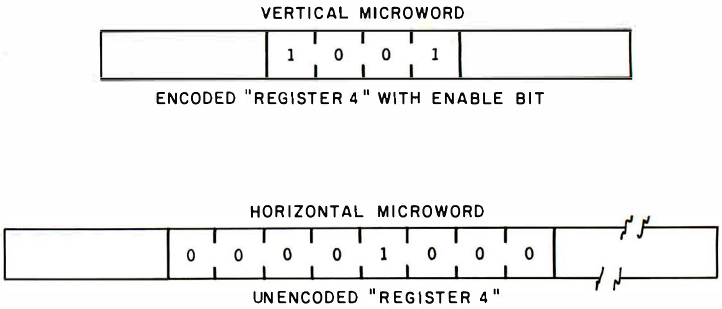


Figure 4: *Comparison of horizontal and vertical microcode patterns.*

A denser but slower form of microcoding is *vertical microcoding*. Here, control functions are encoded, so that only 4 bits of microcode are required to select one of 16 registers. While it needs a much shorter microword, vertical microprogramming is potentially slower than horizontal microprogramming. Vertical microprogramming will take at least one level of logic gates to decode the encoded signals. This level of gates may just throw the total gate propagation delay over the threshold of the clock pickets, forcing an additional clock cycle into the instruction.

In the MACSS project, the MC68000 was selected to be microcoded. In retrospect this was a very wise decision. The first silicon prototype worked well enough so that the major circuits in the device could be tested, and subsequent "fixes" were often just microcode corrections. The instruction set was not firm until just before the masks went to wafer fabrication, allowing some late decisions to be made to improve the performance of the chip.

A combination of horizontal and vertical microcoding was used on the MC68000 to gain the optimum advantages of both. Essentially, a microcode and a nanocode were developed. The microcode is a series of pointers into assorted microsubroutines in the nanocode. The nanocode performs the actual routing and selecting of registers and functions, and directs results. This combination is quite efficient because a great deal of code can share many common routines and yet retain the individuality required of different instructions.

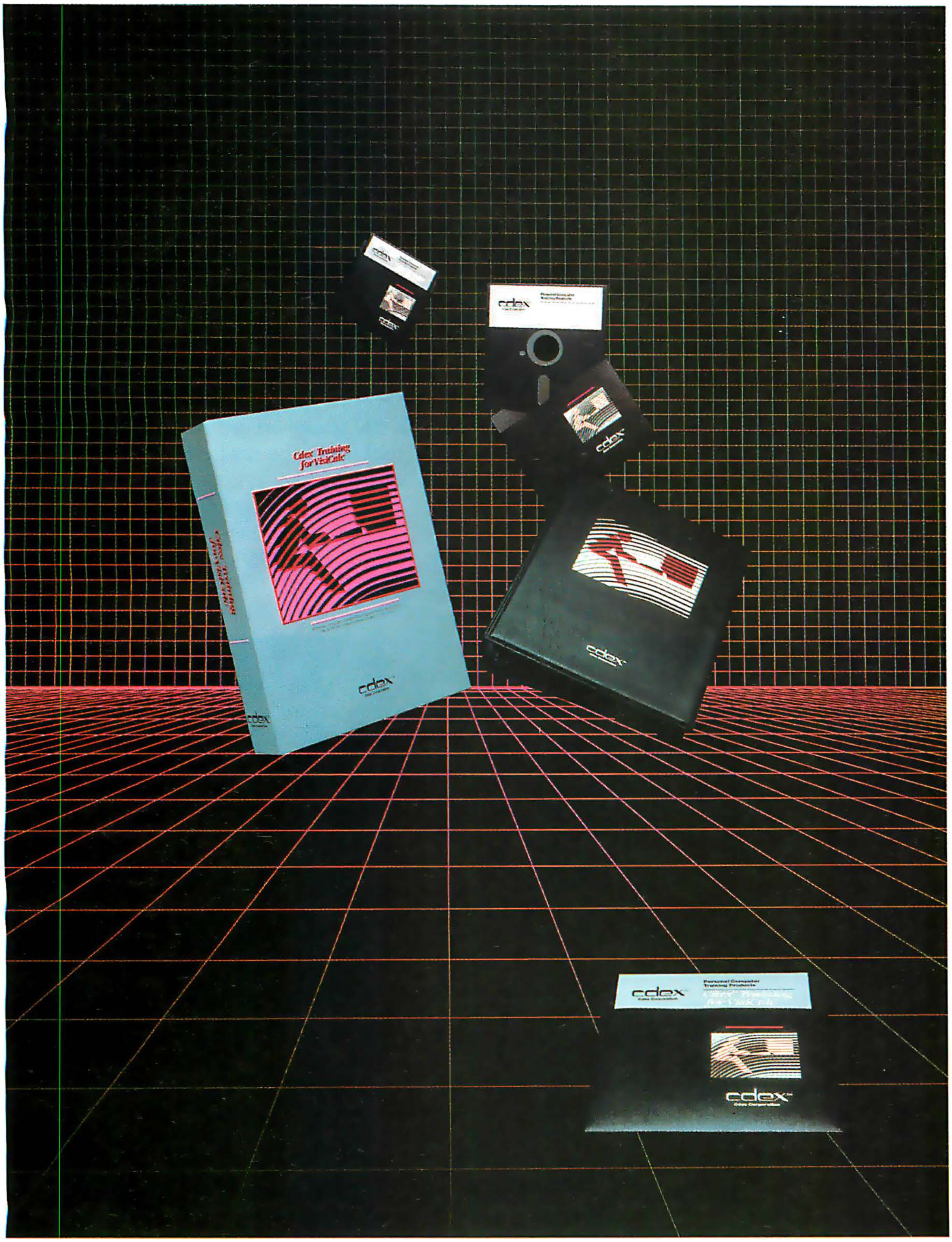
Decoding of an instruction's op code generates starting addresses in the microcode for the type of operation and the addressing mode. Completion of an instruction enables interrupts to be accepted or allows access to the prefetch queue for the next op code. The prefetch queue actually keeps bus use at 85 to 95 percent, i.e., the bus is idle only 5 to 15 percent of the time!

Conclusion

Let's look back now at the MC68000 and see what parts of it might qualify it as a 16-bit device. The internal data ALU is 16 bits. It processes 32-bit addresses, though only 24 bits are brought off chip. The op code that tells the processor what operation to perform is 16 bits wide. The data bus is 16 bits wide. The microprocessor will operate on either 8, 16, or 32 bits of data automatically. There are 16 general-purpose 32-bit-wide registers in the chip.

The MC68000 is generally considered a 16-bit microprocessor, though it uses 32-bit addresses and contains 32-bit registers. It also can operate on 32 bits of data as easily as 8 and 16. Many users of the MC68000 consider it a 32-bit just as much as a 16-bit processor. Whatever you consider it there is no doubt that the MC68000 is indeed a powerful microprocessor. In coming articles, I will discuss in more detail exactly what operations are available in the MC68000 and will illustrate examples of MC68000 code.■

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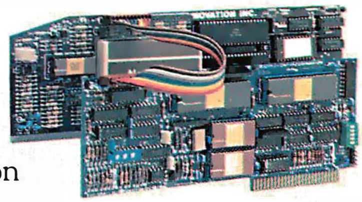
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The CRT 9007 Video Processor and Controller

Explore the heart of a smart terminal.

Brian Cayton and Mort Herman
Standard Microsystems Corp.
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The CRT 9007 VPAC (video processor and controller) is a powerful new "next-generation" CRT (cathode-ray tube) controller that features advanced memory-addressing techniques and flexible video-timing parameters.

To better understand the virtues of the VPAC, we should first review the function of the basic CRT controller. Characters are "painted" by the scan of a modulated electron beam across the screen phosphors. All CRT displays demand continual readdressing of a video memory to refresh the screen before the characters fade. This screen addressing must be synchronized to the raster scan (via the horizontal and vertical sync pulses) to ensure that the characters are in the same screen position every *frame* or refresh period. In the most elementary sense, a CRT controller is nothing more than a memory-address generator to refresh and synchronize the video screen.

If a CRT controller is to gain acceptance, users must be able to program its screen parameters and format (i.e., the number of characters per row, the number of rows, the character cell size, sync pulse widths, and so on). Moreover, the controller should offer other characteristics desirable in a display system. These include cursor generation, retrace blank generation, and interlace capability.

The first-generation LSI (large-scale integration) controllers all fit this description. Some of them differ architecturally in the techniques of addressing data and so on, but they all provide much the same function. The first-generation CRT controllers revolutionized the terminal marketplace by reducing the chip count of earlier CRT terminals built with SSI (small-scale integration) and MSI (medium-scale integration) techniques by some 50 to 60 chips. As a result, they substantially reduced both cost and board space and made relatively inexpensive multifeature terminals possible. The CRT controllers also removed much of the black magic associated with CRT display design, bringing the design of CRT displays within the reach of most engineers.

Although the first-generation CRT controller chips were very successful in reducing hardware costs by reducing component counts, they did nothing to improve the actual terminal performance. Over the last few years, however, the terminal marketplace has changed. Computer manufacturers, wanting to enhance their powerful new mini- and microcomputers with powerful new displays, were forced to surround the first-generation CRT controllers with the discrete circuitry needed to provide smooth scrolling and more transparent memory-contention schemes. In addition, they overburdened CRT processors with the software required to provide editing features.

A New Generation

When Standard Microsystems Corporation began on a next-generation CRT controller to replace the first generation CRT 5037 (introduced in 1977), the company decided that a true next-generation CRT controller should not only simplify hardware design decisions but carry out software tasks previously relegated to the system's processor. The designers also felt that the CRT controller should not dictate the hardware architecture of the CRT terminal. The controller should be versatile enough to give the terminal designer maximum freedom in specifying components.

The result was the CRT 9007 VPAC and a family of ancillary circuits. Four LSI circuits resulted from this project: the CRT 9007 VPAC, the CRT 9006 SRB (single-row buffer),

About the Authors
Brian Cayton is the marketing manager (standard products) for Standard Microsystems Corporation. Mort Herman is the product marketing manager (display products) for SMC.





Auxiliary ICs

CRT 9006 single-row buffer: contains RAM, an address counter, and data latches. Two versions are available: CRT 9006-135 (up to 135-column display) and CRT 9006-83 (up to 83-column display). Both versions can be cascaded for longer data rows.

CRT 9212 double-row buffer: essentially two single-row buffers in one package. One buffer fills with character data while the other provides screen refresh. It has separate clocks for reading and writing the buffers to allow for different input and output data rates.

CRT 9021B video attributes controller: controls video attributes (blink, blank, reverse video, underline, and intensity along with double height/double width and programmable cursor) and graphic attributes (wide and thin modes). Contains 28.5-MHz video shift register.

Table 1: *The three auxiliary ICs developed by Standard Microsystems Inc. to support the CRT 9007 VPAC.*

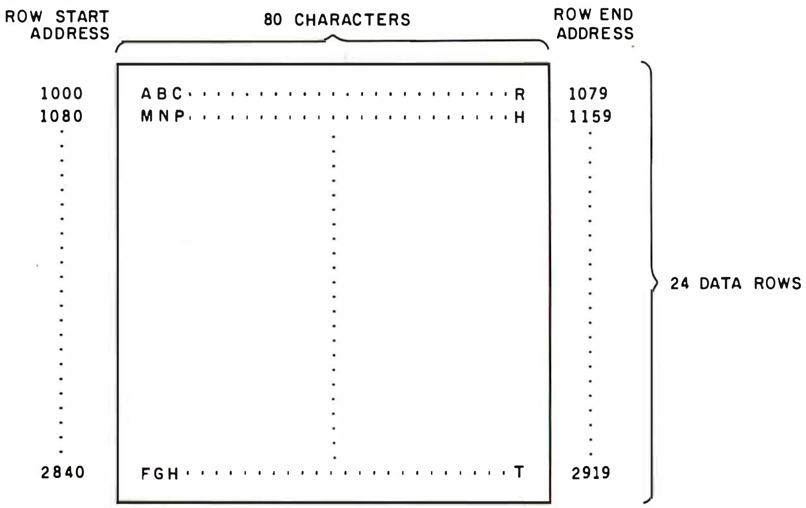


Figure 1: *A typical (80 by 24) display employs sequential memory addressing for its 1920 bytes of video memory.*

the CRT 9212 DRB (double-row buffer), and the CRT 9021B VAC (video attributes controller). See table 1.

VPAC Design

The CRT 9007 contains 30 registers, 12 of which contain the *vital screen parameters,* the data that determines the screen format. The remaining registers provide for cursor control, light-pen operation, and the software features that are unique to the VPAC.

Traditionally, video memory is addressed sequentially. In sequential addressing, the characters on the display screen are located in successive memory locations. As each character is read out for display refresh, an internal video-address counter is incremented by one, to point to the next character to be accessed. For example, an 80-character by 24 data-row display will require 1920 sequentially located bytes that represent all character locations on the screen (see figure 1).

Intelligent terminals must provide on-screen data manipulation through editing functions. Typically, such designs also include display features such as double-height and double-width characters, bidirectional variable-speed smooth scrolling, and multiple-width screens (83 and 135 columns).

With sequential memory addressing, inserting and deleting single characters within a row are relatively trivial examples of data manipulation. However, when whole lines are inserted or deleted, large blocks of data must be moved rapidly to avoid screen flashing, "garbage" displays, or undesirable blanking of the entire screen. A single-line insertion in an 80-column display requires that every succeeding memory byte be moved forward by 80 address locations. On a 24-row display, this can involve moving up to 2K bytes of data. The microprocessor manipulating this data must also be able to service the various interrupts coming from data-communication ports, the keyboard, and possibly even a magnetic-storage medium.

Nonsequential Memory Addressing

To take some of the burden off the microprocessor, the VPAC provides not only sequential memory addressing but two modes of *row-table* oriented nonsequential memory addressing to assume the duties of moving data from the host processor.

The row table, a list of starting addresses for the rows, resides in memory for addressing by the VPAC. Row-table addressing links each data row by pointers, eliminating the need to locate the rows in sequential memory addresses. Instead of manipulating entire data rows, only the pointers need be moved. Two formats for the row-table organization are provided—*contiguous* and *linked list.* In the contiguous format, a start address register in the VPAC points to the first entry of the row table (see figure 2). In the linked-list format, the start address register points to the beginning of the linked list. The first 2 bytes of each data row point to the starting address of the following data row, as shown in figure 3.

To insert a data row using a row table, the VPAC modifies the row table by entering the starting address of the new data into the table. To delete a data row, the VPAC deletes the existing entry in the row table.

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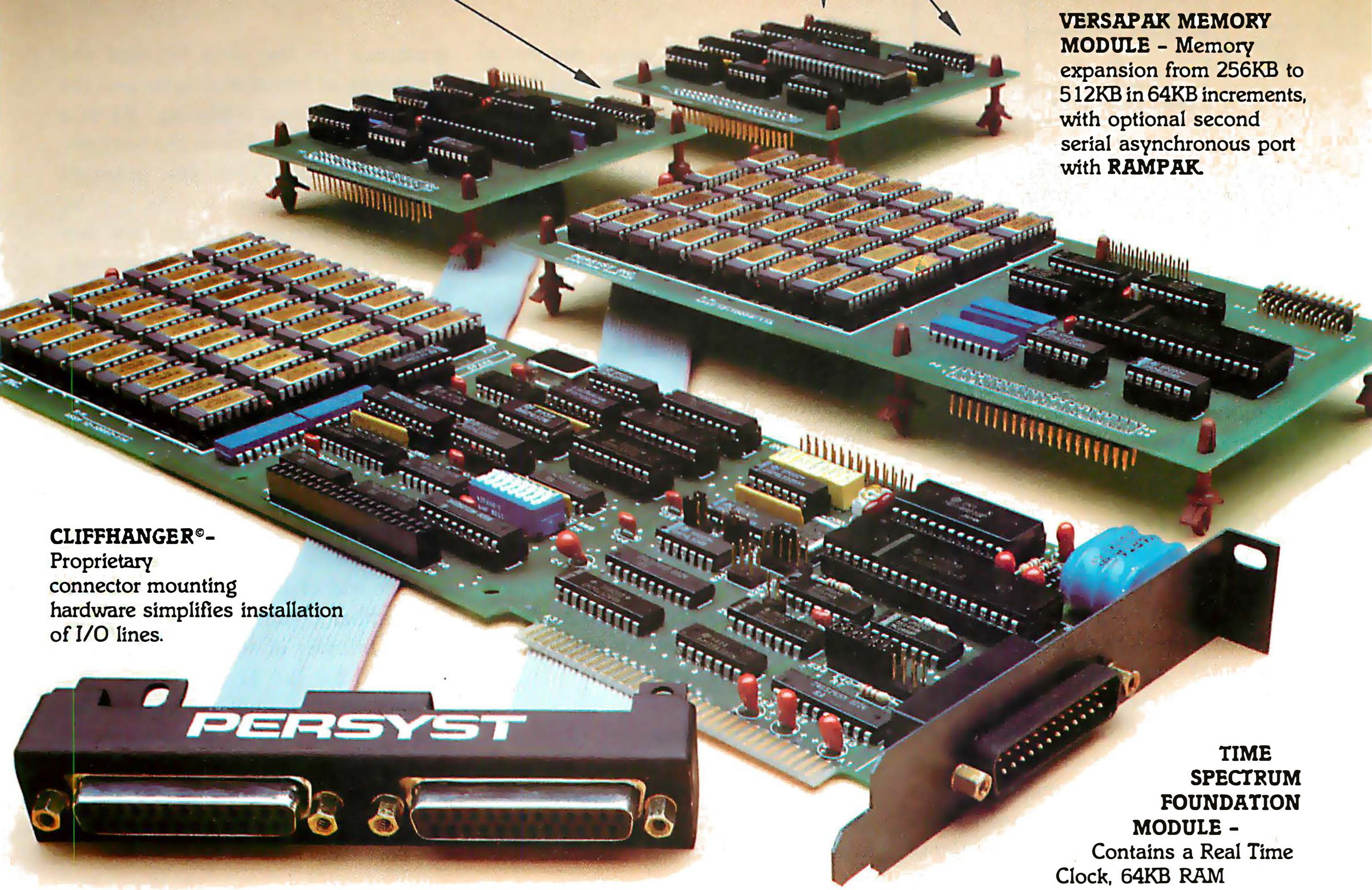
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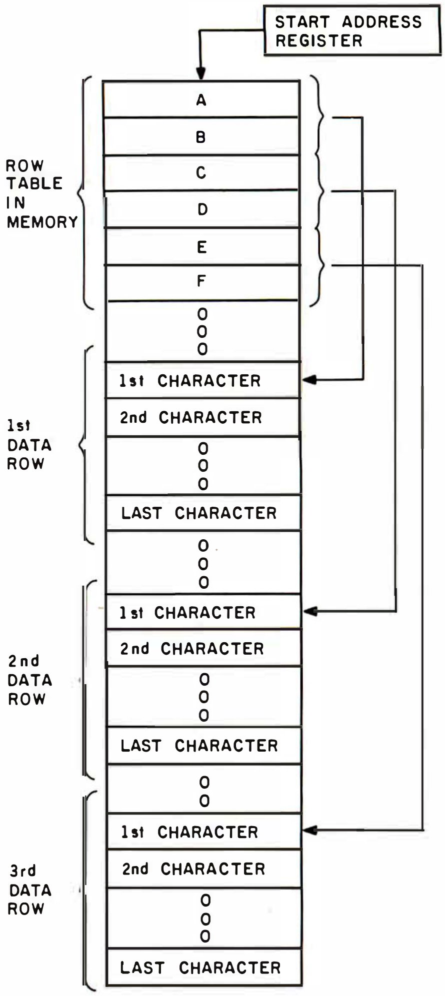


Figure 2: *Contiguous row-table format. Each data row (screen line) is stored contiguously within memory. The start address register points to the first row table.*

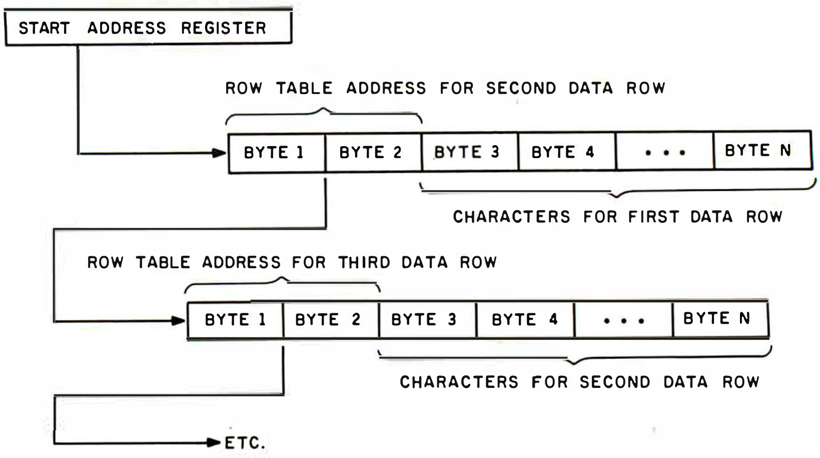


Figure 3: *Linked-list row-table format. The start address register points to the address for the second data row. The first 2 bytes of that data row point to the address of the next data row, and so on.*

Additional Features

Another addressing feature of the VPAC is the provision of *sequential break* and *auxiliary address* registers.

When a break is encountered in the sequential addressing mode, the VPAC begins addressing the memory locations indicated by a starting address stored in one of two auxiliary address registers. This enables you to scroll a portion of the screen while keeping the rest fixed. The position of the sequential breaks is defined in sequential break registers 1 and 2 and programmed with the data-row number that starts the particular break.

You can combine a row-driven screen for the top portion of the display with a sequential screen for the bottom portion of the screen (i.e., split screen) by specifying a row-driven format in the table start register and then using sequential break register 1. If sequential break register 1 is programmed within the displayable screen parameters, the row address for that data row will be overridden and the remainder of the screen will be addressed sequentially, starting at the address specified in auxiliary address register 1.

Combining a row-driven screen with a sequential screen could be useful in some communications applications. A high-priority message to the terminal could be stored sequentially. As more of the message came in, sequential break register 1 would be decremented to allow the message to overlay the row-driven screen one data row at a time. By programming sequential break register 1 outside the display range, the original row-driven screen is restored.

Display Formatting

To allow the terminal designer maximum freedom, nine registers are used to store the horizontal and vertical timing parameters that are output to the monitor.

Horizontal timing is determined by four registers (R0-R3). Both R0 and R1 are 8-bit registers that contain, respectively, the number of character time periods per horizontal period (i.e., 1 scan line) and the number of displayable characters per horizontal period (i.e., the active display time). R2 is a 6-bit register that can be programmed for the time between the beginning of horizontal sync and the end of horizontal blanking. R3 is a 7-bit register that defines the horizontal sync width. When you program these registers, sync widths can be generated narrow enough for so-called *sync monitors* or wide enough for *drive monitors*. The sync pulse can be extended well into the active video portion of the horizontal time or kept within the blank time.

Vertical timing capabilities are as broad as the horizontal, with five registers used to store the vertical timing parameters: R4 defines the vertical sync pulse width, R5 the delay between the leading edge of vertical sync and the end of the vertical blank, R7 the number of data rows per frame, R8 the number of scan lines per data row, and R9 (an 11-bit register) the number of scan lines per frame. An 11-bit register enables the designer to program the VPAC for as many as 2048 scan lines per frame so that it can be used in systems ranging from low-cost terminals to high-resolution word-processing and graphics applications.

Some Hardware Configurations

An intelligent terminal must allow both the CRT controller and the host processor contention-free access to the video memory. Unless the CRT controller has continuous memory access, the display will flicker. The

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MEMORY ADDRESS (TYPICAL)	MEMORY DATA (8 BITS)
0D00	ATTRIBUTE 0
0D01	CHARACTER 0
0D02	ATTRIBUTE 1
0D03	CHARACTER 1
⋮	⋮
2N	ATTRIBUTE N
2N+1	CHARACTER N

Figure 4: *The Attribute Assemble mode lets the programmer create a pseudo 16-bit word that describes both the character and its attributes (see text).*

processor cannot, however, be denied access to memory.

The simplest and most common terminal configurations may be referred to as *repetitive memory addressing*. In the repetitive addressing configurations, the microprocessor and the VPAC share memory. The VPAC will repeat the sequence of video addresses for every scan line of every data row. To allow the processor access to the memory, you can use one of several schemes. In one approach, *retrace intervention*, the processor is given memory access during the blanked portion of the display and the VPAC has priority during active video.

The retrace-intervention approach, although simple, does reduce microprocessor throughput by denying the host processor access to memory during active video. An alternate—and more expensive—variety of repetitive memory addressing uses double-speed memory. In double-speed memory addresing, both the processor and the VPAC are allowed video-memory access during alternating time slots within one character time.

Single-Row Buffer Operation

By using the VPAC's DMA mechanism and SMC's CRT 9006 single-row buffer, efficient sharing of the video memory results in systems that have high throughput. In this system, data is loaded into the single-row buffer during the first scan line of every data row. The CRT 9006 also allows this data to be simultaneously sent to the character generator and the CRT 9021B. During all subsequent scan lines, the display is driven by the row buffer, which frees up the video memory. In a display with 12 scan lines per data row, the processor will have uncontested access for 11 scan lines, or 92 percent of real time.

In a single-row buffer arrangement, the processor must be idle for one entire scan line, which could be for 50 to 60 microseconds. This delay means that the processor's ability to respond swiftly to real-time events is compromised. A second DMA device within the system, if needed, might create restrictive timing conflicts. The processor itself might not be able to tolerate a DMA cycle of 50 to 60 microseconds.

Double-Row Buffer Operation

The use of the VPAC with the CRT 9212 double-row buffer lets the user overcome such restrictions by evenly distributing the DMA requests for each data row throughout all scan lines within the data row. With a double-row buffer, while one buffer is fully loaded and supplying data to the character generator for the data row currently being painted, the other buffer is being loaded with the data for the next data row. In the double-row buffer mode, the user can program the number of DMA cycles for each burst and the delay between each DMA burst. In this way, the processor and other DMA devices can perform their tasks more quickly.

Attribute Assemble

In addition to the 7 or 8 bits used to provide character or graphic data, 8 bits may be used to provide attributes such as color, reverse-video, blink, blank, underline, and intensity. This will typically result in 16 bits per character. There are, however, many reasons to keep the video memory 8 bits wide while still providing all the advantages of wide-memory terminals. First, an 8-bit processor might be all that you need to meet the CRT system's design goal. Second, the most inexpensive memory devices, dynamic RAMs (random-access read/write memories), are all 1 bit wide. An 8-bit-wide video memory requires 8 devices; a device must be added for each bit increase in memory-data width.

The Attribute Assemble mode lets the user maintain an 8-bit-wide video memory but "assemble" a 16-bit-wide word for the CRT display. By arranging an 8-bit-wide memory as shown in figure 4, the user can sacrifice time to gain memory-bit width. In other words, for 80 characters per data row, instead of accessing 80 locations of 16 bits each, the VPAC accesses 160 locations of 8 bits each. The VPAC "assembles" the first 8 bits in an internal attribute latch during the first access and outputs these 8 bits while accessing the second 8 bits. At this time the VPAC causes a 16-bit word to be loaded into two double-row buffers every other video-memory fetch.

Double-Height Double-Width Display

The VPAC will enable double-height/double-width characters to be displayed on a row-by-row basis as a function of the two most significant bits of the particular row-table entry. When a particular scan line is to be painted in double height or double width, the VPAC activates the CURS output during the retrace interval (CBLANK). (See figure 5.) This allows logic external to the VPAC to divide the character and dot clocks to produce the desired visual effect. Proper phasing of the divided character clock with respect to CBLANK is necessary so as not to cut the first visible character on the data row in half. The CRT 9021B video attributes controller will automatically perform the division and phasing of the character and dot clock as required to display the double-height or double-width data rows with no additional hardware.

Smooth Scrolling

When a page is filled in a typical CRT system, the entire display jumps up one row, making room for more data to be entered on the bottom row. When *jump* scrolling takes place on a frequent basis, the display is hard to



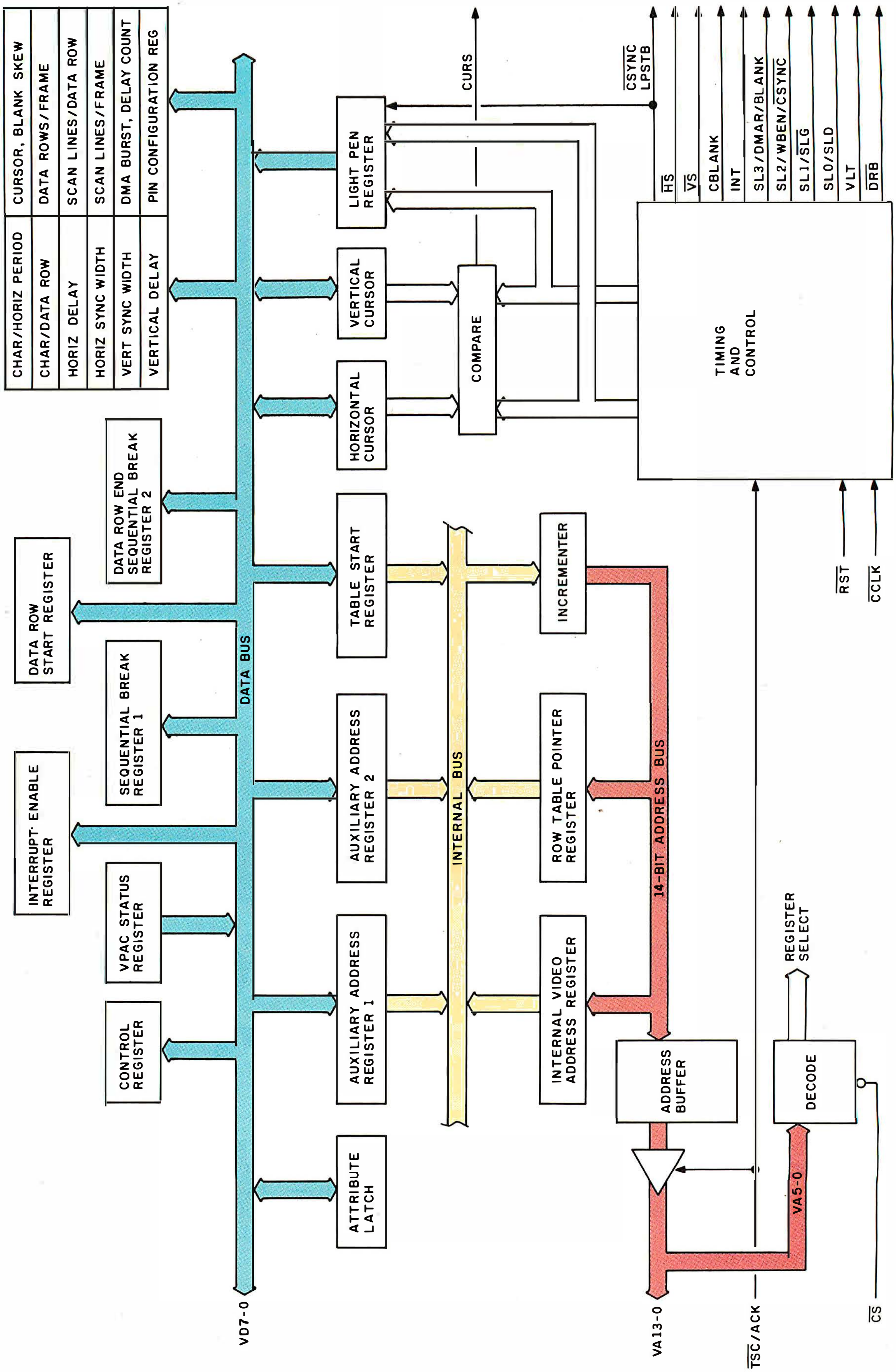


Figure 5: *A block diagram of the CRT 9007 VPAC.*

read. If the increments occur one scan line, rather than one data row, per frame time, the scroll is smoother and easier to read. The CRT 9007 VPAC provides smooth scrolling at variable rates. Furthermore, bidirectional smooth scrolling may take place over any selected portion of the display rather than the whole display.

Smooth scrolling adds some interesting requirements to system design. You can no longer assume that a particular scan line (usually the first or last one within a data row) has an absence of dots as defined by the character generator. Smooth scrolling can define *any* scan line as the first one in a data row. In any given frame, fractions of full data rows will be displayed when the display is in the process of scrolling. Thus the data row that is defined to start a smooth scroll interval and the data row one less than the data row defined to end a smooth scroll interval can show fractional data rows. The first and last data row for a partial-page smooth-scrolling operation is defined in the *data row start* and *data row end* registers respectively. Because a constant number of scan lines is painted on each frame, as one data row loses scan lines, another must appear to take up the extra scan lines. Because of this, it is necessary to maintain an extra data row within the row table. Once the display is scrolled, a portion of the extra data row must enter the display at the appropriate place. If 24 data rows are defined, then for an unscrolled display 24 data-row boundary ($\overline{\text{DRB}}$) signals are generated, all equally spaced in time as defined by the number of scan lines per data row. In this case, the data-row boundary signals will coincide with scan line count 0. Once the display is scrolled, an extra $\overline{\text{DRB}}$ will appear, and some $\overline{\text{DRB}}$s will not be equally spaced.

A smooth scrolling operation involves a data-row insertion at the point defined by the data-row end register when it goes from an unscrolled frame (no offset) to a scrolled frame. In each successive frame, the offset is updated. If the software updates the offset by 1 scan line each frame, the display will scroll smoothly at the rate of 1 scan line per frame. Under software control, it is possible to update the offset register by any number of scan lines to produce a variable-speed smooth scroll. When the offset register is again loaded with 0, it means that the smooth scroll of a single data row has concluded.

A smooth scroll-down operation is accomplished by reversing the process. The offset register is decremented and a data row is inserted at the data-row start position when going from an unsrolled to a scrolled display section. A data row can be deleted in a similar fashion.

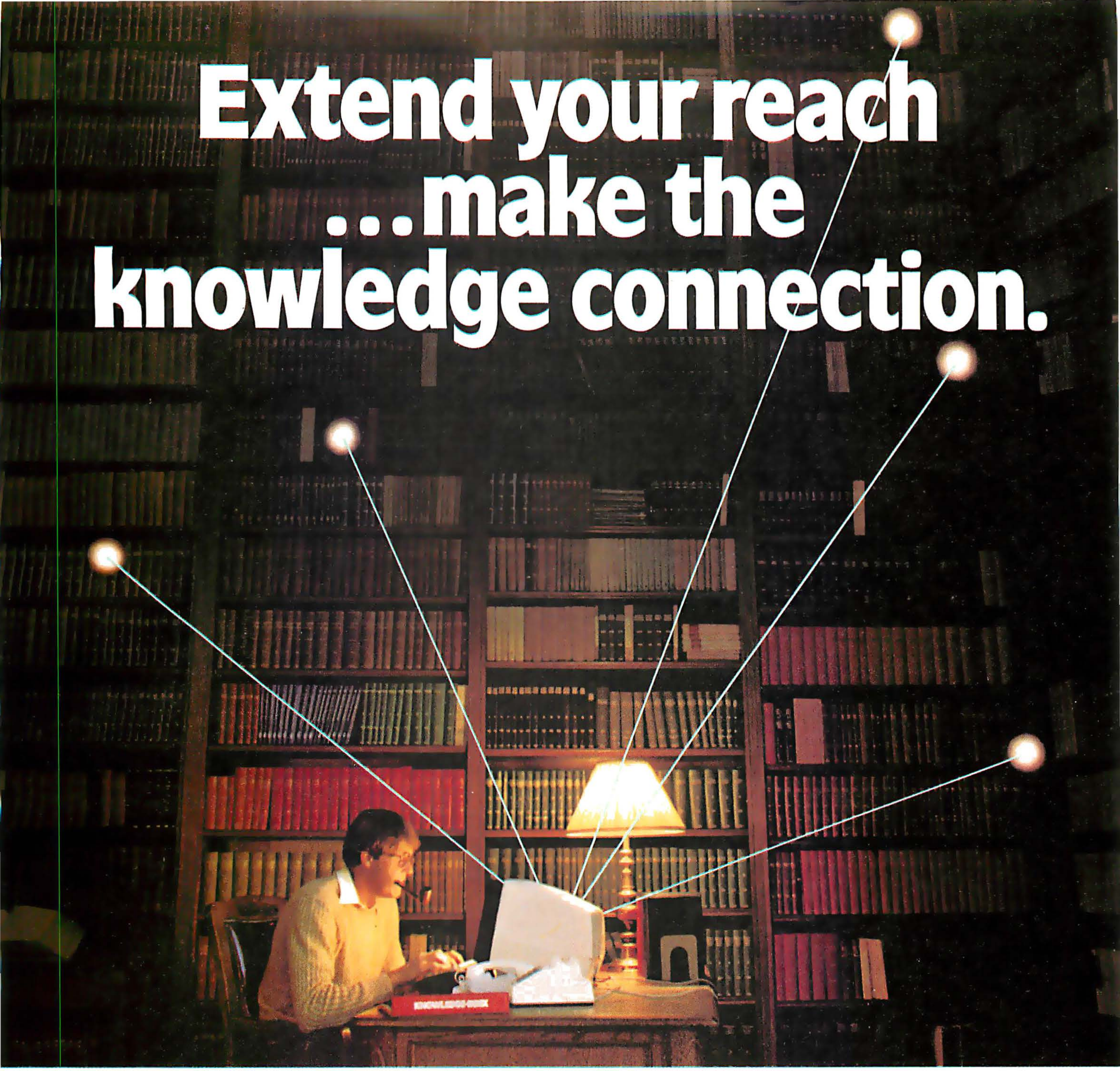
Conclusion

The use of LSI circuitry in the CRT 9007 video processor and controller has two major consequences for manufacturers of video terminals. First, because so many functions are integral to the chip, the component count can be substantially reduced—to less than 20 chips in some applications. As the chip count decreases, the costs of design and manufacturing decrease. Second, some of the features of the VPAC, such as Standard Microsystems' scheme of nonsequential memory addressing, were not previously available on a cost-effective basis. The primary benefit of nonsequential memory addressing is data-row insertion/deletion without moving large blocks of data. Therefore the terminal procesor is not overworked and the video display is free from flickering and blanking. The other major feature is bidirectional smooth scrolling.

For the end user, these improvements mean the next generation of smart terminals will contain even more features at a reduced cost—a trend to be encouraged. ■

For Further Information

For those who want more information on the VPAC and its support chips, Standard Microsystems Corporation has published a data sheet, two technical notes, and two application notes covering the VPAC's programming and use. For copies, contact SMC at 35 Marcus Blvd., Hauppage, NY 11788.



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New Japanese Microcomputers

A Report from the Japan Data Show and Electronics Show

Phil Lemmons
West Coast Editor

The Japanese will make mistakes in the process, but sooner or later they will make some excellent personal computers. That is the lesson of the Japan Data Show '82, held October 19 through 22 at the Tokyo International Trade Center Exhibition Site on Harumi Island. The Japan Electronics Show, held at the same site during the following week, confirmed this impression and also revealed more about the intentions of the Japanese consumer-electronics companies. In short, most of the major Japanese electronics manufacturers are now or soon will be offering every type of microcomputer from handheld units to extremely powerful desktop systems. Most of the Japanese companies have chosen the Intel 8088 and 8086 microprocessor chips for their top-of-the-line personal computers. In addition, the consumer-electronics companies are beginning to produce home computers of a type not yet seen in the United States: sleek, consumer-oriented machines that will enter the home as part of an advanced video-entertainment system.

In this article I'll describe the most impressive machines I saw in Tokyo. I'll also touch on some interesting new developments such as an infrared modem, both infrared and fiber-optic local networks, and the continuing spread in Japan of high-resolution video graphics and dot-matrix and inkjet printers.

The Japanese offer broad product lines aimed at all segments of the world market.

Japanese 16-bit Microcomputers

At least twenty 16-bit microcomputers were on view at the Japanese electronics shows. I will report on the machines of greatest interest to personal computer owners and shoppers. (The order of the following presentation is random.)

National Mybrain 3000: This is the personal computer that you would expect from Matsushita, whose brand names in the United States include Panasonic, National, and Quasar. As photo 1 shows, the Mybrain 3000 comes in four separate units: detached keyboard with eight programmable function keys, a numeric pad, cursor keys, editing keys, and palm rest; a system unit; a video monitor for high-resolution color graphics; and disk drives.

The Mybrain 3000 has an 8088 central processor, a minimum of 96K bytes of user RAM (random-access, read/write memory), and 32K bytes of additional video RAM, plus a 16K-byte ROM (read-only memory). Video RAM can be increased to 128K bytes. Video graphics have a resolution of up to 640 by 400 dots. The available floppy-disk drives include 3-inch, 5¼-inch (160K-byte), and 8-inch (1.2-megabyte) drives, all in separate vertical units. An RS-232C serial input/output (I/O) port is standard, and an IEEE-488 port, a light-pen, joysticks, and a graphics tablet are available.

National is offering both MS-DOS (from Microsoft) and CP/M-86 (from Digital Research) as operating systems, along with many of the languages available with these operating systems in the United States. Applications software can be expected to ap-

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Photo 1: *National Mybrain 3000.*



Photo 4: *NEC PC-9800.*



Photo 2: *Mitsubishi Multi16.*



Photo 3: *Toshiba Pasopia 16.*

pear by the time the Mybrain 3000 reaches the United States, probably in mid-1983.

With two 5¼-inch disk drives, a video monitor, an 80-column dot-matrix printer, an operating system, and BASIC, the system lists for 783,500 yen (about $3000 at the exchange rate of 265 yen per dollar, which I will use throughout). With one 5¼-inch floppy-disk drive and no printer, the cost in Japan is about $2000. Of course, shipping the machines to the United States and marketing them here should add to the cost.

Mitsubishi Multi16: Since the Multi16 has already been introduced in the United States, I'll be brief. The Multi16 looks like an "all-in-one" microcomputer (all the components in one box), but the combined monitor/disk-drive unit is detachable from the system unit/keyboard combination (see photo 2). The Multi16 has an 8088 processor and an optional 8087 coprocessor, standard memory of 128K bytes expandable to 576K, 640- by 400-dot video resolution, one or two 300K-byte 5¼-inch floppy-disk drives, an RS-232C port with optional GP-IB, a general-purpose parallel bus, and the CP/M-86 operating system. Several different disk drives and several different printers are also available.



Photo 5: *NEC N5200. It is marketed as the Advanced Personal Computer in the U.S.*



Photo 6: *Hitachi BASIC Master 16000.*

Microsoft BASIC, Multiplan, and Supercalc-86 are among the available software, as well as a Japanese word processor with the intriguing name Multiword-J. Could this be related to Microsoft's rumored Multiword?

Toshiba Pasopia 16: The Toshiba personal computer, sold in the United States as the T100, is called the Pasopia in Japan, and the Pasopia 16 is its big brother. (In the United States, the Pasopia 16 will be called the T300.) A variety of video monitors is available with resolution ranging from 320 by 200 to 640 by 500 dots. The monitor rests on its own pedestal or on the top of the compact system unit, which contains two thinline 5¼-inch disk drives holding a total of 640K bytes. Photo 3 shows the Pasopia 16 with an optional 80-column dot-matrix printer resting on the system unit. Eight-inch floppy disks are also optional. The slender detached keyboard has a cursor diamond, numeric pad, editing keys, and programmable-function keys. The processor is an 8088; an 8087 math coprocessor is optional. Standard memory is 4K bytes of ROM and 192K bytes of RAM expandable to 512K. Users can also add video RAM of 128K or 256K bytes. Standard equipment includes one RS-232C port and one parallel printer port.

MS-DOS is the only operating system available for the Pasopia 16. Toshiba offers T-BASIC 16 and other Microsoft languages.

In addition to the Pasopia 16, Toshiba showed the Tosbac UX-300, based on the Toshiba 88000 processor, which has segment registers and seems to be very much like an 8086. The UX-300 runs Unix and has a vertically oriented video monitor resting on a pedestal, 512K bytes of RAM, two RS-232C ports, and an 8-inch disk drive holding 1 megabyte and resting horizontally in the separate system unit. With a 10-megabyte hard disk, the UX-300 costs about $9300.

NEC PC-9800 and Advanced Personal Computer: One of the surprises at the Japan Data Show was the NEC (Nippon Electric Company) PC-9800 (see photo 4), a personal computer based on the Intel 8086—the true 16-bit version. The PC-9800 surprised people because NEC introduced its 8086-based Advanced Personal Computer (APC) in the United States in mid-1982. In Japan, the APC machine sells under the name N5200 (see photo 5). How many American companies make two 16-bit microcomputers based on the same processor?

In Japan, the APC (N5200), with 128K bytes of RAM, two 8-inch floppy disks holding 1 megabyte



Photo 7: *Hitachi PT-1 Personal Terminal.*



Photo 8: *Sanyo MBC-55.*

each, a high-resolution monochrome monitor (640 by 475), a serial port, and a printer port, has a list price equivalent to about $2800. The same system lists in the United States for $3900.

With its separate keyboard (cursor keys, programmable keys, numeric pad, and editing keys), system unit, monitor, and disk drives, the PC-9800 looks more like a home machine than the APC does. The standard memory is 128K bytes expandable to 640K. However, the PC-9800 also has a 96K-byte ROM containing NBASIC-86, and you can get another 96K bytes of video RAM. NEC offers monitors for the PC-9800 with resolution as high as 640 by 400 dots and also an assortment of disk drives. Both MS-DOS and CP/M-86 are available. With two 8-inch drives storing a megabyte each, the keyboard, and the system unit containing 128K bytes of RAM, the PC-9800 costs the equivalent of about $2600 in Japan. When the PC-9800 reaches the United States (and the NEC spokesmen would not say whether or when that will happen), the list price will probably be about the same as that of the APC.

When I pressed the hosts in the NEC booth about the differences between the APC and the PC-9800, they would say only that the PC-9800 lacks the software power-down that the APC has. There's also the BASIC in ROM, of course, and the PC-9800 system unit is clearly too small to hold the boards that go in the APC's large card cage. (I was not allowed to look inside the PC-9800 or any other machines at the Japanese shows.) The last obvious difference is that the APC has 22 programmable-function keys to the PC-9800's ten.

Both the APC and the PC-9800 are impressive machines. NEC deserves praise for basing both of its top personal computers on the 8086 rather than imitating IBM and choosing the less powerful 8088.

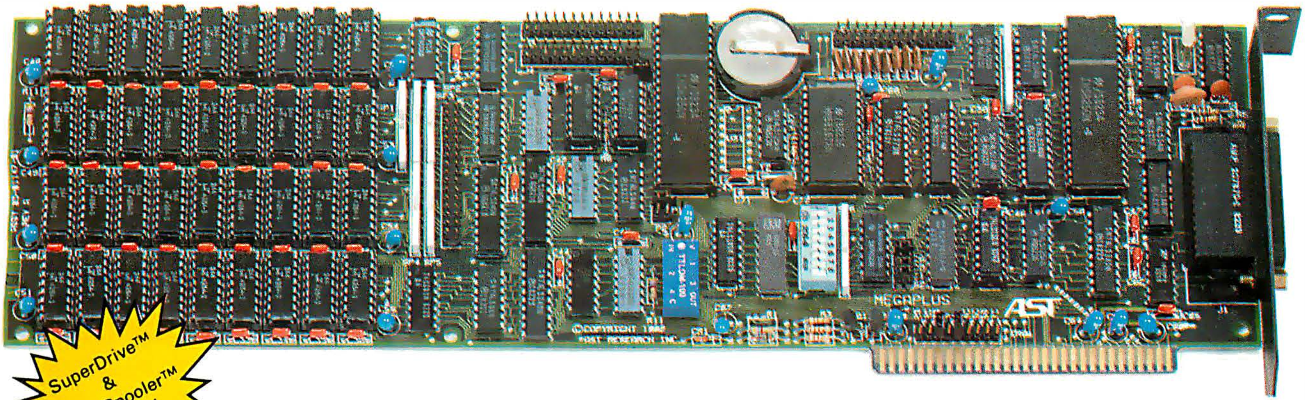
Hitachi BASIC Master 16000 and PT-1 Personal Terminal: Like NEC, Hitachi is offering two 16-bit personal computers, the BASIC Master 16000 (photo 6) and the PT-1 Personal Terminal (photo 7). The BASIC Master 16000 has an 8088 processor, runs MS-DOS, and has 320K bytes of RAM as standard equipment. Video resolution is 640 by 400. The system unit, unlike most of the other modular Japanese microcomputers, is taller than it is deep. Two 5¼-inch floppy disks hold 320K bytes. The Hitachi booth had no brochures about the BASIC Master 16000, and information about it was limited, but the price quoted was 490,000 yen, or about $1850. I was unable to determine for certain whether that included the video monitor and two disk drives, but it seems hard to believe that it could.

The PT-1 also uses the MS-DOS operating system. Video resolution is 720 by 520, and each of the 8-inch floppy disks holds a megabyte of data. The Hitachi exhibits of office automation equipment showed the PT-1 communicating with larger Hitachi systems.

Both the PT-1 and the BASIC Master 16000 have detached keyboards. Besides the numeric keypad, cursor keys, and editing keys, the PT-1 has 24 programmable-function keys. The BASIC Master 16000 has 10 programmable-function keys besides editing and cursor keys and a numeric pad.

Sanyo MBC-55: Sanyo's top-of-the line personal computer is the 8088-based MBC-55. The compact system unit contains two thin-line 5¼-inch floppy disks holding 160K bytes each. Although a Sanyo representative in the booth at the Electronics Show said the disk format used is not the same as the IBM PC's, he also said that the hardware bus is compatible. Buyers should, therefore, be able to use boards made for the IBM PC in the Sanyo MBC-55 when it reaches the United States.

The MBC-55 runs CP/M-86, Concurrent CP/M-86, and MS-DOS. Standard memory is 64K bytes expandable to 256K. A 4K-byte "boot" ROM (which contains instructions for reading the operating system from a floppy disk) is standard. An 8087 coprocessor is optional. The MBC-55 will go on sale in the United States in June or July 1983. Although the exact price in the United States has not been



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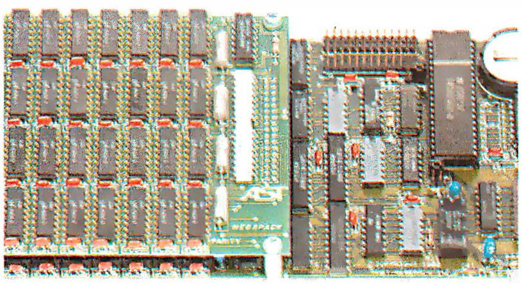
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Photo 9: *Sord M-343.*

decided, the Sanyo booth attendant said that the MBC-55 with 64K bytes and one floppy will cost about $1000. That does not include the video monitor.

As photo 8 shows, the MBC-55 is very compact and seems aimed at the home market. Sanyo did not exhibit the machine at the Data Show, saving it for the more consumer-oriented Electronics Show. Sanyo showed a great deal of video-recording equipment, and the MBC-55 looks as if it might be part of the same family of products. The MBC-55's system unit is only 4⅓ inches (11 cm) thick, just deep enough to accept boards made for the IBM PC. To keep the keyboard as small as possible, Sanyo chose to supply only four programmable-function keys. The numeric keypad, as on the IBM PC, doubles as a cursor-control pad. Although no Sanyo spokesman said so, I would not be surprised to see the MBC-55 sold as part of a home-video system and used to control video storage systems and to mix computer graphics with video images. (See the section on the Sharp X1 microcomputer later in this article.) The marketing approach would be to say, "Since you're buying a new color television, why not let us throw in an IBM-compatible personal computer?"

Sord M-343: Sord, one of Japan's few new companies, makes several interesting microcomputers. (See the comments on the M5 home computer and the M23P portable later in this article.) As photo 9 shows, the M-343's color graphics are impressive. The M-343 is the Sord flagship and is powerful indeed. The processors include an 8086, and 8087, and a Z80A. The M-343's large, all-in-one unit can hold up to 1176K bytes of RAM. The video resolution is 640 by 400. There are four serial I/O ports, and the M-343 can serve as the hub of a network of Sord M23 Z80A-based computers. Standard floppy-disk storage is 1.2 megabytes. The keyboard has 20 programmable-function keys, cursor-control keys, a numeric keypad, editing keys, and another 12 keys that I believe are dedicated to communications and system operations. Finally, the M-343 is the only major Japanese 16-bit microcomputer that has three vacant S-100 bus slots.

Sord offers five different operating systems: the Realtime Disk Operating System, the Realtime Multi-job Disk Operating System, MS-DOS, CP/M-86, and the UCSD p-system. Sord has developed an applications system (PIPS) that integrates database, spreadsheet, and graphics functions. Sord achieved this software integration sooner than its American competitors.

The M-343's color graphics are impressive.

Anritsu Packet II Hy Personal Computer: What happened to the 68000 processor chip? The only new 68000-based personal computer that I saw in Japan is the Anritsu Packet II. This powerful machine is an all-in-one computer with two 5¼-inch floppy disks (150K bytes each) horizontally mounted to the right of the video monitor. The keyboard has cursor keys, editing keys, 10 programmable keys, 12 keys dedicated to BASIC commands, and a numeric keypad. A printer is built in and sends 40-column paper scrolling out above the monitor. Standard equipment includes 256K bytes of RAM. You can add memory in 128K and 256K increments. You can also add various kinds of ports and an analog-to-digital (A/D) converter. One of the best features of the Packet II is the way it accommodates added features. The back has six horizontal metal plates that come off and allow you to slide a board in just as you slide a drawer into a chest. Each board has a metal plate on its back that closes the opening in the back of the machine. Each I/O board has appropriate sockets in its back. Anritsu intends the Packet II for technical users, and the software supports engineering graphics.

AI Electronics AI-M16: Another hefty and powerful Japanese microcomputer is the AI-M16 from AI Electronics. Based on the 8086, the M16 also has an 8089 I/O processor and an optional 8087 math coprocessor. The keyboard is detached, but everything else comes in one big package with disk drives mounted vertically to the right of the monitor. Standard equipment includes a calendar clock.

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Standard RAM is 256K bytes expandable to 1 megabyte. The public bus is an IEEE-796 bus. There are two serial ports and provision for a lightpen. A 16K-byte boot ROM and an 8K-byte character-generator ROM are standard, and a 128K-byte kanji (Japanese-character) ROM is optional. Mass storage can be on 8-inch floppy disks or 5¼-inch Winchester hard disks.

The M16 comes with a wide choice of operating systems: Genix, CP/M-86, Concurrent CP/M-86, MP/M-86, MS-DOS, or the UCSD p-System. Languages mentioned include LISP, PL/I, and C.

Seiko 9500 and 8600: The 16-bit Seiko microcomputer shown in Tokyo was the 9500 Super Personal Computer. All the components come in one large package with disk drives mounted horizontally beside the monitor. What makes the 9500 super? It has an 8086 processor, an 8087 math coprocessor, and two 8088s: one to manage I/O and the other to control communications. Standard RAM is 256K bytes, maximum is 512K. The operating system is RMX/86 (from Intel?). The color video is dazzling, with 512 by 480 resolution. But the large package would be awkward in most settings.

While I was in Japan, Seiko introduced the 8600, based on the 8086 microprocessor, intended for the American market, and decidedly smaller and better looking than the 9500.

Slick Consumer Computers

Sharp X1: One eight-bit computer made a big impression at the Electronics Show, the Sharp X1. The X1 has two primary components, the CZ-800D and the CZ-800C. Shown in photo 10, the X1 is a Z80A-based machine but certainly not another Z80A desktop system. Sharp offers the CZ-800D 14-inch color television monitor for 113,00 yen, or about $425. The CZ-800D has one button that other color televisions don't; it turns the television into a color monitor. For another 155,000 yen (about $585) you can have the CZ-800C, consisting of an integrated computer and keyboard unit. The computer is

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Photo 10: *Sharp X1. The symbol of the Tokyo Data Show is superimposed on the television broadcast.*



Photo 11: *Aval AVC-777J2.*

based on a Z80A and has 64K bytes of RAM, 4K bytes of video RAM, and 6K bytes of character RAM. The 80C48 and 80C49 processors supplement the Z80A. You can add another 48K bytes of video RAM as an option.

The computer unit includes a built-in cassette-tape recorder for data storage. Also standard in the computer unit are a Centronics-type printer interface, an interface for two joysticks, a clock with battery backup, and sound-synthesis output capacity ranging over eight octaves. When the system is being used as a computer, it can display 25 lines of 80 characters on the monitor. Four additional I/O ports are optional, as is a unit containing two very thin, 5¼-inch floppy disks.

An optional digital Telopper (the CZ-8DT) lets you connect the computer to a video camera, video-tape recorder, or videodisc. The keyboard has five separate blocks: character keys, number keys, function keys, television-monitor-control keys, and tape-operation keys. A color BASIC interpreter is standard equipment and includes a function that assigns a priority to each character and color in order to achieve the appearance of perspective. You can enlarge, reduce, or move graphics displays under program control. You can change each color variable instantly. You can paint and hatch graphic "phrases" (areas that can be manipulated as units) in eight basic colors and neutral colors to achieve the effect of "tile-painting." You can mix five different character styles in the same display. The calendar clock works with a programmable timer and can turn on the television for a broadcast while you are away.

The Sharp X1 lets you superimpose your computer graphics on video images. You can, in other words, display television signals and computer graphics simultaneously. An RGB (red-green-blue) mix circuit makes the superimpositions possible. Sharp has named the concept *visual integration* and calls the X1 the world's first personal computer/television monitor system. Suggested applications include video editing, art, and games. The most obvious use would be putting titles on home videotapes.

Sony SMC-70: The SMC-70 is another Z80A-based microcomputer and seems destined for integration in a video system too. Sony revealed at the electronics show that the SMC-70's add-on 8086 unit will run MS-DOS. Sony has sold the SMC-70 in the United States only as a business system and has not sold the system in Japan at all. The system differs from the Sharp X1 in several important respects: the SMC-70 has two 3½-inch disk drives as standard equipment, can be upgraded by adding an 8086 microprocessor, has a numeric keypad only as an optional

separate unit (strange for an office computer), and costs much more than the X1. Even though the SMC-70 can control videodiscs, Sony's true consumer computer has yet to appear.

Japanese Portables

I expected to find a lot of new Japanese portable computers at the Tokyo shows but found only four portables of interest, two of them from Aval, one from Sord, and one from Epson.

Aval AVC-777J2: This portable all-in-one computer (see photo 11) running CP/M 2.2 might be thought of as Japan's answer to the Otrona Attache. A Z80A system with 64K bytes of user RAM and 16K bytes of video RAM, The AVC-777J2 has a 5-inch monochrome video monitor, two double-sided thin-line 5¼-inch drives storing 600K bytes each, a built-in 5-inch thermal printer, one parallel port, two RS-232C serial ports, a connector for an 8-inch floppy-disk system, a connector for the system bus, and video output for a larger monitor. The keyboard is detachable and fits into the carrying case along with everything else. The price in Japan is 880,000 yen, or about $3320. The weight is 12.5 kilograms, or about 27.5 pounds.

Aval AVC-666: This is billed as a CP/M 2.2 development system, but I find it even more appealing as a portable. It doesn't have a printer or a monitor and has the two 5¼-inch drives mounted horizontally. In many other respects, the AVC-666 is just like the 777J2. The AVC-666 is only as wide as the two 5¼-inch floppy disks, brings a video signal out for connection to a monitor, and weighs much less than the 777J2. It costs the equivalent of about $2500, with an optional 12-inch monochrome monitor costing another $152. With one monitor at home and the other in the office, the AVC-666 would serve as an adequate portable by today's standards.

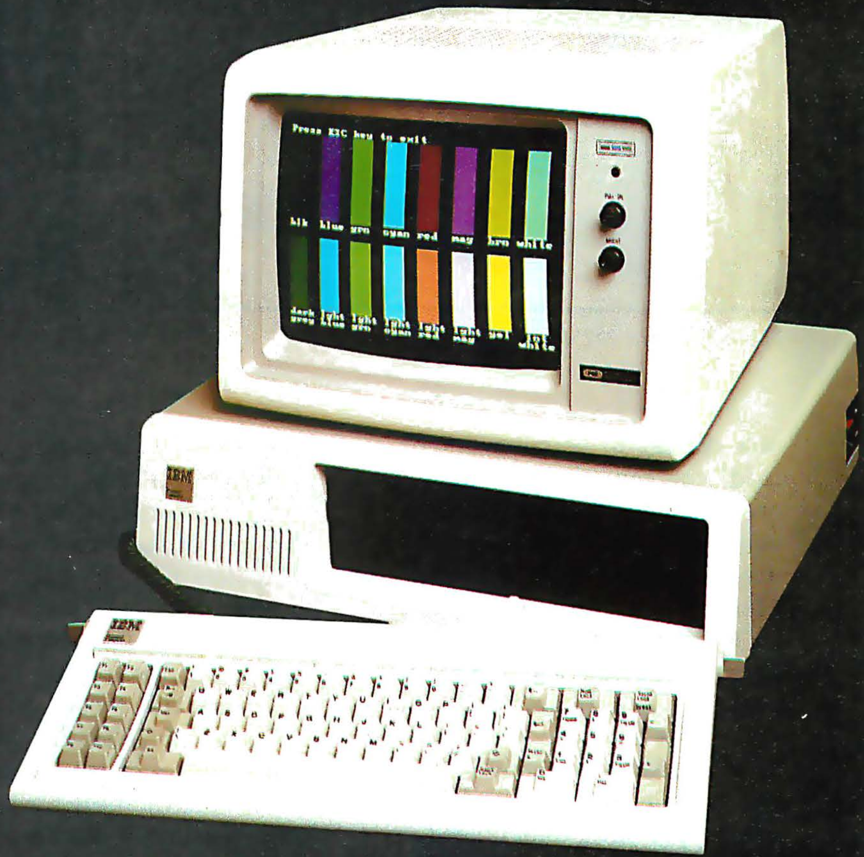
Sord M23P: I consider the Sord M23P (see photo 12) a true portable and a good value. The M23P has a Z80A processor, 128K bytes of RAM, and an 8-line by 80-character liquid-crystal display (LCD). That is enough

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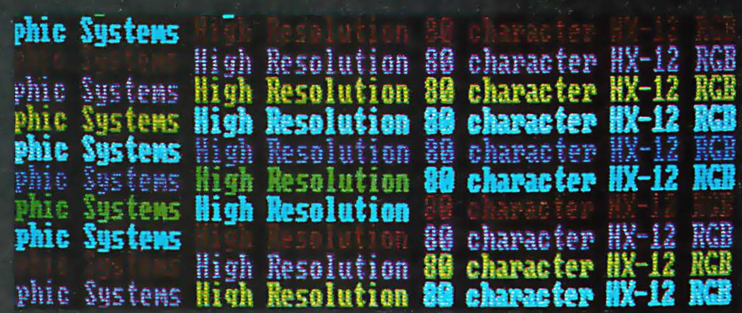
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Photo 12: *Sord M23P.*



Photo 13: *National JR-200 Personal Computer.*

of a display to permit work on the road; you can edit text without too much strain on human memory. At home, of course, you'll want the optional 12-inch green monitor or 14-inch color monitor (both 25 lines by 80 characters). The integral keyboard has a numeric pad, four cursor keys, seven programmable-function keys, plus the standard keyboard. Two double-sided Sony microfloppies (running at 600 revolution per minute) provide a total of 580K bytes of high-speed mass storage. With the LCD, the carrying case, and the rechargeable battery pack (the yellow box in photo 12), the M23P weighs 9 kilograms or 19.8 pounds. The M23P runs Sord's PIPS integrated spreadsheet-database-graphics software package and will cost about $2200 in the United States. The combination of size, price, and performance should make the M23P a real competitor among the portables.

Epson HC-20: This true portable is sold in the United States as the HX-20. It has a tiny display, microcassette mass storage, and limited computing power compared to the M23P. The HX-20 costs only about $800. It is the ideal size for portability (the whole computer is no bigger than full keyboard size) but does have performance limitations. It will be interesting to see how the long-term competition based on size, price, and performance treats the HX-20 and the M23P.

New Home Computers

National JR-200 Personal Computer: The computer shown in photo 13 is one of the three low-cost home computers now produced by Matsushita; the others are the National JR-100 and the Tomy 16-bit Graphics Computer. The JR-200 has a 6802 processor, 16K bytes of ROM, and 32K bytes of RAM. The rubber keyboard has a wonderful touch, a diamond configuration for the cursor keys, plus a full standard keyboard with shift, insert, and delete keys. It can be used with a variety of monitors, including a television set or an RGB monitor. The JR-2000, which has a list price of about $300 in Japan, can use tape recorders or disk drives for mass storage, drive a speaker, and handle input from joysticks.



Photo 14: *Sord M5*

JR-100: The JR-100 has a 6802 processor, 8K bytes of ROM, 16K bytes of RAM, a more limited keyboard, and a list price of abut $210. (The Tomy machine was not exhibited at the Electronics Show, but later I saw it for sale in the Akihabara district in Tokyo. The Tomy processor is a TMS9995.)

Sord M5: This computer (photo 14) has a Z80A processor, an 8K-byte ROM containing a monitor, 4K bytes of system RAM, and 16K bytes of graphics RAM. You can get software for the M5 in audio cassettes or ROM cartridges. Cartridges include BASIC, household accounting, bank-loan management, and simple word processing. Most of the ROM packs are 16K bytes. The keyboard is typewriterlike, two joysticks are optional, an audio cassette provides mass storage, and both an AC power unit and a DC power pack are available. The M5 features RF (radio-frequency) output so that you can use a television as a display. Most interesting of all is an animation program that lets you use 32 types of special figures called sprites. The basic M5 costs about $187 in Japan.

Sanyo PHC-25: The Sanyo PHC-25 is an advanced home computer with a list price of about $264. The complete computer is slightly larger than a standard keyboard but has four cursor-control keys and four programmable-function keys. A 24K-byte BASIC is in ROM, and there are 22K bytes of RAM. As you

would expect, the PHC-25 uses a television as a video monitor and a cassette recorder for mass storage. The Sanyo PHC-20 is less expensive and less powerful than the PHC-25.

New Hand-Held Computers

Sanyo PHC-8000: This hand-held computer has an NSC-800 CMOS microprocessor, 24K bytes of ROM, and 4K bytes of RAM. To the right of the one-line LCD are five programmable-function keys and the break key. Four cursor-control keys and a home key are in a diamond configuration—a first, I think, for hand-held computers. The QWERTY keyboard is too small for touch-typing, as the description "hand-held" implies. The list price is 69,800 yen or about $263. An optional I/O unit, the PHC-8010, costs almost twice that amount and permits connection to a video monitor and a microcassette recorder as well as adding 14K bytes of ROM and 22K bytes of RAM. A tiny printer is available, as is an acoustic coupler. Computer, I/O unit, microcassette recorder, acoustic coupler, and printer all fit in a custom attaché case.

Toshiba Pasopia Mini: The computer in photo 15 has an 8-bit CMOS microprocessor, 4K bytes of RAM, and 20K bytes of ROM, which contain a 16K-byte BASIC. The one-line LCD is above the keyboard. Four cursor-control keys are above the numeric keypad. The base price is about $210. Another 12K bytes of RAM costs $113. An I/O expansion unit permits connection of a printer and a cassette recorder and costs another $170.

NEC PC-2001 Hand-Held Computer: This is the hand-held computer that I liked best. It has an 8-bit CMOS uPD7907 microprocessor running at 4 MHz, 36K bytes of ROM, and 16K bytes of RAM. It also has an RS-232C serial port (up to 2400 bits per second) at the left end, a 2-line by 40-character LCD, four cursor-control keys, two editing keys, five programmable-function keys, a numeric pad, and a typewriterlike keyboard that is, of course, too small for touch-typing. The list price is 59,000 yen, or about $225.

Company Lines

The trend among electronics companies in Japan is to produce complete lines of microcomputers, everything from hand-held to very powerful desktop systems. Consider NEC, for example. It makes the PC-2001 hand-held computer, the PC-6000 home computer, the PC-8000 Z80-based personal computer, the PC-8800 (an improved Z80-based personal computer), the PC-9800 (an 8086-based personal computer), and the N5200 (or Advanced Personal Computer, another 8086-based personal computer). Toshiba makes the Pasopia Mini hand-held computer, the Pasopia Z80-based personal computer, the T200 8-bit desktop computer with two 5¼-inch floppy disks, the T250 8-bit desktop computer with two built-in 8-inch floppy disks, and the Pasopia 16, an 8088-based personal computer. Both NEC and Toshiba spokesmen said that they will produce keyboard-sized computers similar to the Epson HC-20 before the end of 1983. More powerful portables are likely to appear also.



Photo 15: *Toshiba Pasopia Mini.*



Photo 16: *These Radicom infrared transceivers are mounted on top of Hitachi BASIC Master 16000 computers. The tapes running from each transceiver to mirrors in the ceiling indicate the path taken by the infrared beams.*

What American manufacturer is producing a comparable line of microcomputers? Only Hewlett-Packard. True, Hewlett-Packard makes no home computer like the PC-6000, but HP is making portables, a variety of 8-bit systems, at least two 16-bit systems—one based on the 8086, the other on the 68000—and the incredible new model 9000, which represents the state of the art in microcomputing (a 32-bit system with 128K-byte RAM chips and very fast operation). To some degree, Hewlett-Packard's emphasis on technical users may suggest that the company is not competing for as broad a market as NEC, but Hewlett-Packard cannot be accused of fearing to compete.

The Japanese seem determined to keep making new microcomputers until each segment of the world market says, "That's the computer I've been waiting for." Let's hope that more of the major American electronics manufacturers will broaden their product lines and compete more vigorously.

High-Resolution Displays and Printers

The Japan exhibitions demonstrated once again that the Japanese are pushing ahead in the development of relatively inexpensive high-resolution video monitors, inexpensive high-resolution dot-matrix printers, and color displays and printers. As has often been noted, the Japanese katakana and kanji character sets force the Japanese to use high-resolution displays and very fine dot-matrix printers. The Japanese had to develop low-cost versions of such displays and printers if the microcomputer market was to expand in Japan as rapidly as elsewhere, and they have now done so. Many companies showed dot-matrix printers that produced characters that could be described fairly as "letter quality." Fujitsu and Matsushita both demonstrated impressive thermal color-transfer printers.

Disappointments

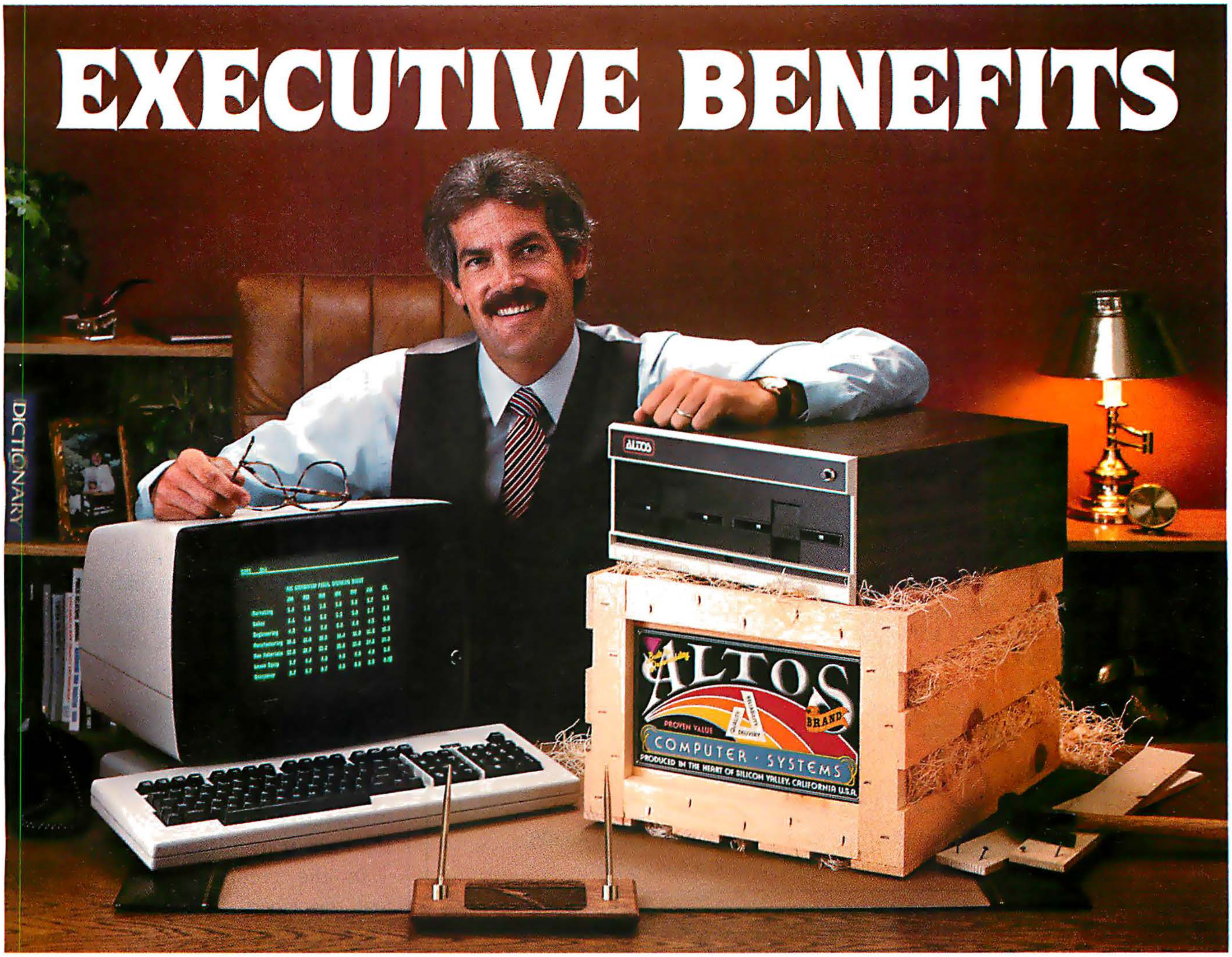
One disappointment—and probably the reason that so few portable computers were introduced—concerned the development of flat-screen displays. The plasma displays and LCD televisions were on view at the shows, but price, product life, or both have prevented their use in affordable portable computers. The Sony flat-screen cathode-ray tube (CRT) was not exhibited. The Victor company showed a very high resolution 5-inch CRT monitor.

Nor was there an abundance of low-cost 5¼-inch Winchester disks. While Matsushita showed an optical storage system, the most interesting such exhibit was from Drexler, an American company (see "Optical-Memory Media" by Edward Rothchild, March 1983 BYTE, page 86).

Optical and Infrared Communications

NEC showed a fiber-optic-based microcomputer network called Netbranch 4800. NEC had four microcomputers connected by NEC optical branch modules at the Electronics Show. The network provides communication at 10 million bps and can extend over 3 kilometers. The Branch 4800 module connects the local network to a larger network.

Is the world ready for an infrared-based local network? Hitachi and a small company called Yagi showed an infrared-based network connecting two Hitachi BASIC Master 16000s. As you can see from photo 16, the usual cables are replaced by infrared transceivers—which look like



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lamps—located atop each BASIC Master 16000. The transceivers, called Radicoms, communicate with one another via mirrors on the ceiling. That's right, it's all done with mirrors. As the network gets bigger, you need more mirrors, but you don't need any cables. Would cigarette smoke impair communications? If so, throw the smokers out. The Radicom network at the show was described as a prototype.

Yagi also showed a working infrared-based modem called the Beacom. As you might expect, it looks like a lamp. Described as a free-space optical communication system, Beacom can link two points that cannot be linked by cable, can relay television broadcasts, can perform high-speed data communications, and is said to be free from interference from sunlight and artificial light. Different models communicate at from 1 to 3 million bps and at ranges of from 300 to 1600 meters. Of course, you need interfaces between the computers and the light transmitter/receivers.

In the communications products just described, in the clever and attractive Sharp X1 microcomputer, and in printers and displays, the Japanese have brought something new to the world of microcomputing. More innovations would be welcome, including those innovations that substantially lower the price of equipment already available elsewhere. ■

Exploring the Asian World of Microcomputers

During my travels in Asia, I attended the Korea Electronics Show in Seoul, the Taiwan Electronics Show in Taipei, the Hong Kong Consumer Electronics Show in Kowloon, and China Comm 1982 in Beijing, People's Republic of China, as well as the Japanese shows described in the accompanying article.

A delightful surprise was the discovery of the Akihabara neighborhood in Tokyo, an electronics bazaar that surpasses anything I have ever seen or imagined. I'll discuss this wondrous neighborhood as well as encounters with microcomputers at the other shows in a second article in the May issue of BYTE. . . . P.L.L.

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- Transmit your password to the host computer
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- The protocol for accessing any other computer.
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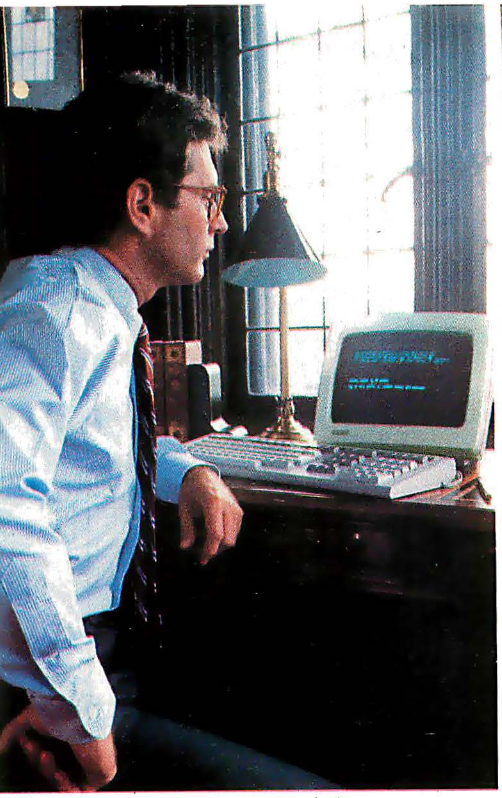
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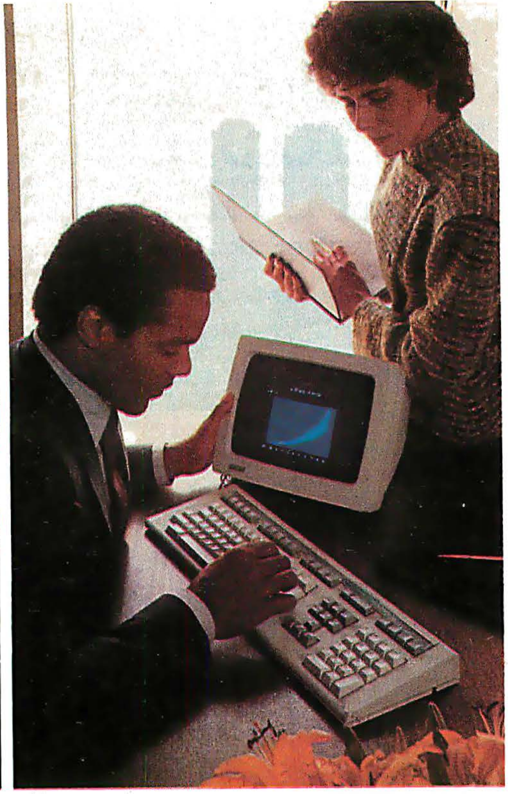
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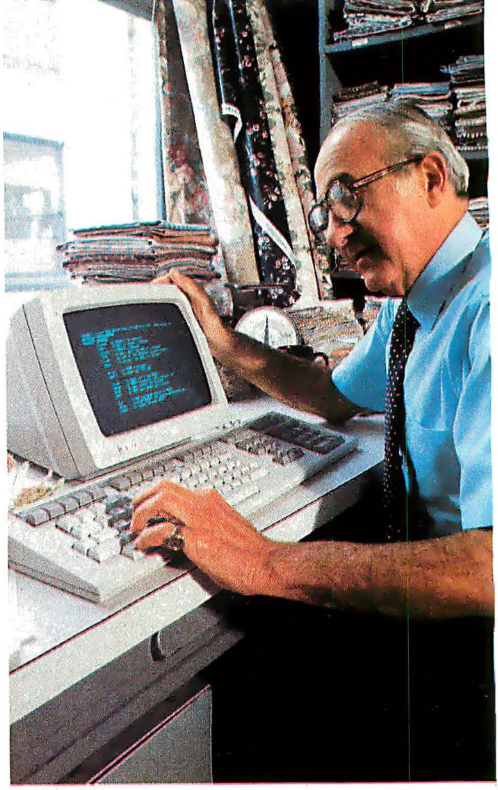
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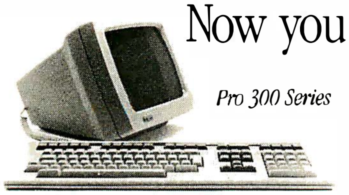






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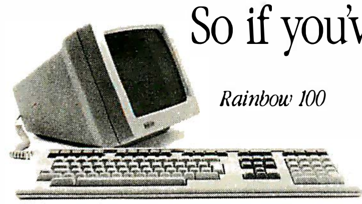


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Intel's 80186

A 16-Bit Computer on a Chip

The 80186 is the first integrated circuit that attacks the cost problem in 16-bit microcomputers.

Tony Zingale
Product Marketing Engineer
Intel Corporation
3065 Bowers Ave.
Santa Clara, CA 95051

Two factors are slowing the rush to 16-bit microcomputers. The 16-bit systems cost more than their 8-bit ancestors, and they have less software available to them than 8-bit systems. Fortunately, time is solving the problem of software availability for 16-bit machines, and very-large-scale integration (VLSI) will soon reduce the cost of 16-bit systems.

The 80186 or iAPX 186 (advanced processor) from Intel is the first integrated circuit that addresses the cost problem in 16-bit microcomputers. The phrase "computer on a chip" is often used to describe microprocessors, but they are really central processing units (CPUs) only. The 80186, on the other hand, incorporates in a single chip all the functions of a CPU *board* except memory.

The 80186 combines an enhanced 8-MHz 8086-2 CPU with a clock generator, two independent high-speed DMA (direct memory access) channels, and a programmable interrupt controller. It includes three programmable 16-bit timer/counters, programmable memory-select and peripheral-select logic, a programmable wait-state generator, and a local bus controller, all on one 68-pin chip (see figure 1). One 80186 chip will replace as many as 20 other chips, reducing the size, weight, power-supply requirements (a single 5-volt supply is all it needs), and the cost of the system while increasing performance (see table 1).

Up until now, the difference in the cost of integrated circuits for 8-bit and 16-bit systems has been significant. A little computation confirms that fact. Building an 8086-based computer system requires the CPU chip ($19.15 in quantities of 10,000) and additional integrated circuits that cost $52.35. Building an 8-bit 8085-based system requires a CPU chip that costs only $2.65 and other chips costing $27.10, for a total of $29.75. The integrated circuits for an 8086-based system, then, cost $41.75 more than similar parts for an 8085-based system.

The 80186 chip narrows that price differential considerably. While the chip itself costs $30.00, the additional integrated circuits to complete the system cost only $5.90. Consequently the integrated circuits for the 80186 cost only $6.15 more than those for the 8085 system (see table 2).

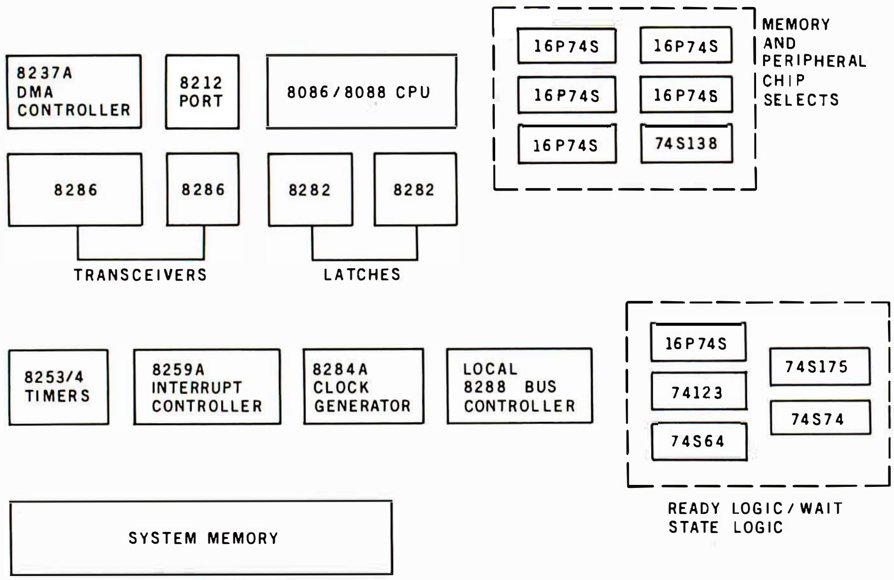
Equally important to the end user, the 80186 uses the same instruction set as the 8086 and 8088 and is compatible with the large and growing body of software and peripherals available for those systems. The 80186 adds 10 instructions that enable programmers to make more efficient use of the code, and Intel is revising its development software tools to include support for the new instructions.

	8085	8086	80186	80286
Performance in MIPS	.07	0.3	0.7	1.5
Cost/performance ratio in IPS/$	700	1500	10,000	7500

Table 1: *Performance comparisons of four microprocessors. MIPS means million instructions per second; IPS/$ means instructions per second per dollar.*

About the Author
Tony Zingale, product marketing engineer for Intel's 80186 and 80188 microprocessors, has extensive experience in the use of microprocessor technology in a wide variety of applications.

(1a)



(1b)

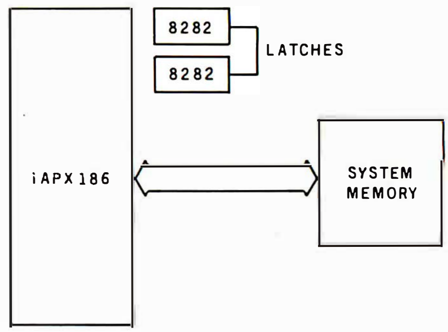


Figure 1: *(1a) Chips necessary to make an 8086-based microcomputer system. (1b) Chips necessary to make an 80186-based microcomputer system.*

10K Piece Kit		
80186		$30.00
2 latches (8282)		5.90
	total	$35.90
Equivalent 16-bit CPU Board		
8086 CPU (5 MHz)		$19.15
DMA controller (8237A-5 + 8212 port)		15.30
interrupt controller (8259A)		3.75
timers (8253)		3.40
2 latches (8282)		5.90
2 transceivers (8286)		5.90
chip-selects (6 memory/7 peripherals)		3.50
wait-state generator		3.50
local bus controller (8288)		7.95
clock generator (8284A)		3.15
	total	$71.50
8-bit CPU Board		
8085 CPU (3 MHz)		$ 2.65
interrupt controller (8259A)		3.75
DMA controller (8237 + 8212 port)		8.80
timers (8253)		3.40
latch (8282)		2.95
transceiver (8286)		2.95
chip-selects (3 memory/3 peripherals)		1.75
wait-state generator		3.50
	total	$29.75

Note: An 8088-based 8-bit board price following a similar set of options comes to a total of $58.65.

Table 2: *Price comparisons of chips necessary to make 8- and 16-bit systems based on Intel microprocessors.*

The Intel 8086 family is growing. The 80186 expands on the basic workhorse 8086, and the 80286 (see the text box on page 144) adds multiuser capabilities. The 8088 has the same 16-bit internal architecture as the 8086, but it uses an external 8-bit bus. The same is true for the 80188 or iAPX 188 highly integrated 8-bit microprocessor. (Unless otherwise noted, all references to the 8086 and 80186 apply to the 8088 and 80188.) For detailed information about the architecture of the 8086, see *The 8086 Book* by Russell Rector and George Alexy (Osborne/McGraw Hill, 1980) and *The 8086 Primer* by Stephen P. Morse (Hayden, 1980).

System designers who are familiar with the 8086 will recognize the identical architectural scheme in the 80186. In some cases, hardware has been used to support functions formerly handled in microcode. Though the programmer's instructions are the same, the user will notice the enhanced performance of the 80186 (see table 3).

The instruction set, including the new instructions, is divided into those for data transfer, arithmetic operations, string manipulation, logicals/shifts/rotates, processor control, procedure entry and exit, and program-transfer operations. There are 101 instructions in the 80186 set (see table 4).

The registers within the 80186 are identical to those in the 8086, with the addition of the 16-bit relocation register, which locates the 256-byte peripheral control block in the 80186's 1-megabyte memory or 64K I/O (input/output) space. The control-block registers define the func-


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Relative 80186 Execution Times
8086 time divided by 80186 time (8-MHz clock rate)

Instruction	8086 (5 MHz)	8086-2 (8 MHz)	8086-1 (10 MHz)
Move Contents of Register to Memory	2.0 *to* 2.9	1.2 *to* 1.8	1.0 *to* 1.4
Add Contents of Memory to Register	2.0 *to* 2.9	1.2 *to* 1.8	1.0 *to* 1.4
Multiply 16-bit Register	>5.4	>3.4	>2.7
Divide 16-bit Register	>6.1	>3.8	>3.0
Multiple (4-bits) Shift/Rotate Memory	3.1 *to* 3.7	1.95 *to* 2.3	1.6 *to* 1.8
Conditional Jump	1.9	1.2	1.0
Block Move (100 bytes)	3.4	2.1	1.7

Table 3: *Comparison of execution speeds of 8086 microprocessors to those of the 80186.*

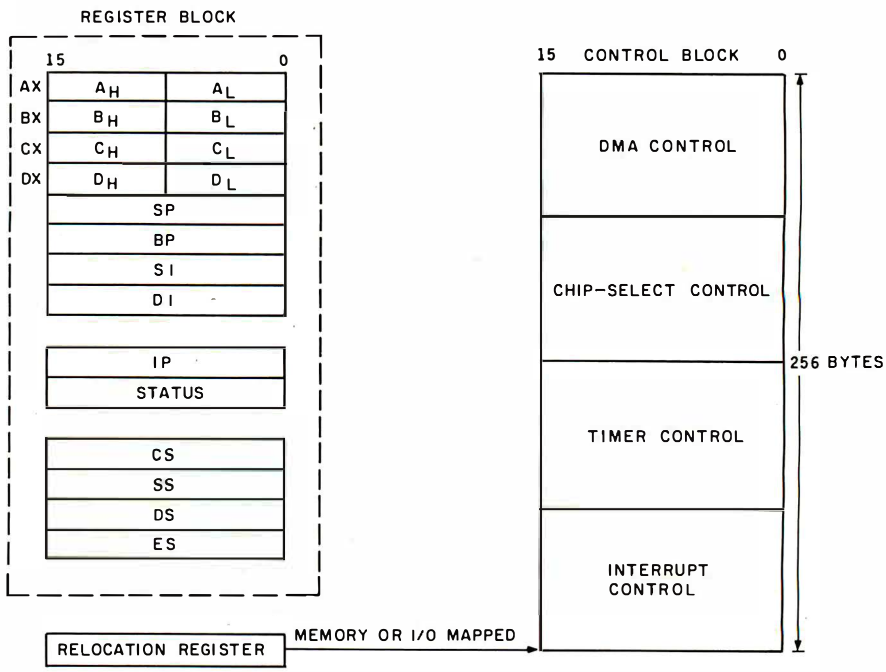


Figure 2: *The 80186 register file. Each of the four segment registers—CS, SS, DS and ES—defines a 64K-byte area of memory. There are four general-purpose registers: AX, BX, CX, and DX. The pointer and index registers are stack pointer (SP), base pointer (BP), source index (SI), and destination index (DI). IP is the instruction pointer.*

tions of the on-chip timers, DMA support, interrupt controllers, and chip-select logic (see figure 2).

Enhanced CPU

Several enhancements have been made to the 80186's CPU to reduce the number of instructions it needs to carry out a task and to increase the overall processing speed. The multiplier portion has been augmented with additional parallel hardware to provide a fivefold to sixfold improvement in executing multiplication and division instructions over the standard 5-MHz 8086.

Using its own dedicated hardware adder, the bus-interface unit (BIU) calculates the effective addresses of operands and instructions in parallel with the execution unit (EU). Formerly, this task was done in microcode using the adder that resides in the arithmetic and logic unit (ALU).



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Data-Transfer Instructions	
GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSH(X)	Push user-specified value
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

Processor Control Instructions	
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for TEST pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation

String Instructions	
MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/PREZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

Arithmetic Instructions	
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

Table 4: *The 80186 instruction set. The 80186 instructions not found in the 8086 instruction set are highlighted.* *Table 4 continues on page 139.*

Shift/Rotate/Logical Instructions	
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
High-Level Instructions	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure text
BOUND	Detect values outside prescribed range

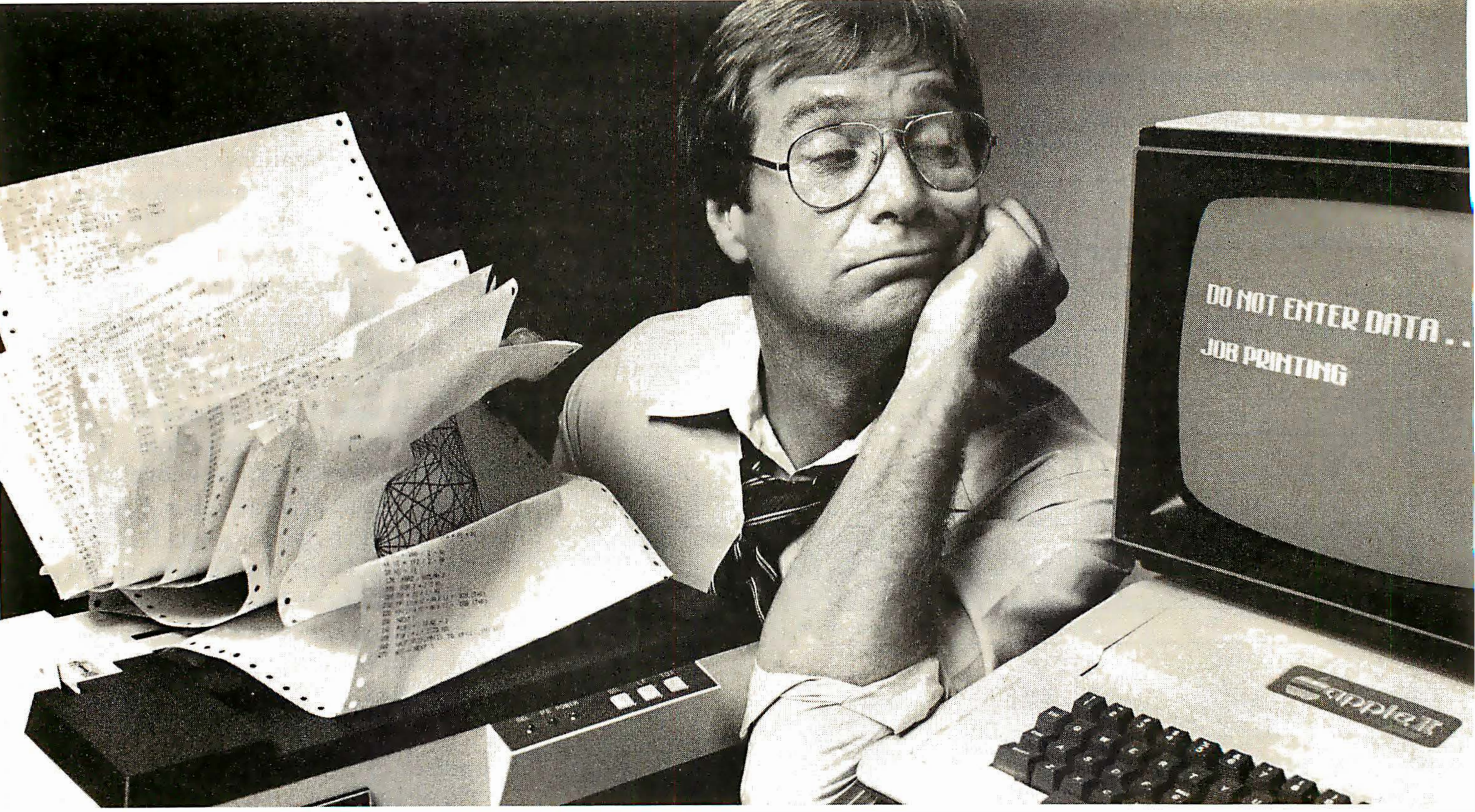
Additional hardware offers the programmer streamlined string-manipulation operations. Previously, the Repeat Prefix to Move instruction on the 8086 caused a delay for each byte that was moved because a microcoded subroutine had to be executed to decrement the CX register and check the status flags for "end of move." The extra hardware on the 80186 eliminates this overhead by performing these operations in parallel. As a result, string-move operations occur at nearly bus bandwidth (2 megabytes per second).

Bit-manipulation instructions such as Shift and Rotate have also been enhanced by means of additional hardware. Now both operate at a rate of 1 bit per clock.

Superset of Instructions

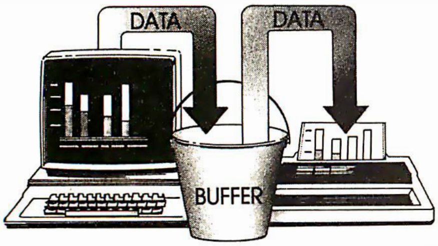
The 80186 adds additional instructions to those of the 8086. The Block I/O Move instruction is similar to the existing 8086 string instructions but allows the source or destination to be in the I/O space rather than in memory. If Block I/O Move is used with the repeat prefix, the number of words or bytes specified by the CX register is moved. The result is a very high transfer rate (4 megabytes per

Program-Transfer Instructions			
CONDITIONAL TRANSFERS		UNCONDITIONAL TRANSFERS	
JAJNBE	Jump if above not below nor equal	CALL	Call procedure
JA/JNB	Jump if above or equal not below	RET	Return from procedure
JB/JNAE	Jump if below not above nor equal	JMP	Jump
JBEJNA	Jump if below or equal not above		
JC	Jump if carry	ITERATION CONTROLS	
JE/JZ	Jump if equal/zero		
JG/JNLE	Jump if greater/not less nor equal	LOOP	Loop
JGE/JNL	Jump if greater or equal/not less	LOOPE/LOOPZ	Loop if equal/zero
		LOOPNE/LOOPNZ	Loop if not equal/not zero
JLE/JNG	Jump if less or equal/not greater	JCXZ	Jump if register CX = 0
JNC	Jump if not carry		
JNE/JNZ	Jump if not equal/not zero	INTERRUPTS	
JNO	Jump if not overflow		
JNP/JPO	Jump if not parity/parity odd	INT	Interrupt
JNS	Jump if not sign	INTO	Interrupt if overflow
JO	Jump if overflow	IRET	Interrupt return
JP/JPE	Jump if parity/parity even		
JS	Jump if sign		



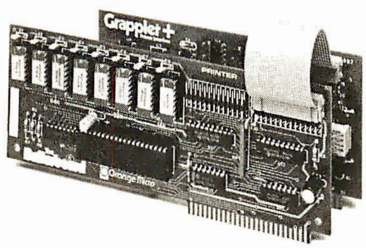
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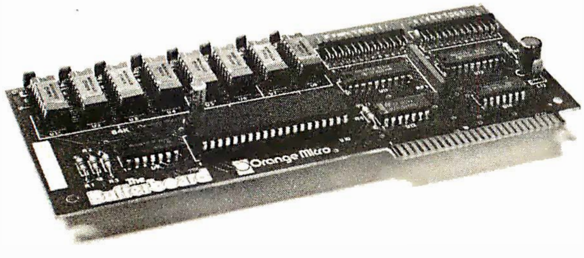
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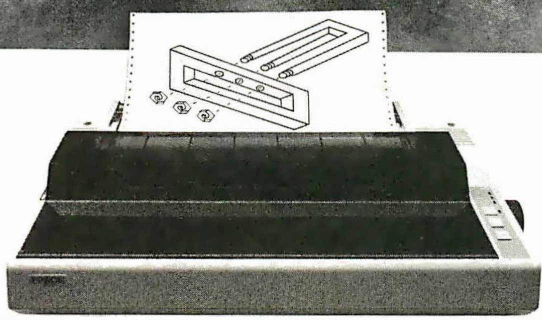
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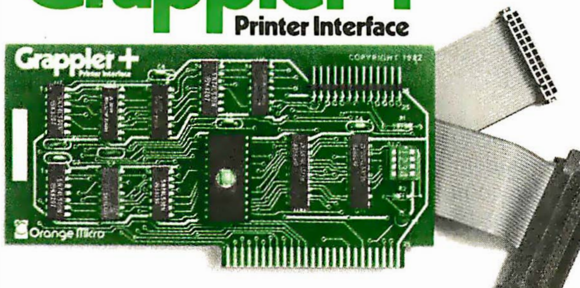
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second) because no op codes are fetched during the operation.

To support block-structured, high-level-language programs, Enter Procedure and Leave Procedure instructions are included. The Enter instruction performs the calling sequence for a high-level language, flushes the register set, and sets up the segment pointer registers as well as performs the other necessary "housekeeping" tasks. The Leave instruction, on the other hand, restores the 80186 to its state prior to entering the procedure. Normally, such operations would be done using assembly-language subroutines. In that case, the operations are performed with microcode for increased throughput.

Instead of using an internal register to temporarily store constants during a routine, the new Push Immediate instruction lets the user put a signed 8- or 16-bit value directly on top of the stack.

Numeric calculations are faster with "immediate" instructions, too. The two Multiply Fast instructions (one for signed 16-bit, the other for extended 8-bit values) work with immediate values. These instructions take one operand from the immediate field of the instruction itself and the other from either a memory or a register. In both cases, the values are "latched" by the new streamlined multiplier array for fast processing. These new instructions are very handy and were specifically designed for array index calculations in high-level languages.

Array handling is further enhanced by a Bound instruction that checks to see that the bounds of an array index value have not been exceeded. The index to be checked is kept in a register, and the upper and lower bounds are stored in a two-word block that is pointed to by the instruction's effective operand address. If the index is out of bounds, a "trap" is generated that vectors instruction execution to a known memory location.

Immediate Shift and Rotate instructions speed bit manipulations. In addition to the 3-bit field for determining left or right movement, an additional byte specifies the number of bits to be shifted or rotated; this eliminates the need to use a loop to perform that same function.

Finally, the contents of the AX, BX, CX, SP, BP, SI, and DI registers can be pushed onto the stack with a single Push All instruction. Similarly, they can be popped off with the Pop All instruction. Again, this instruction eliminates the use of slow assembly-language subroutines when you're servicing interrupts and subroutine calls. Another enhancement in the 80186 is its ability to generate an error interrupt when the 80186 attempts to execute an illegal instruction op code.

Interrupt Controller

The on-chip interrupt controller can handle eight prioritized, vectored interrupt sources. Internal interrupt sources are the counter/timer unit and the two DMA channels, which can be selectively disabled via bits in

Text continued on page 148

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The 80286

Today's microcomputer systems are capable of serving many users and simultaneously running a variety of programs. These multiuser, multitasking systems require high-performance processing, a large memory space, efficient addressing, and an effective means to protect system software from inadvertent user mishandling. In addition, each user's programs and data must be protected so that another user's program cannot "write" over them. Isolating both system software and user software requires effective hardware-supported protection.

Multiuser and multitasking systems are not new concepts; minicomputers have offered both of these features for years. But the demand for such microcomputer systems is a relatively recent development. To date, no microprocessor exists that has built-in memory management and protection or the ability to efficiently address a gigabyte (2^{30}) of virtual memory. In that regard alone, the 80286 or iAPX 286 sets a precedent. The capabilities of the 80286 along with its high performance make for a rare combination indeed.

Moreover, the 80286 lets users take advantage of a large base of existing software. Underlying several new instructions aimed at streamlining high-level-language coding and operating system execution (see table 1) is the familiar instruction set of Intel's popular iAPX 86/88 (8086/8088) family. The 80286 is compatible with the software that exists for these other processors. As a result, users can now achieve an immediate increase in a system's performance simply by making design changes in the new 80286 hardware and using the existing software or the growing base of third-party software written for the 8086. Later, programs may be moved to run in a memory management and protection environment. Further system enhancements or completely new products can be produced with no hardware changes.

Many logic elements, and therefore many active devices such as transistors, are required to handle all the functions that the 80286 includes. The 8086 microprocessor contains approximately 29,000 transistors; the 80286, in comparison, contains 130,000.

Organized in Four Pipelined, Functional Units

In most microprocessors, a complete sequence of instruction fetching, decoding, and execution must take place before the next instruction can be fetched. In the 80286, these operations are carried out in parallel, resulting in an overall increase in performance without the use of faster memory chips, which would be needed if performance were enhanced simply by speeding up the clock rate.

Pipelined architecture permits the CPU to detect invalid op codes well in advance of their execution, another advantage. The 80286, for example, has time to perform the memory-protection functions without degrading the processing performance or restricting memory access.

Pipelining in the 80286 is separated into four logical units: bus, address, instruction, and execution.

The bus unit provides a demultiplexed bus interface between the processor, system memory, and external I/O subsystems. It monitors bus-cycle requests from other processors or the chip's own address unit, and when there is a pause, the bus unit's "prefetcher" grabs the next instruction and places it in a "code queue." Here, instructions are available for immediate access by the chip's instruction unit.

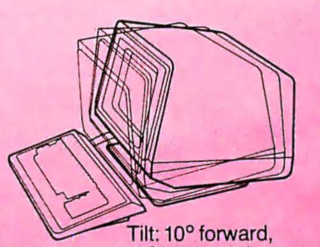
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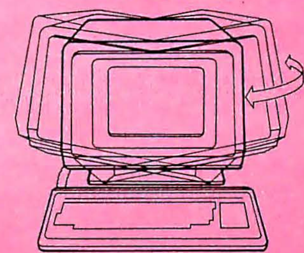
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Text box continued:

The instruction unit receives data at a rate of 1 byte per clock cycle, decodes and formats complete instructions, and places them in its "instruction queue" to await action by the execution unit.

The execution unit contains the CPU registers, the arithmetic and logic unit (ALU), and the microcode firmware for the CPU in read-only memory (ROM). Instructions are executed under the control of the ROM's internal microinstruction sequence. When it nears completion of the sequence, the ROM signals the execution unit to take the next instruction out of the instruction queue. This treadmill-like process keeps the execution unit operating very efficiently.

Finally, the address unit performs the memory-management and protection function by translating virtual addresses to physical addresses and checking protection rights, all simultaneously. This unit maintains its own explicit cache containing all address mapping and protection information (base address, boundary limit, and the access rights) for the virtual-memory segments currently selected by the executing task. By storing this information in its own on-chip cache, the address unit does not need to retrieve it from memory-based address-translation tables. Therefore it can perform all functions in a single clock cycle.

By operating in parallel, these units enable the 80286 to manage virtual memory and protect the memory without degrading system throughput.

Memory and User Protection Via Tight Access Control

The 80286's memory-management and protection mechanism is an integral part of the architecture. It is physically integrated on the same silicon die as the rest of the CPU, so the protection of system and user code and data does not require extensive system software or add-on memory-management units (MMU). Such an approach has many advantages. It is more reliable, easier to implement, and faster. It also reduces software overhead.

The 80286 protects users from one another and the system software from its users. Each user has up to one gigabyte of virtual address space that may be split between shared and private use. Common data, files, and library routines are typically stored in shared space. Each user's private space is accessible only to him.

Each user's large virtual address space contains his "view" of the operating system. Because all users share the operating system, it is usually stored in the shared address space. Putting the operating system within the direct-address space of each user means that access to operating system routines is simpler and faster. Within each user's virtual-memory space are up to four hierarchical protection levels, so that even within his own space a user's application-program tasks can be guarded from improper access to the operating system.

The 80286's hardware supports this four-level protection hierarchy. Should a task attempt to access an address without right of access, the CPU will prevent it and then signal that a fault has occurred. In addition to providing more protection than usual, this architecture is more flexible and efficient than the typical two-level schemes minicomputers and other microprocessors use. It offers the user more flexibility, configurability, and reliability for the system software. These features are especially important for reprogrammable business and office systems applications, which will typically have many concurrent users.

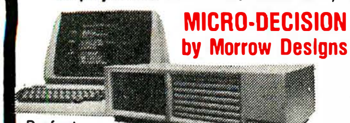
Software Compatibility

Like the 80186, the 80286's instruction set is a superset of the 8086/8088 set, and its software is compatible with them. This provides a real upgrade path from the 8086 and 8088 to the 80286, and users can take advantage of the wealth of existing 8086/8088 software to get a jump on the development process. Current 8086 users will be able to enhance system performance immediately simply by changing the CPU subsystem hardware for the 80286. They can also modify their software to take advantage of the 80286's new instructions for further performance enhancements.

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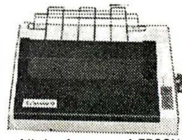
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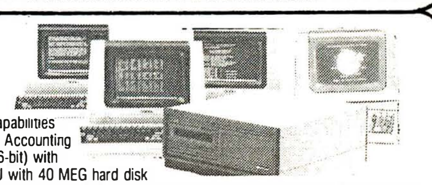


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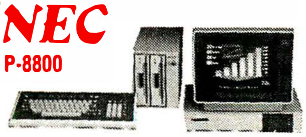
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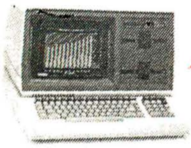
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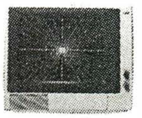
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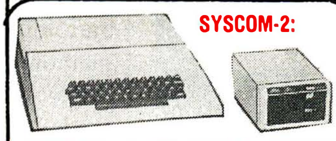
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the interrupt control register. The controller resolves simultaneous requests based on predefined priorities. The higher-priority interrupt will cause servicing to cease on a lower one. Interrupt control can be expanded externally by cascading 8259A programmable interrupt control chips or 80130s to the 80186 via dual-function interrupt pins provided for that configuration. Five external interrupt input pins—four plus nonmaskable interrupt (NMI) input—can be programmed to respond to either levels or edges.

Chip-Select and Ready Functions

All CPU subsystems must interface with an array of memory and peripheral chips. In other typical microcomputer systems, external random logic or VLSI components must be used to translate microprocessor output states into appropriate memory or peripheral chip-select signals. Because the 80186 has built-in chip-select generation circuitry, in many cases no additional external logic is needed to interface with memory I/O subsystems.

Users can program in a selection of wait states (0 to 3 states) to accommodate memory or peripheral chips with a variety of access-time characteristics. Where the 80186's internal wait-state selections are not sufficiently long, external wait-state generators can be ORed to the internal "read" circuitry.

Memory can be divided into three separate sections—upper, middle, and lower. The upper- and lower-memory sections are selected by a single select line. The middle-memory section is selected by four select lines, so it can be further divided into four equally sized subsections. Memory-block sizes may be programmed for 2K, 4K, 8K, 16K, 64K, or 128K bytes. The upper and lower sections can be programmed for those sizes as well as for 1K and 256K bytes. Thus if sixteen 64K by 1-bit chips are used in the upper segment, that select line would be programmed for 128K bytes.

Peripherals are selected by as many as 7 signal lines. Each line is active for

a 128-byte memory segment (the peripheral block). As many as 7 of these segments can be grouped contiguously, and the entire 996-byte set of blocks may be located on any 1K-byte boundary. Two control registers, the base address register (PACS) and the mode register (MPCS), govern the function of the peripheral select lines.

Users can select 5 or 7 lines. The 5-line mode is convenient for 8-bit peripherals because the remaining 2 lines can be used as latches for the A_1 and A_2 address lines. That way, the 80186 can treat the address lines as if they were 16-bit peripherals located on even-address boundaries. Then no external logic or compensatory software routines are necessary.

Direct Memory Access Support

When blocks of data are to be moved from one memory location to another, or from memory to an I/O device, or even from one I/O device to another, it is inefficient for the CPU to handle this data 1 byte or word at a time. DMA makes these kinds of transfers much more efficient by limiting the CPU's involvement. The 80186 supports two such DMA channels, each capable of transferring data at a rate of 2 megabytes per second.

Each DMA channel maintains two 20-bit source and destination hardware pointers that can be incremented or decremented after each data transfer. Each transfer typically consumes only two bus cycles, one to fetch the data and the other to store it in its new location.

Each channel is associated with a control register that specifies word or byte transfers and states whether an interrupt must be generated upon completion. The control register also specifies automatic incrementing (or decrementing) of source or destination registers, the channel priority, and the starting and stopping of the transfer itself.

Programmable Counter/Timers

Many microcomputer applications depend on timing or counting external events, generating nonrepetitive waveforms, and combinations of

counting and timing. To meet these needs, CPU subsystems commonly have one or more timer/counters implemented with external circuitry. The 80186's three timer/counters eliminate the need for the external circuits.

Two of the 80186's 16-bit timer/counters are designed to interface to external circuits, and the third is for internal operations. All three have several programmable options that are selected by a set of three 16-bit control registers. In addition, each timer has its own maximum-count register (timers 0 and 1 have two). Each timer/counter can be programmed to halt or continue when it reaches the specified maximum count. Users can program the counter to issue an interrupt upon reaching maximum count and then either continue or reset and then continue. The various functions are programmed via the mode-control register.

On-Chip System Clock

An on-chip system clock is implemented by a crystal oscillator and divide-by-two logic. By connecting a 16-MHz crystal to the external pins, an 8-MHz system clock signal is produced. This signal is used internally to control the synchronous execution of instructions and operations. One of the 80186 pins provides an external clock signal and can be used to synchronize external circuits to the internal clock.

Interface with Support Chips

The 80186 interfaces with Intel's full line of peripheral control components. Like the 8086, the 80186 communicates with and controls those components via the system bus. The 80186 emits the same local bus handshake signals as the 8086.

Memory control, data communication, and display control components as well as VLSI controllers are available for the graphics display, disk drive, and keyboard interface. Controllers for the serial and parallel, asynchronous and synchronous data-communications protocols are also available.

Systems integrators can choose from several operating systems, among them iRMX-86, CP/M-86, and MS-DOS. Compatible operating system software for the above is available from Intel for the 8086, 8088, and 80186.

Many applications programs have been written for 8086- and 8088-based systems. The list is growing significantly as a result of IBM's introduction of the 8088-based Personal Computer.

For users who already have developed software for their 8086- or 8088-based machines, the 80186 offers an additional advantage: programs written for the 8086 and 8088 will run on the 80186 without modification. The 10 new instructions can replace longer subroutines, making programs more compact.

Conclusion

The 80186 replaces as many as 20 chips in an 8/16-bit microcomputer at about half the cost of the 8086/8088 kit of parts. It also has twice the capability of the standard 8086/8088 running at the standard 5-MHz clock rate. The 80186 will pave the way for the next generation of microcomputers to be both less expensive and more powerful. ■

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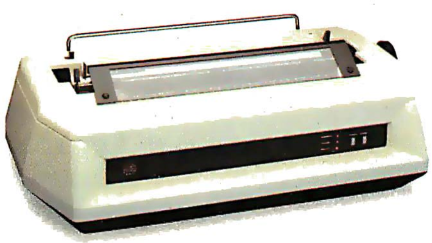
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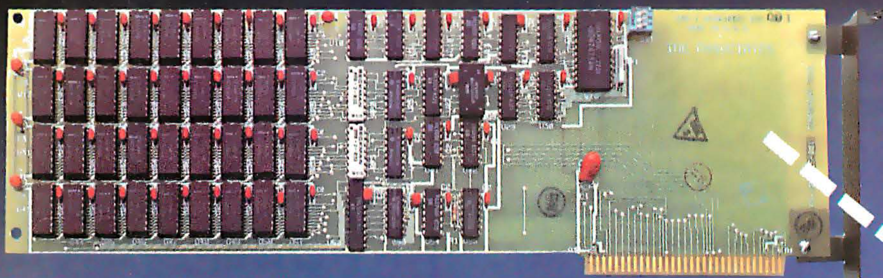
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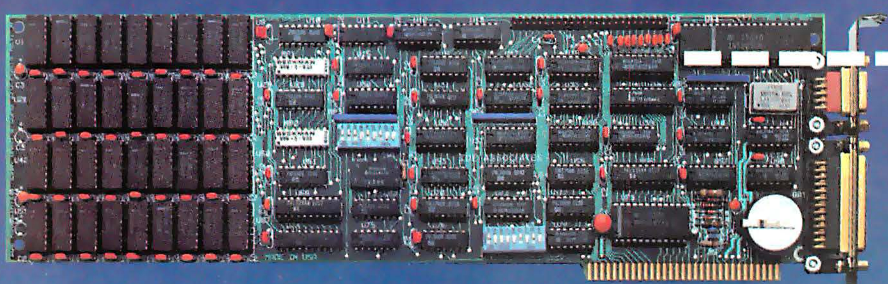
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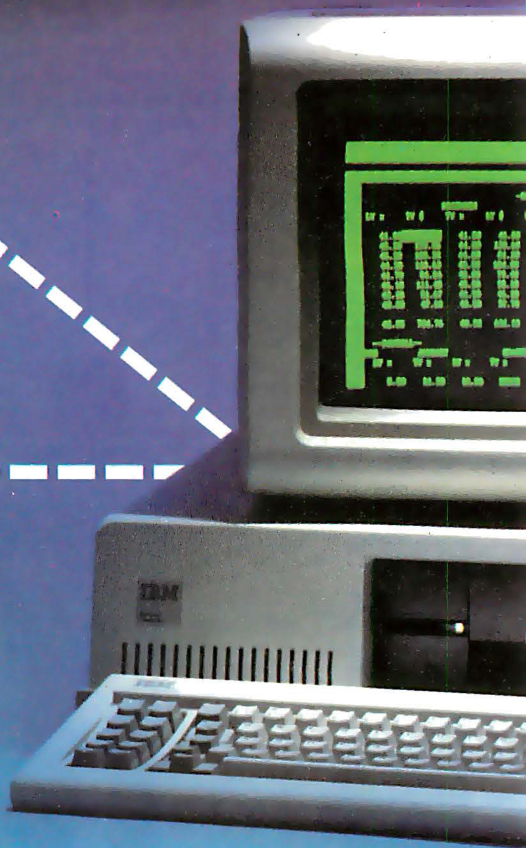
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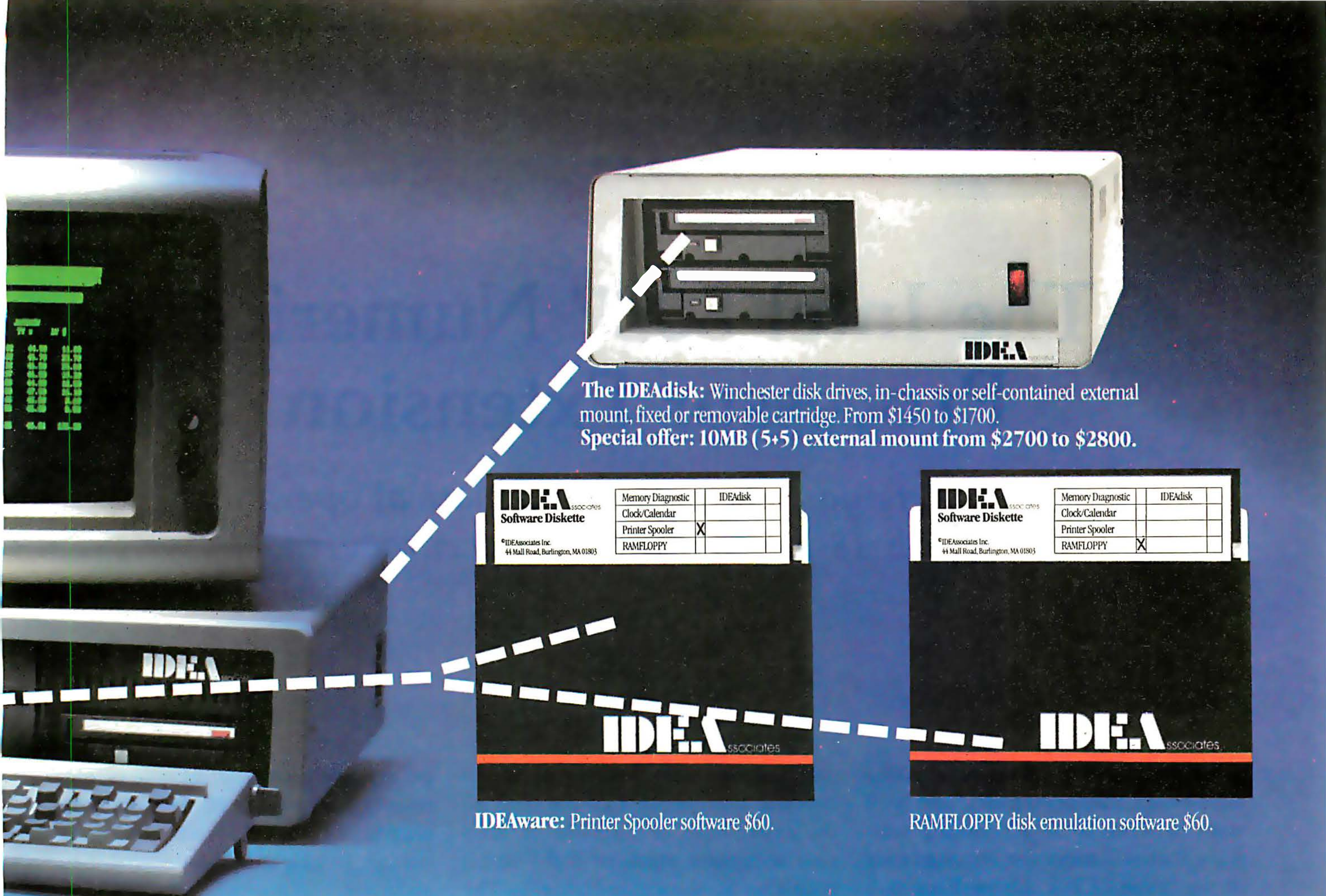
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The Intel 8087 Numerics Processor Extension

This chip lets you perform mathematical operations with 18-decimal digits of accuracy.

R. B. Simington
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So you have a shiny new 8086/8088-based microcomputer and you want to write some accounting software that will meet the requirements of the fussiest CPA. Or perhaps you want to write some code to control your latest robotics experiment and you need to do some critical number-crunching with very accurate results. Let me introduce you to the Intel 8087 Numerics Processor Extension (NPX).

The 8087 NPX is a chip that will give you, regardless of your mathematical skill, the ability to write code that will perform mathematical operations with guaranteed accuracy of 18-decimal digits. To make things even easier, the NPX, known as a coprocessor, is easy to interface to a host processor (8086 or 8088). When you add an NPX to one of its host processors, you have a Numeric Data Processor (NDP).

Registers

The 8087, due to its special status as a coprocessor, combines with the architecture of the host processor to produce a processor that contains all the capabilities of an 8086 or 8088 plus a register stack of eight 80-bit registers, as shown in figure 1. The NDP also brings the ability to execute a set of 68 new floating-point-arithmetic instructions in addition to the extensive instruction set of the host alone. These 80-bit registers hold all the operands for the floating-point operations in a format called Temporary Real, which is capable of representing any whole number up to 2^{64} exactly. This 80-bit format is accurate enough to guarantee 18-decimal-digit accuracy.

You can think of the eight registers of the 8087 as a standard register set or use them as a classical stack. This arrangement allows you a great amount of flexibility in using these storage areas. You can use the registers as a stack, for example, to

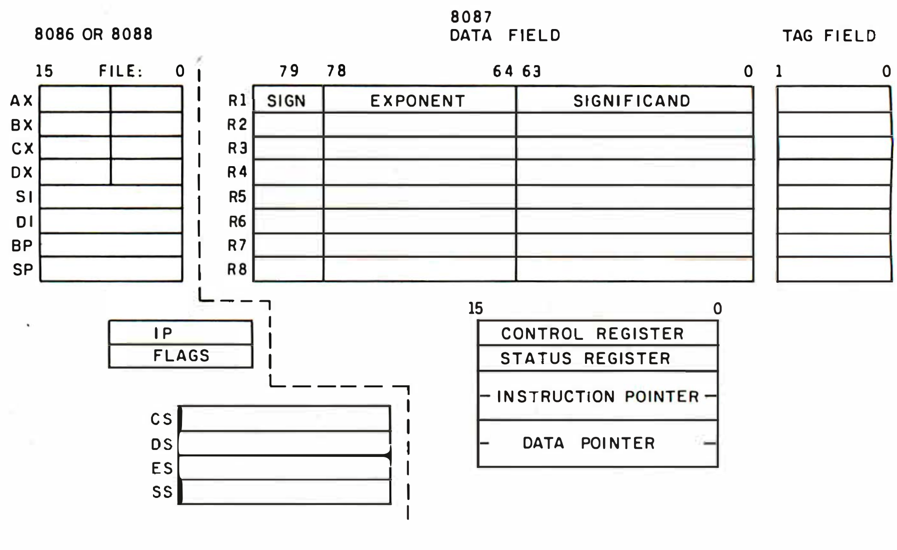


Figure 1: *The NDP register set of eight 80-bit registers.*

About the Author

Bob Simington is a curriculum developer for Intel's customer training department. He is responsible for the development of all microprocessor training curricula. His most recent assignment was to develop a course based on 16-bit personal computers.

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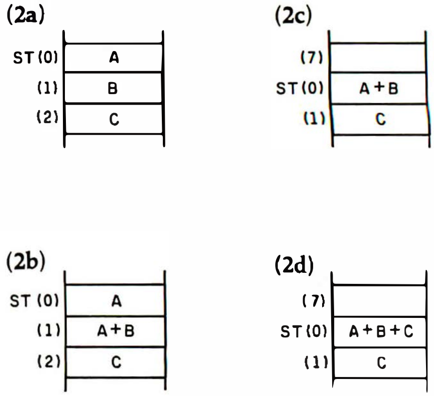


Figure 2: *The effects of instructions on the register stack.*

pass operands to a floating-point subroutine that expects to find its parameters in the 8087 register stack. The instruction set of the 8087 exploits this capability by allowing assembly-language instructions that use the stack top as one of the operands implicitly.

You can also treat these registers as a standard register set; the instruction set supports this use of the registers by allowing both operands to be specified explicitly for an operation. Look at the example in figure 2.

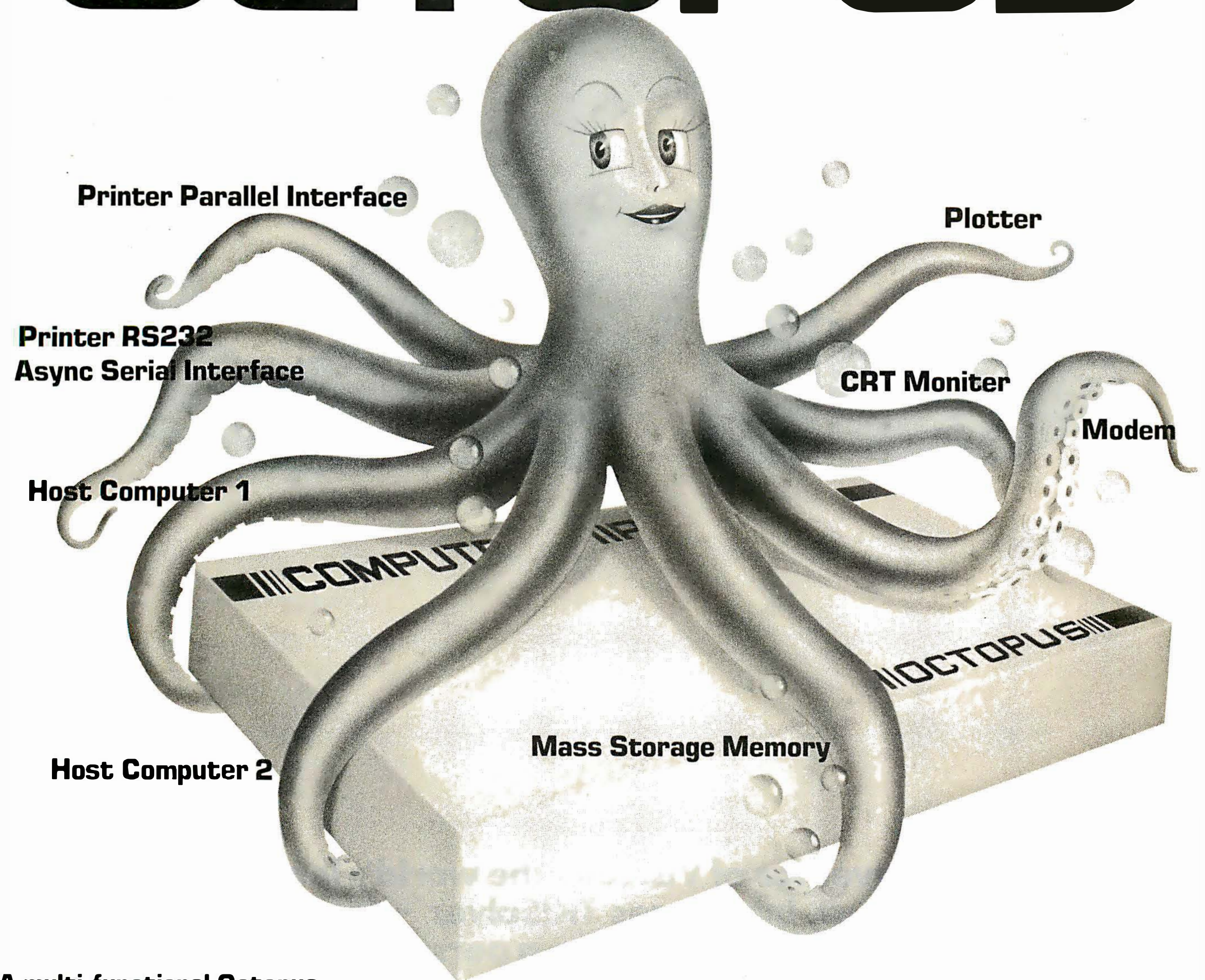
Your NPX stack contains the values A, B, and C, as shown in figure 2a. You can cause the value in the stack top to be added to the value in the next stack element (ST(1)), as shown in figure 2b, and then have the stack popped, so that the sum is the new stack top, as shown in figure 2c, with the one instruction FADD. This is the classical stack operation where none of the operands are specified. The same instruction could have been specified explicitly with the instruction FADDP ST(1),ST.

As another example, you could add the value that is in ST(1) to the value in the stack top and retain both values, as shown in figure 2d, with the instruction FADD ST,ST(1). All registers are addressed with respect to the current stack top. The Status Word of the 8087 contains a field that identifies the current stack-top status at all times.

Status Word

The Status Word, as its name implies, reflects the status of the NDP at

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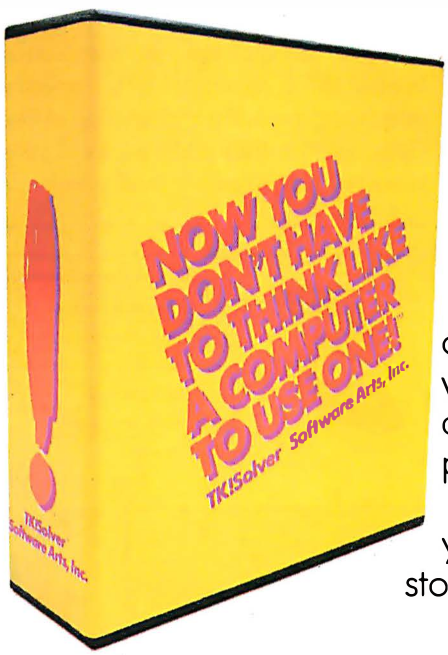
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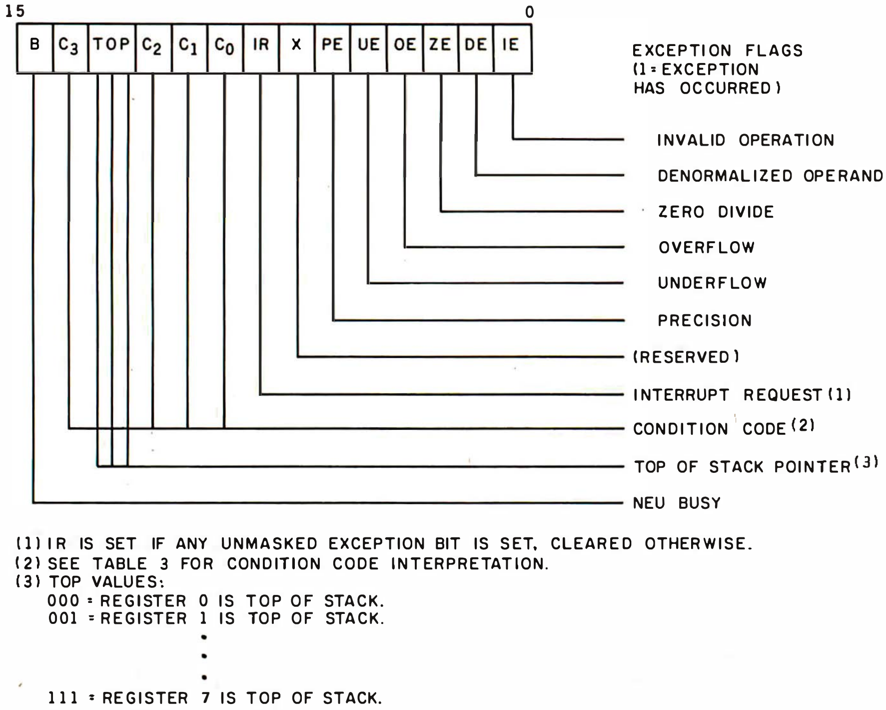


Figure 3: *The various fields of the Status Word.*

all times. The various fields of the Status Word are shown in figure 3.

The Busy bit indicates whether the 8087 is in the process of performing an operation at any given time. The 4 condition bits (C3 through C0) denote the result of a previous operation, and the host processor can examine them to determine if a branch should take place in the program. This is accomplished by storing the 8087's Status Word in memory and then causing the host processor to fetch and examine the condition codes.

Three of the bits of the Status Word, ST2 through ST0, specify which register is the current top of the stack. Notice that if the ST field contains 000, for example, and a value is pushed onto the NDP's stack, the ST field would decrement to 111. By the same token, if the ST field contains 000 and a value is popped from the stack, the ST field would increment to 001.

As it turns out, you really don't need to know which register is the current stack top, but this gives you some idea of what the bits mean. You *do* need to know the relative position of your various data elements on the stack, however, and keeping track of them is one of the jobs of the programmer.

All the remaining bits in the Status Word apply to exceptions (errors) and the way to handle them. Bits 0 through 5 signify whether the NDP detects an exception condition. Table 1 indicates the significance of these exceptions. Bit 7 is set to indicate whether the 8087 requests the host central processing unit to execute an interrupt-service routine in response to one of the exception conditions. It is possible for an exception condition to take place without an interrupt request if the programmer masks a particular exception (or group of exceptions). Generally, however, the NDP uses a collection of built-in default routines to handle most exceptions.

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C



Invalid Operation
- Attempt to load a register that is not empty
- Attempt to pop an operand from a register
- Operand is a NAN (not a number)
- Operands cause operation to be indeterminate (%, √– number

Denormalized Operand
- Attempt to use an operand that is not normalized

Zerodivide
- Attempt to divide by 0

Overflow
- Result too large for destination format

Underflow
- Result too small for destination format

Precision
- Result not exactly representable in destination format
- 8087 rounds result

Note: Exception bits are "sticky" and can be cleared only by the FCLEX (clear exceptions) instruction.

Table 1: *The significance of the exceptions.*

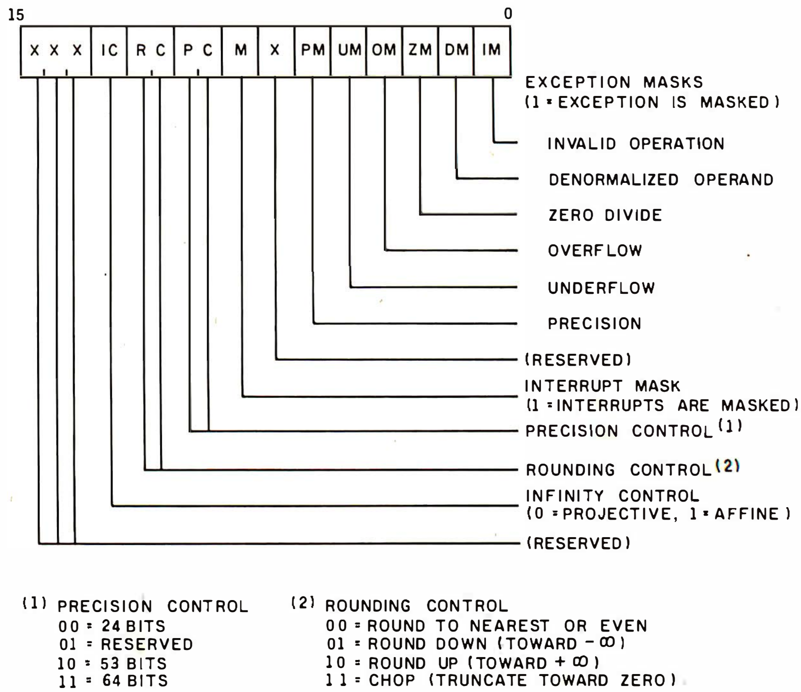


Figure 4: *The Control Word.*

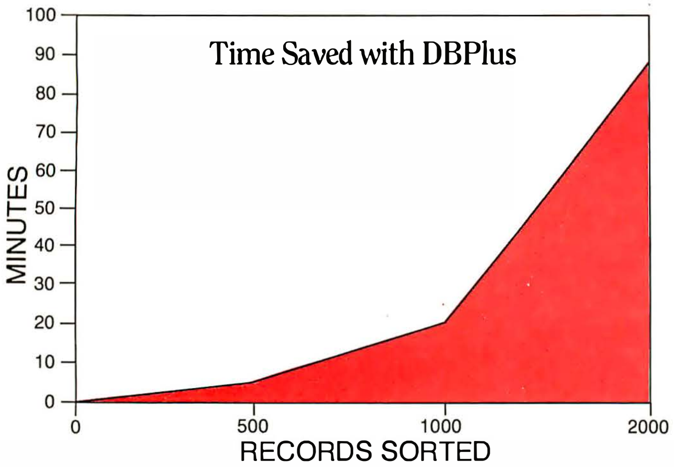
IEEE standard that specifies the NDP default routines. (See the text box on pages 174-175.) In other words, you can take responsibility for handling an exception condition or you can let the chip do it. To inform the NDP which exceptions it will handle and which ones you will handle, you use the Control Word.

Tag Word

Before we move to the Control Word, let's look at one other thing. How would the NDP know if we had tried to pop something from an empty register so that it could set the invalid operation flag? For that matter, how would it know if one of the operands was not a number? Well, the NDP stores a Tag Word that contains a 2-bit field for each of the eight registers, and which keeps track of the contents of each register and marks the contents as being Valid, Zero, Special (not a number, infinity, etc.), or Empty.

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Control Word

The Control Word is shown in figure 4. The least significant portion of the Control Word coincides with the least significant portion of the Status Word in that you set or clear these bits to mask or unmask (respectively) the exception conditions and to disable or enable the ability of the 8087 to interrupt the host processor. The Control Word also has bits that allow you to set the precision of the NDP to various levels. You should realize that there is no advantage to lowering the precision of the NDP in terms of execution speed. This capability exists only to allow the 8087 to more accurately emulate previous floating-point products that might be replaced by the 8087.

The next 2 bits in the Control Word set the rounding convention that the NPX uses. You can set the NPX to round up, round down, round to the nearest or even number, or to round toward zero.

Lastly, a bit in the Control Word selects the model of infinity for the NPX. Just think, philosophers argue whether infinity even exists and you get to define it in one of two different ways!

Simply put, the first method, known as the Affine closure mode, considers that there are numbers that are positively infinite and numbers that are negatively infinite. While this may seem reasonable, it can cause unexpected problems in calculations. For example, if we divide a number by the number X, and X is very, very small and positive, the result could be positive infinity. If X is very, very small but negative, the result could be negative infinity. In other words, you have two very different results.

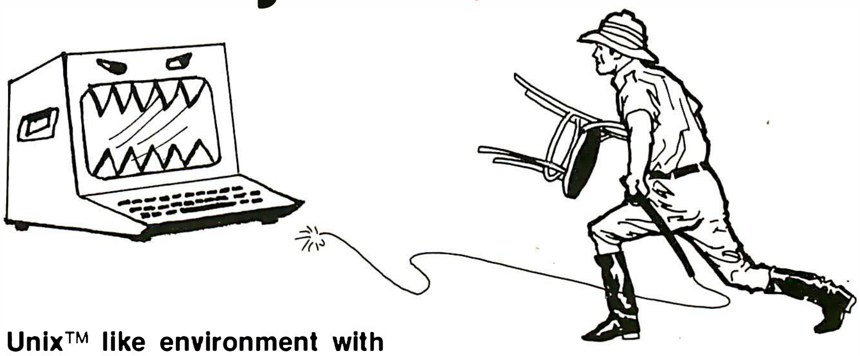
The Projective closure mode uses only one infinity. Although it is very large, it has no sign. This mode is the easiest to use and therefore is recommended.

Exception Pointers

If an exception does take place, and you have unmasked that particular exception flag, it would be nice to know a few things before you jump in and try to recover from your error. You would probably like to know

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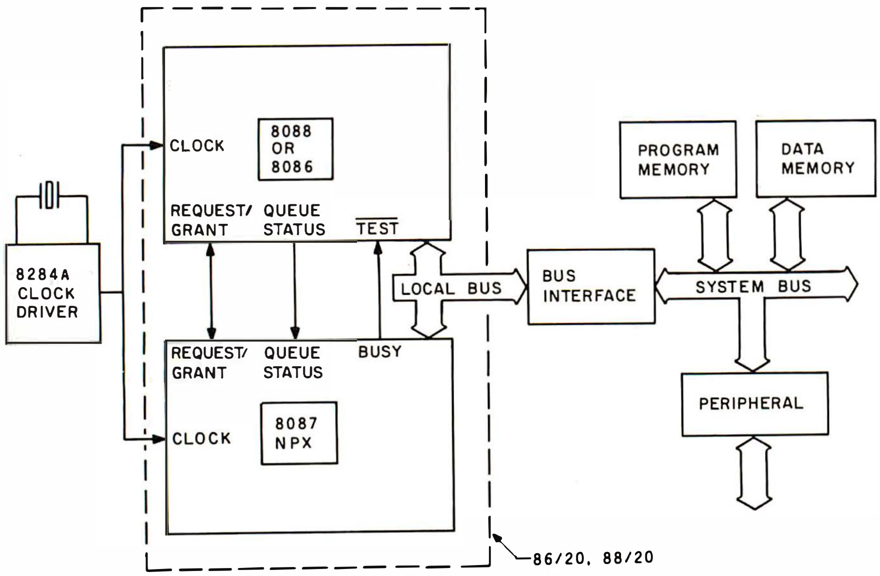


Figure 5: *The interface and communication lines.*

which instruction or op code caused your problem. It would also be nice if you could determine this instruction's address so that you might resume at that point when you have eliminated the cause of the problem. Also, if the instruction operated on data in memory, you might want to know where this data came from. The 8087 contains all this information in three registers that are collectively called the Exception Pointers. The operational details of these registers are beyond the scope of this article, but can be found in Intel technical documents.

Synchronization

The 8087 works in close harmony with its host. In order for this to take place, there must be some communication and synchronization between the two devices. The interface and communication lines are shown in figure 5.

When you add an 8087 to a host microprocessor, the host retains the responsibility of fetching the instructions from system memory. As the host fetches these instructions, the 8087 also captures them and puts them in a queue—just as the host processor does. The answer to how the 8087 knows whether to emulate the 6-byte queue of the 8086 or the 4-byte queue of the 8088 is quite simple.

Whenever the processor is reset, the host processor goes to absolute address 0FFFF0 hexadecimal to begin fetching instructions. The 8088 always fetches a byte from this location because the 8088's data bus is a byte wide. The 8086, however, can fetch its instructions one word at a time. So when it goes to address 0FFFF0 to fetch its first instruction, it fetches a word instead of a byte. To accomplish this, the 8086 issues a signal called Byte High Enable (BHE/). The 8087 simply looks to see if its host generates a BHE/ signal when it performs its first op-code fetch after a reset. The presence or absence of the signal determines if it is connected to an 8088 or an 8086, and it then emulates the correct queue.

In order for the 8087 to work in close harmony with its host, there must be some synchronization between the two devices.

All 8087 instructions have a unique 5-bit prefix called the Escape prefix (11011). When the host fetches an op code with this prefix, it is placed in the queue as any other instruction would be. The 8087 captures the same op code as it is fetched by the host and places the op code in its own queue. As this op code moves through the queue of the host processor, its movement must be emulated by the NPX queue as well. The mechanism that is set up to do this is the first of the three types of synchronization signals that are shared by the host and the NPX. The host has two lines called the Queue Status lines (QS0 and QS1). They allow an external device such as a coprocessor to emulate its queue. When this floating-point instruction finally makes its way through the queue, the host determines that it is an instruction for the NPX rather than for itself.

Once the host has determined that the instruction is an NPX instruction, it looks at the instruction to see if the NPX will need to access memory in the execution of the instruction either to fetch (read) an operand from memory or to store (write) an operand to memory. If it sees that this is the case, the host will calculate the address of the operand and perform a *dummy read*. By performing this dummy-read operation, the host can supply the NPX with the address of the memory operand. The host generates the address and even issues the strobe signals, but it ignores the data that is read from the addressed location.

The NPX, on the other hand, captures the address that the host generates. Then, depending on whether the NPX needs the data that is read or whether it needs the address so that it can write a result in memory after it finishes its instruction, the NPX captures the data or ignores it. Even if the data were required by the NPX to execute the instruction at hand, the dummy read will result in only one byte or one word of data. Typically, the NPX will be working with data types that are 4, 8, or even 10 bytes in length. This means that the 8087 will have to perform additional memory-read cycles in order to access the remainder of its operand. Because the 8087 shares the host processor's buses, it must have a way of informing the host that it wishes to use them.

The mechanism to do this is the

Text continued on page 170

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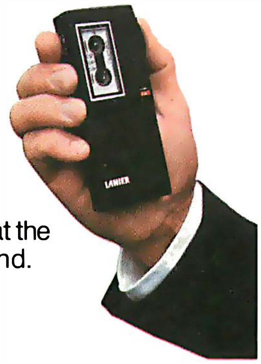
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4K byte graphics display memory
5-slot expansion bus

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Upper- and lower-case letters

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same used by any potential bus master to borrow bus cycles from the host. This line is the Request/Grant line (RQ/GT), and it is the method that the host uses to implement the HOLD and HLDA (hold and hold acknowledge) functions. When the NPX wants to use the buses, it toggles the RQ/GT line low. The host latches this request and, when it is done with the buses, three-states its buses and signifies to the requesting device that it can have them by toggling the same line low itself.

The NPX takes over the buses at this point and generates all the signals (address and control) to access the operand. It signifies when it is finished by once again toggling the RQ/GT line low. In the case where the NPX needs the address generated during the dummy read to store a result, it simply executes its instruction, saving the address until it has completed the execution and then requests the bus so that it can perform the memory-write cycles required to put the result in the proper memory location.

In some cases, the host can continue to fetch and execute instructions (with the NPX emulating its queue) while the 8087 is busily crunching numbers. There may be a situation, however, when this cannot take place. For example, we have two instructions in a program, the first of which causes the NPX to operate on a variable and to store the result in memory. If the second instruction causes the host to use this result, we must not allow the host to execute the second instruction and to access the variable until the 8087 has written the proper value in the variable location.

To accomplish this, we precede the instruction intended for the host with a WAIT instruction. The WAIT instruction causes the host to look at its TEST pin. The TEST pin, as you can see in figure 5, ties to the BUSY line of the NPX. Whenever the NPX is busy, the BUSY line is high and the TEST pin on the host is high. When the host executes the WAIT instruction, it cannot go on to the next instruction until its TEST pin goes low.

Another case where you would not want the host to go off blindly is when you have more than one floating-point instruction back to back. In this situation, the host would like to be more than obliging by performing all the dummy reads in the world just so that it can get to an instruction that it can execute. The problem is that the 8087 queue has to be in sync with the host, and if the host just gobbles its way through a series of floating-point instructions, ignoring them as it is designed to, the devices will never be able to regain sync. You can solve this problem simply by adding a WAIT instruction in front of all floating-point instructions.

Listing 1: *An application of the 8087 using an Intellec Series III Microcomputer Development System and Intel's 8087 software emulator.*

```
SERIES-III 8086/8087/8088 MACRO ASSEMBLER V1.0 ASSEMBLY OF MODULE PYTHAGORUS
OBJECT MODULE PLACED IN :F1:EUCLID.OBJ
NO INVOCATION LINE CONTROLS


LOC  OBJ                 LINE     SOURCE

                           1 +1   $SYMBOLS DEBUG
                           2
                           3              NAME PYTHAGORUS
                           4
                           5              EXTRN   INIT87:FAR
                           6
----                       7      TRIANGLE        STRUC
0000                       8              BASE    DD      ?       ; The DD memory allocation allows
0004                       9              ALT     DD      ?       ; enough space for the variables
0008                      10              HYP     DD      ?       ; to be defined in the SHORT REAL
000C                      11              AREA    DD      ?       ; format.
----                      12      TRIANGLE        ENDS
                          13
----                      14      DATA    SEGMENT PUBLIC  'DATA'
                          15
0000 ????????             16      RIGHT   TRIANGLE        <>      ;We will assume that these
0004 ????????
0008 ????????
000C ????????
                          17                                      ;variables are initialized by
                          18                                      ;another program.
0010 3E03                 19      CONTROL_87      DW      033EH
                          20
                          21      ; This is the default control word which masks all exception except
                          22      ; INVALID OP, leaves the INTERRUPTS UNMASKED, ROUNDS TO NEAREST OR EVEN,
                          23      ; and sets the INFINITY CONTROL to PROJECTIVE.
                          24
                          25
----                      26      DATA    ENDS
                          27
                          28
----                      29      STACK   SEGMENT STACK   'STACK'
                          30
0000 (100                 31              DW      100 DUP(?)
     ????
     )
```

Application

The following application of the 8087 uses an Intellec Series III Microcomputer Development System and Intel's 8087 software emulator (see listing 1). The program takes the base and altitude of a right triangle, which are stored in memory as two fields of a structure called TRIANGLE, and uses this data to calculate the area of the triangle and the length of its hypotenuse. Notice that I define the fields of the structure as double words (DD). This allows me to define the variables in the Short Real format. I will discuss the program using both the listing and a chart in figure 6 that tracks the status of the NPX's stack as references. When I refer to the chart, I use lowercase letters in parentheses.

The procedure INIT87, which I reference on line 42, is in the 8087 emulator and prepares the environment. The FLDCW instruction on line 46 causes the Control Word, which is stored in memory at a location symbolically called CONTROL-87, to be loaded into the 8087. The function of the Control Word is explained beginning with line 21.

Notice that all the floating-point instructions are preceded by a hexadecimal 9B op code. This is the WAIT op code that is inserted automatically by the assembler. The first thing that I must do is set up the stack so that I can perform my calculations. The instructions on lines 50 through 53 perform this. FLD1 puts the number 1.0 on the top of my stack (figure 6a). FADD ST,ST(0) causes the value at ST(0), which is my stack top, to be added to the stack top.

The result of this instruction is to multiply the stack top by 2 (figure 6b). The FLD instructions cause the 8087 to load the contents of the specified memory locations, which are considered to be in the Real format, on the stack (figure 6c). In the process of loading these values, they are transformed into the Temporary Real format. Notice that because the host processor calculates all the operand addresses, I can use any of the addressing modes of the host. The 8086 and 8088 processors are capable of 24 powerful addressing modes. In this case, I am accessing a field of a structure.

Next, I calculate the area of the triangle. The instructions that do this are on lines 57 through 60. The FLD ST(1) instruction causes the contents of the current ST(1) register to be duplicated on the top of my stack (figure 6d), and the FMUL ST,ST(1) instruction puts the BASE X ALT in the stack top (figure 6e). FDIV ST,ST(3) divides the stack top by the 2.0 that I have saved on the stack (figure 6f), and the FSTP causes the result, which is equal to the area of the triangle, to be popped into the ap-

Listing 1 continued:

```
00C8                     32      T_O_S   LABEL    WORD
                         33
----                     34      STACK   ENDS
                         35
                         36 +1   $EJECT
----                     37      CODE    SEGMENT  PUBLIC  'CODE'
                         38              ASSUME   CS:CODE,DS:DATA,SS:STACK
                         39
                         40      ; INITIALIZE 8087
                         41
0000 9A0000----     E    42      INIT:   CALL     INIT87          ; This routine is in a library.
                         43                                       ; It sets up the environment
                         44                                       ; for the 8087.
                         45
0005 9BD92E1000     R    46              FLDCW    CONTROL_87      ; Load control word from memory.
                         47
                         48      ; SET UP 8086 REGS AND CONSTANT STACK IN 8087
                         49
000A 9BD9E8              50      SETUP:  FLD1                     ; PUT 1.0 IN STACK TOP (ST)
000D 9BDCC0              51              FADD     ST,ST(0)        ; ST=ST X 2
0010 9BD9060000     R    52              FLD      RIGHT.BASE      ; ST <-- BASE
0015 9BD9060400     R    53              FLD      RIGHT.ALT       ; ST <-- ALT
                         54      ;
                         55      ; CALCULATE AREA=(BASE X ALT)/2 AND STORE IN MEMORY
                         56      ;
001A 9BD9C1              57      CALC:   FLD      ST(1)           ; Duplicate BASE in ST
001D 9BD8C9              58              FMUL     ST,ST(1)        ; ST <-- BASE X ALT
0020 9BD8F3              59              FDIV     ST,ST(3)        ; ST <-- ST/2
0023 9BD91E0C00     R    60              FSTP     RIGHT.AREA      ; Store ST in AREA and discard
                         61      ;
                         62      ; CALCULATE HYPOTENUSE = ((BASE**2)+(ALT**2))** 1/2
                         63      ;
0028 9BDCC8              64              FMUL     ST,ST(0)        ; Square ALT
002B 9BD9C9              65              FXCH     ST(1)           ; Exchange ALT**2 and BASE
002E 9BDCC8              66              FMUL     ST,ST(0)        ; Square BASE
0031 9BDEC1              67              FADD                     ; ST <-- BASE**2 + ALT**2
0034 9BD9FA              68              FSQRT                    ; ST <-- ST** 1/2
0037 9BD91E0800     R    69              FSTP     RIGHT.HYP       ; Store ST in HYP and discard
                         70
003C F4                  71      HALT:   HLT
                         72
                         73
                         74
----                     75      CODE    ENDS
                         76              END      INIT,DS:DATA,SS:STACK:T_O_S
```

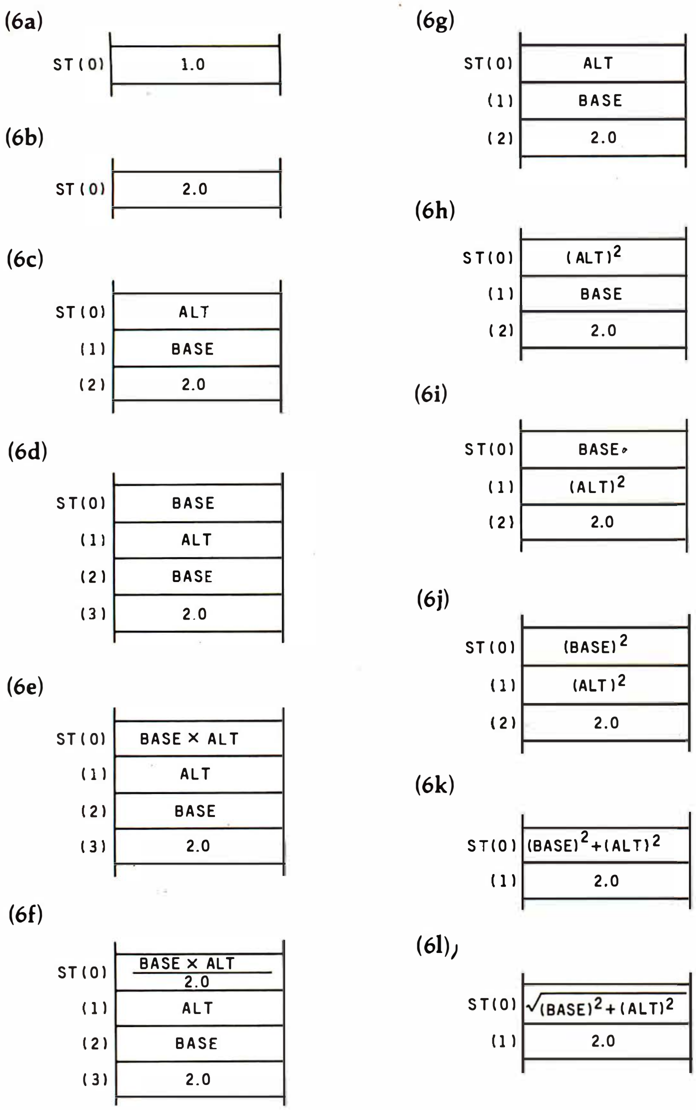


Figure 6: *The status of the NPX stack during operation of the program in listing 1.*

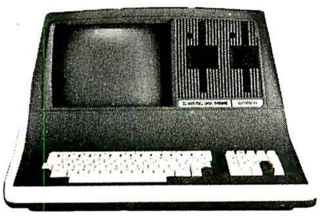
propriate memory location in the Short Real format (figure 6g).

My next task is to calculate the length of the hypotenuse of the triangle. The instructions to do this are on lines 64 through 69. First, I multiply the element on the top of the stack by itself (figure 6h). Next, I exchange this element with the element below it (figure 6i), and once again I square the stack top by multiplying it by itself (figure 6j). All that remains is to add the stack top to the register below it, pop the old stack top (figure 6k), and find the square root of the stack top (figure 6l). The value in the stack top now equals the length of the hypotenuse. I next pop this value into the appropriate location in memory and I am finished.

This concludes the example. I have just performed calculations that involve transcendental functions and that use operands that are very accurate with no concern for either the complexity of the algorithm or the accuracy of the result. If I had attempted to perform the same calculation in software, I would have had to write some very complicated algorithms and the code necessary to trap any errors that may have occurred. Instead, I let the 8087 and the standard to which it complies worry about such things. It puts the world of accurate, high-level mathematics in the realm of every assembly-language programmer. ■

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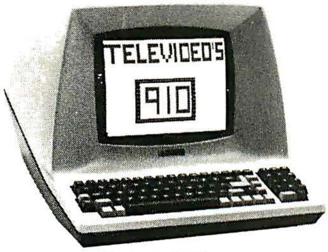
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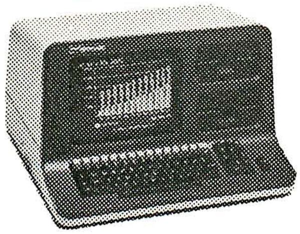
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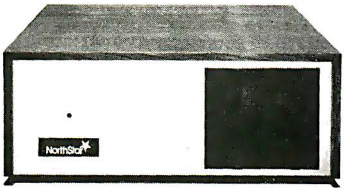
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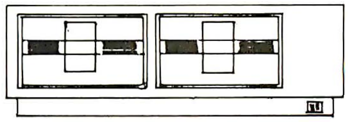
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In an attempt to standardize both the data types and algorithms used in floating-point-arithmetic problems, the IEEE formed a committee in 1979 to produce a standard to which all floating-point-arithmetic processors and software would comply. This standard not only established standard data formats, but also set rules for rounding and precision control and required that all machines (and software packages) complying with the standard be capable of performing the same algorithms with the same predictable results. The concept of exception handling was expanded and standardized so that all machines (and software) that complied with the standard would monitor their own activity and be capable of signifying when the result of their calculations was suspected of being in error. The 8087 implements this standard fully.

Data Formats

One of the most important aspects of the IEEE standard was the definition and standardization of the seven data formats that would be used in floating-point calculations. These formats belong to three basic types: Integer, Decimal, and Real.

The Integer type should be familiar because it is a standard data type used quite generally. The Integer formats are capable of representing signed whole numbers. The most significant bit denotes the sign (where a 0 indicates a positive number and a 1 indicates a negative number that is represented in standard two's-complement notation). The three Integer formats differ in length. The shortest format, Word Integer, is 16 bits in length and identical to the Integer format used by the host processor in its own instruction set (IMUL, IDIV). The Short Integer is 32 bits in length. Most 8086 assemblers allow you to allocate space for this type of variable using the Define Doubleword (DD) operator. Appropriately, the longest format is the Long Integer, which is 64 bits in length. Most assemblers allow you to allocate space for this type of variable with the Define Quadword (DQ) operator.

The Packed Decimal format, 80 bits long, is similar to the Integer format in that the most significant bit is a sign bit. The similarity ends there, however, because the data is stored in Packed Decimal format where the 18 least significant nybbles (bits 0 through 72) each represent a decimal digit. This means that each group of 4 bits must be equal to a value between 0 (0000) and 9 (1001). If this looks like a lot of data, remember that this processor is capable of delivering results that use all 18 nybbles of this format with no round-off error! You can use the Define Tenbyte (DT) operator to allocate space for this variable.

Up until now I have described only data formats that represent whole numbers. While it would be nice if everything always worked out neat and clean without any fractions, in the real world we have to deal with all types of numbers. The next data type, Real, was created to handle these types of numbers.

The Real data type contains three formats. They are very similar to the scientific notation that represents large decimal numbers. A number represented in scientific notation has three components—sign, mantissa, and exponent. In scientific notation, I would represent the decimal number $-547{,}390$ as -5.4739×10^5. In other words, I denote the sign of the number in the normal manner. Then I display its value or mantissa as a value between 0 and 10. I do this by moving the decimal point to either the right or the left. Whenever I move the decimal point to the left to normalize the number (make it equal to a value between 0 and 10), the exponent increases. When I move the decimal point to the right to normalize the number, the exponent decreases. For example, 0.0075 becomes 7.5×10^{-3}. The Real formats also have a sign, mantissa or significand, and an exponent, but they are binary values that are calculated a little differently.

As an example, I'll convert the decimal number 66 to the Short Real format. The Short Real format uses the 23 least significant bits to denote the mantissa of the number, the next 8 most significant bits to denote the exponent, and the most significant bit to denote the sign of the number. The first thing I must do is to convert the number to binary: decimal 66 = binary 1000010. Because this is a whole number, I have no fractional part to worry about. Now I must normalize the number by moving the decimal point over so that the value has a "1" in the most significant digit. As in scientific notation, I increase the exponent whenever I move the decimal point to the left and decrease the exponent whenever I move the decimal point to the right. In this case, because I move the decimal point to the left, the exponent is positive: 1000010 = 1.000010 E 110.

Now I am just about to finish the conversion, but you must know two things. In the Short and Long Real formats I save a bit by dropping the leading "1" bit of the significand. This allows me to denote 24 or 53 digits in the space required for 23 or 52 in the Short or Long formats, respectively. For some reason, this is not done in the Temporary Real format. The second thing is that the standard format requires that a bias be added to the exponent so that negative exponents appear as positive values. The bias is different for each format and is shown in figure 7. The bias for the Short format is 7F hexadecimal (01111111). This means that the exponent becomes 110 + 01111111 = 10000101. Putting it all together, I get

sign   biased exponent
0   10000101
significand
00001000000000000000000

or

0100 0010 1000 0100 0000 0000 0000 0000

With a number with a fractional part, the conversion looks like that shown in table 2. Table 3 is useful in understanding the power of the various data types.

Guaranteed Accuracy

The key to the 8087's ability to produce results with such a high degree of accuracy lies in the fact that the 8087 performs all its calculations in the Temporary Real data format. Regardless of the format in which an operand is stored in memory, any piece of data

that is loaded into the 8087 is transformed into this highly accurate, 80-bit-long format. The benefit derived by using this format for all internal calculations can be best illustrated by the following analogy.

I have a calculator with a range of 3 decimal digits and I want to use it to solve the equation $F = A \times B / C$. I got a calculator with 3-digit accuracy because I determined that A, B, and C would never be greater than 3 digits in length. If $A=100$, $B=10$, and $C=10$, you can see that I will have trouble solving this problem using my calculator because $A \times B$ is outside of its range. Even though the final result may be well within the range of my calculator, I may have trouble with the intermediate results.

Although changing the order of operations may help in this particular situation, it should be obvious that this solution will not resolve the problem in all cases, for instance, if $A=100$, $B=10$, and $C=0.1$. In this case, I would have a problem if I were to calculate A/C.

Now, if I got a new calculator that had a range of 4 or 5 digits, even though I expected all my results to be 3 digits or less, I could solve my problem. Regardless of the order in which I did my calculations, the intermediate results would probably not overflow the range of the new calculator.

This is precisely how the 8087 can guarantee such accurate results. By using the Temporary Real format for all its calculations, it avoids errors that may appear in the calculation of its intermediate results. The Temporary Real format, as you can see from table 3, has a range so large that we would probably never overflow it in our calculations. Also, because it uses 64 bits for the mantissa, it can provide results that are accurate to 18 significant digits with no round-off errors.

Ease of Use

Another way in which the 8087 can guarantee accurate and standard results is by providing default exception handlers that ensure results even though an error may have occurred during one of the intermediate calculations. For example, if for some reason during the operation of one of my calculations I somehow manage to attempt to divide a number by 0, the 8087, rather than aborting the operation, executes a default response to the zerodivide exception and replaces the quotient with the most reasonable value—infinity. In this manner, the 8087 provides standard results.

```
          − 178.125D = − 10110010.001B
        10110010.001 = 1.0110010001 E 111
          111 + 01111111 = 10000110
sign    biased exponent          significand
  1        10000110         01100100010000000000000
 1100   0011   0011   0010   0010   0000   0000   0000
```

Table 2: *The conversion of a number with a fractional part.*

Data Type	Bits	Significant Digits	Approximate Range
Word Integer	16	4–5	−32768< x < 32767
Short Integer	32	9	−2E9 < x < 2E9
Long Integer	64	18	−9E18 < x < 9E18
Packed Decimal	80	18	−99...9 < x < 99...9 (18 digits)
Short Real	32	6–7	0, 1.2E−38 < x < 3.4E38
Long Real	64	15–16	0, 2.3E−308 < x < 1.7E308
Temporary Real	80	19–20	0, 3.4E−4932 < x < 1.1E4932

Table 3: *The various data types.*

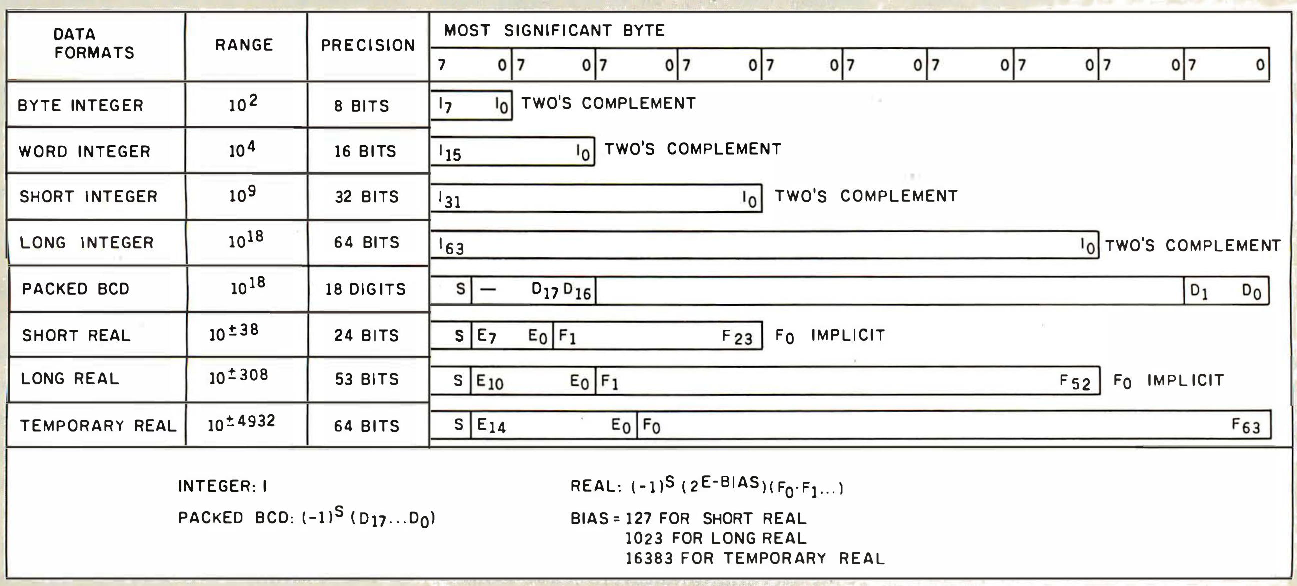


Figure 7: *The seven data formats contained in the three basic types.*

Super Graphics Hardware from NEC

The NEC 7220 GDC is a new item of sophisticated graphics hardware for microcomputers.

Steve Levine
c/o Personal Computer Arts Group
POB 1954
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Graphics capability is rapidly becoming a common feature of personal computers, partially because of consumer demand. The latest item of sophisticated graphics hardware for personal computers is the NEC (Nippon Electric Company) 7220 GDC (graphics-display controller), already found in the NEC Advanced Personal Computer, Epson's QX-10, and the Corvus Concept.

Before explaining what this controller does, I'll make a distinction between video displays and graphics. A video controller generally deals with displaying alphanumeric information such as ASCII (American National Standard Code for Information Interchange) characters. Primarily, it converts ASCII data into a dot pattern that a video monitor displays. You can read a good basic discussion of this subject in *The TV Typewriter Cookbook* by Don Lancaster (Howard W. Sams, 1976).

By contrast, a graphics-display controller converts graphics-image data into pixel (picture-element) data, and then stores them into or fetches them from display memory. The pixel data represents some arbitrary number of different shades or colors (including white or black) for each element of the picture. A graphics controller shares the display memory with a host computer. This arrangement permits both the host and the controller to read from or write to the display memory. In many cases, this arrangement uses a dual-port memory or interlaced DMA (direct memory access). Thus, data written into display memory can be manipulated by the GDC while the processor is off doing something else.

The most time-consuming part of getting a computer to draw a shape is calculating the next display-memory address to access. In fact, you must repeat this part of the process to change any dot on the screen. If you use the host processor to perform the calculations, the display often exhibits flicker and jerkiness because of the calculation time required. Despite this drawback, however, most small-computer manufacturers leave graphics control to the microprocessor, trading quality for lower cost. Presently, special graphics computers use external hardware dedicated to vector generation, as well as shape functions (such as rectangles, squares, and circles) prestored in ROM (read-only memory). With these systems cost is usually secondary, as performance is of most importance to the user.

Parts of the 7220 GDC

The 7220 GDC has several parts. The *microprocessor-interface module* serves as an 8-bit bidirectional interface to the host processor. Data transfers into and out of the device are done by monitoring status-register bit flags, which reflect the state of a FIFO (first-in/first-out) buffer. These transfers do not interfere with internal ongoing operations, and the FIFO buffer can store up to nine 16-bit words. The *command processor* decodes commands, interprets the contents of the FIFO buffer, and passes parameters to the proper blocks within the GDC.

The *DMA control* gives you an easy interface to Intel's 8257 and 8237 DMA controller devices. You can also interface other DMA controllers. Display data can be directly loaded into or out of the GDC display memory over the host microprocessor's bus. Sixteen bytes of internal *parameter RAM* (random-access read/write memory) hold the display parameters used by the GDC when drawing. The programmable *video-sync generator*

About the Author

Steve Levine is currently programming computer-graphics simulations and voice I/O for the U.S. Navy. He is employed by Information Network Systems in Warminster, Pennsylvania. Steve is also one of the cochairmen of The Personal Computer Arts Group, which is responsible for five annual Symposia on Small Computers in the Arts held in Philadelphia. He is also involved in the research of a new digital music synthesizer.

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takes its time reference from the master clock and provides synchronization signals for interlaced video raster. It also accepts external slave synchronization when used in conjunction with multiple 7220s. The *memory-timing generator* provides two clock-cycle refresh signals and four clock-cycle read/modify/write signals for the display memory.

The *zoom and pan controller* module allows you to program a zoom factor (or magnification factor) in integers between 1 and 16. Pan (or side-to-side) control is effected by programming different display-window starting addresses. The *drawing controller* calculates the pixel addresses for lines, figures, and characters. You set the drawing parameters and a starting point, and the controller proceeds to draw the desired figure, without assistance, from that point on. The *display-memory controller* handles all memory multiplexing, modification, refresh counting (for dynamic memories), and partitions the video-field time between different types of cycles. Finally, the *light-pen deglitcher* looks for two rising edges occurring at the same point in two successive video fields. When this occurs, its signals change a status bit to show that the address contained in the light-pen register is valid.

Display Modes

You can select three basic display modes with the 7220: graphics, character, or mixed.

The graphics mode lets you use bit-mapped graphics at the pixel level. This mode allows a display to be up to 4096 pixels square (allowing 1 bit per pixel for intensity information) or 1024 pixels square (allowing 4 bits for color or intensity-level information). Other combinations can be set up as well—the circuit used in this article produces a 512- by 240-pixel window, 1 bit deep, on a 1024-pixel-square, 1-bit-deep world.

Character mode allows up to 8K bytes of display memory for character codes and attributes.

The mixed character and graphics mode allows 64K bytes of display memory.

Displaying Memory

A basic read/modify/write cycle takes place in less than 800 nanoseconds (ns). This interval is the minimum for writing totally new pixels into memory, one at a time. The GDC provides the memory control, refresh, and handshake with DMA controllers. The benefits are obvious. The hardware designer does not have to design circuitry to produce refresh signals, because the 7220 generates them. Additionally, because the 7220 controls the data-modification and video-display functions, you get a clean display without visi-burps. You control several display parameters, including the horizontal width, vertical size, and the world size (total amount of display memory). You can also select zoom factors and interlaced or noninterlaced synchronization.

To display a complete frame of video information, an image must be kept in display memory. Because memory organization is a linear-address space, an image of a single horizontal line is actually stored as a number of widely separated dots. If you divide the number of dots per

See other ad on page 483.

(a) Pitch (P)
P = (XMAX + 1) / 16

(b) Line-Base Address (LBA)
LBA = P • Y

(c) Execute Address (EAD)
EAD = LBA + INT (X/16)

(d) DAD (dot address)
DAD = remainder (from EAD calculation) * 16

Figure 1: *Four equations to locate an individual dot address.*

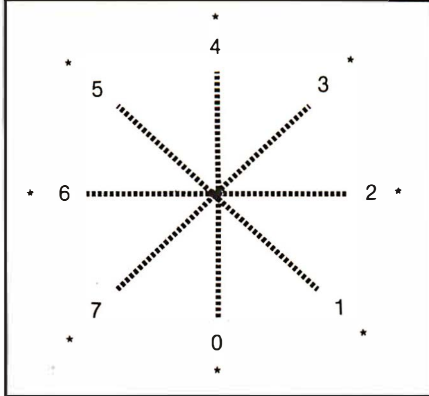


Figure 2: *A direction map for controlling pixel-drawing direction.*

A0	Read	Write
0	S/R	Parameters into FIFO
1	FIFO	Command into FIFO

Figure 3: *GDC addressing.*

Data Ready	FIFO Full	FIFO Empty	DWG in Progress	DMA Execute	V-sync Active	H-blank Active	L-pen Detect
B7	B6	B5	B4	B3	B2	B1	B0

Figure 4: *The status register.*

line by 16 you get a value called pitch, or the number of 16-bit memory words per line. To move the cursor down one dot on the screen, you add the pitch to the 18-bit value in the word address and use a 4-bit dot address to access the individual pixel within that word. To move the cursor forward or backward on a line, all you need are simple increments and decrements. You obtain diagonal movement with some combination of these two methods.

When a new pixel is to be written into display memory, its position within a 16-bit word is loaded into the mask register. Then you specify the absolute cursor position, the modification pattern, and the type of modification (replacement, complement, set, or reset). The GDC automatically changes only the bit you want to update. The host processor continues to do other things while the display processor performs this legwork. You will notice the real power of this approach when you try to create complex shapes made up of many fundamental shapes and scale, and then move or redraw them.

Pixel Addressing

There can be up to 2^{22} pixels organized as 2^{18} sixteen-bit words, and you need a two-part address to select an individual pixel. First, the EAD (execute address) selects a particular 16-bit word out of the 256K bytes; then the DAD (dot address) selects which bit or pixel from the 16 to operate on.

Consider an x-y vector-list scheme where we would like to find the individual dot address (see figure 1). You simply derive the P or pitch from equation a, find the line-base address (LBA) using equation b, and get the EAD from equation c. Next you obtain the dot address from equation d, and you now point to the exact pixel in the x,y matrix. We structure the memory as a power of 2 in order to avoid real arithmetic for these calculations. We send these numbers to the GDC (in binary) to set the cursor position.

An important parameter in deriving consecutive pixel addresses is the DIR, which controls pixel-drawing direction. This is best illustrated by the direction map in figure 2. Drawing direction is divided into eight movements about the center. By specifying a direction, you get a resulting dot movement according to the figure.

Talking to the 7220

The GDC appears as two consecutive addresses to the host, which selects between the two by using address bit 0 (see figure 3). The first address is status register on read and parameter into FIFO buffer on write. The second address serves as read/write FIFO buffer, with write pertaining only to command into FIFO buffer. In order to get commands and data into the FIFO buffer, you handshake with a FIFO ready bit in the status register. You first send a command byte followed by several parameter bytes that make up the command. After initial loading, an internal command processor decodes the commands, sets the appropriate registers to the passed values, and starts the specified process.

A simple software or hardware handshake is necessary when loading data into the GDC FIFO buffer. The status register has FIFO FULL, EMPTY as well as other flags of interest to the programmer (see figure 4).

Summary of Commands

The FIFO buffer holds both commands and parameters. By writing data to the second, or command, address, you apply a special tag to the data that identifies it as a command when it is put into the FIFO buffer. This tag helps the command processor to tell the difference between parameters and commands. When the command processor receives a new command byte, it terminates previous commands. Commands for the GDC are shown in table 1.

Figure Drawing

The *digital differential analyzer* (DDA) forms the workhorse section of the figure-drawing logic. It per-

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Video Control		
A	RESET:	Set 7220 to idle, set video-display format
B	SYNC:	Set video-display format
C	VSYNC:	Master or slave video-sync mode
D	CCHAR:	Cursor and character row heights
Display Control		
A	START:	Begin scanning
B	ZOOM:	Specify zoom factors
C	CURS:	Specify cursor position in display memory
D	PRAM:	Set display area's start and length. Also set 8 bytes for the graphics character
E	PITCH:	Display-memory X-dimension width
Drawing Control		
A	WDAT:	Write data into display memory
B	MASK:	Specify mask-register contents
C	FIGS:	Figure specify of drawing parameters
D	FIGD:	Draw the above specified figure
E	GCHRD:	Graphics character draw
Data Read		
A	RDAT:	Read data from display memory
B	CURD:	Read cursor position
C	LPRD:	Light-pen address read
DMA Control		
A	DMAR:	Request a DMA read transfer
B	DMAW:	Request a DMA write transfer

Table 1: *The GDC command summary.*

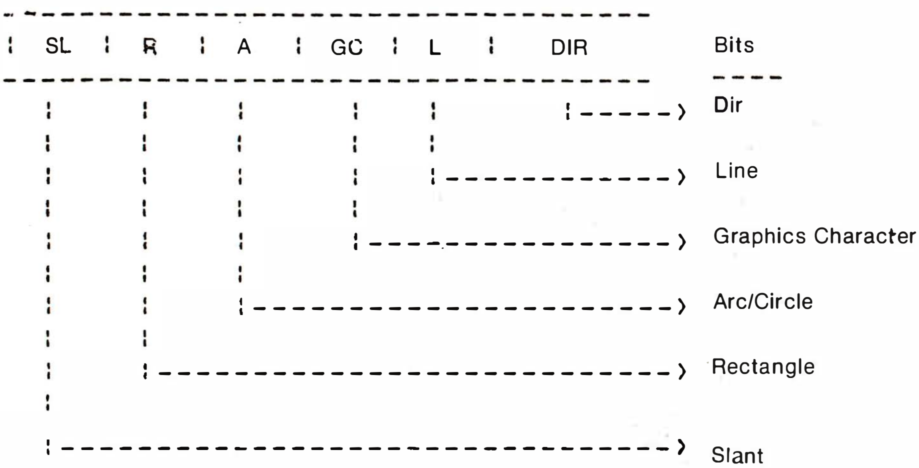


Figure 5: *The layout of the FIGS (figure specify) command.*

forms the necessary adds, shifts, and counts that allow you to draw a 100-pixel figure in only 80 microseconds (μs), using differential equations to specify the delta x,y information. (See *Principles of Interactive Computer Graphics* by William M. Newman and Robert F. Sproul [McGraw-Hill, 1979, pp. 22-28].)

To perform the differential operations on vectors, you specify values for the DDA parameters. The four DDA parameters for vector operations are DC (dot count), an unsigned integer from 0 to 16,383 calculated by the host to be the total number of pixels to move; D1, the same type of number, but used for slope-encoding terms; D, a 16-bit integer, also used as a slope term; and D2, another 16-bit integer used as a slope term. These four parameters are derived from equations that represent initial and ending vectors of a line, arc, or rectangle. In addition to specifying values for these four parameters, you must load the EAD of the beginning pixel, the DAD, and the DIR values before you issue the FIGD (figure draw) command.

With a minimum of instructions, you can make the GDC draw fundamental shapes. The DDA, which is on-chip hardware, does the time-consuming calculation to produce the next pixel address for the shape. This circuit and the memory-modification hardware (read/modify/write) combine to produce a rapid update of new pixels.

When you want to begin figure drawing, you load a figure type, drawing direction, drawing parameters, cursor starting address, and the pattern into the FIFO buffer. Then you issue a FIGD command. A FIGS (figure specify) command alerts the GDC to the necessary drawing parameters, which are either computed by the host processor or stored in a table (see figure 5).

A Line-Drawing Example

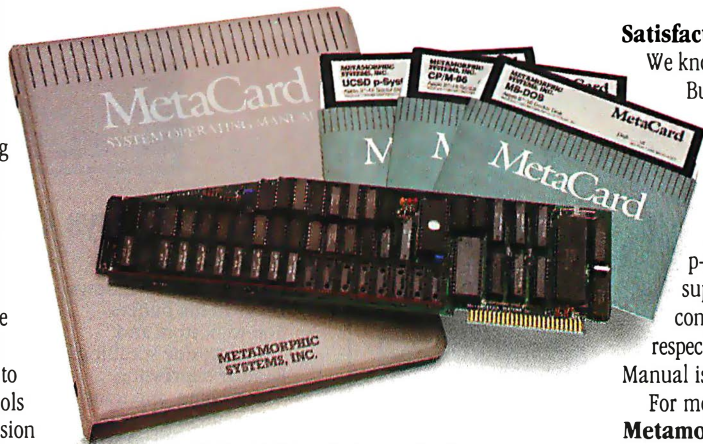
The GDC drawing technique uses independent and dependent axes. The host processor determines which axis is independent and which is dependent for the particular drawing direction or octant of that vector. To draw a line from XY Start to XY End, you first move the cursor to XY Start with the CURS command, then calculate the Deltas (Delta X = X End − X Start, Delta = same), and find the direction by locating the quadrant and the octant (see table 2). If ABS Delta_X = ABS Delta_Y, the vector is on octant boundary within that quadrant and you choose the higher-numbered odd octant.

You then determine the independent and dependent axes with the following equation:

If Delta_X > Delta_Y
  Then I = X, D = Y
If Delta_X < = Delta_Y
  Then I = Y, D = X



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Quadrant

Delta_X sign	Delta_Y sign	Quadrant
+	−	1
−	−	2
−	+	3
+	+	4

Octant

ABS Delta_X	>	ABS Delta_Y
If Quadrant	Then	Octant
1		2
2		5
3		6
4		1

ABS Delta_X	<	ABS Delta_Y
If Quadrant	Then	Octant
1		3
2		4
3		7
4		0

Table 2: *Information for locating the quadrant and octant for line drawing.*

Now you compute the line-drawing DDA parameters:

DC = ABS (Delta_I)
D = [2 * ABS (Delta_D)] − ABS (Delta_I)
D2 = 2 * [ABS (Delta_D) − ABS (Delta_I)]
D1 = 2 * ABS (Delta_D)

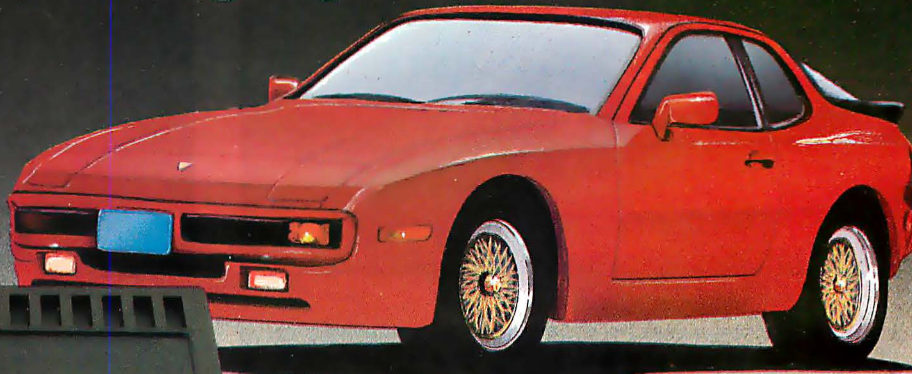
You can make these operations fairly efficient by using a table for octant and axis determination.

Once these parameters are calculated, you load them into the GDC FIFO buffer with a FIGS command. Then you load a pattern into parameter RAM with a PRAM command. The pattern corresponds to the type of line—broken, dashed, or solid. A WDAT (write data) command with bit modifier and a FIGD command complete the figure-drawing process (see photos 1 through 4).

Drawing a circle of arbitrary radius at a specified point on the display requires that you prepare most of the parameters discussed above with the



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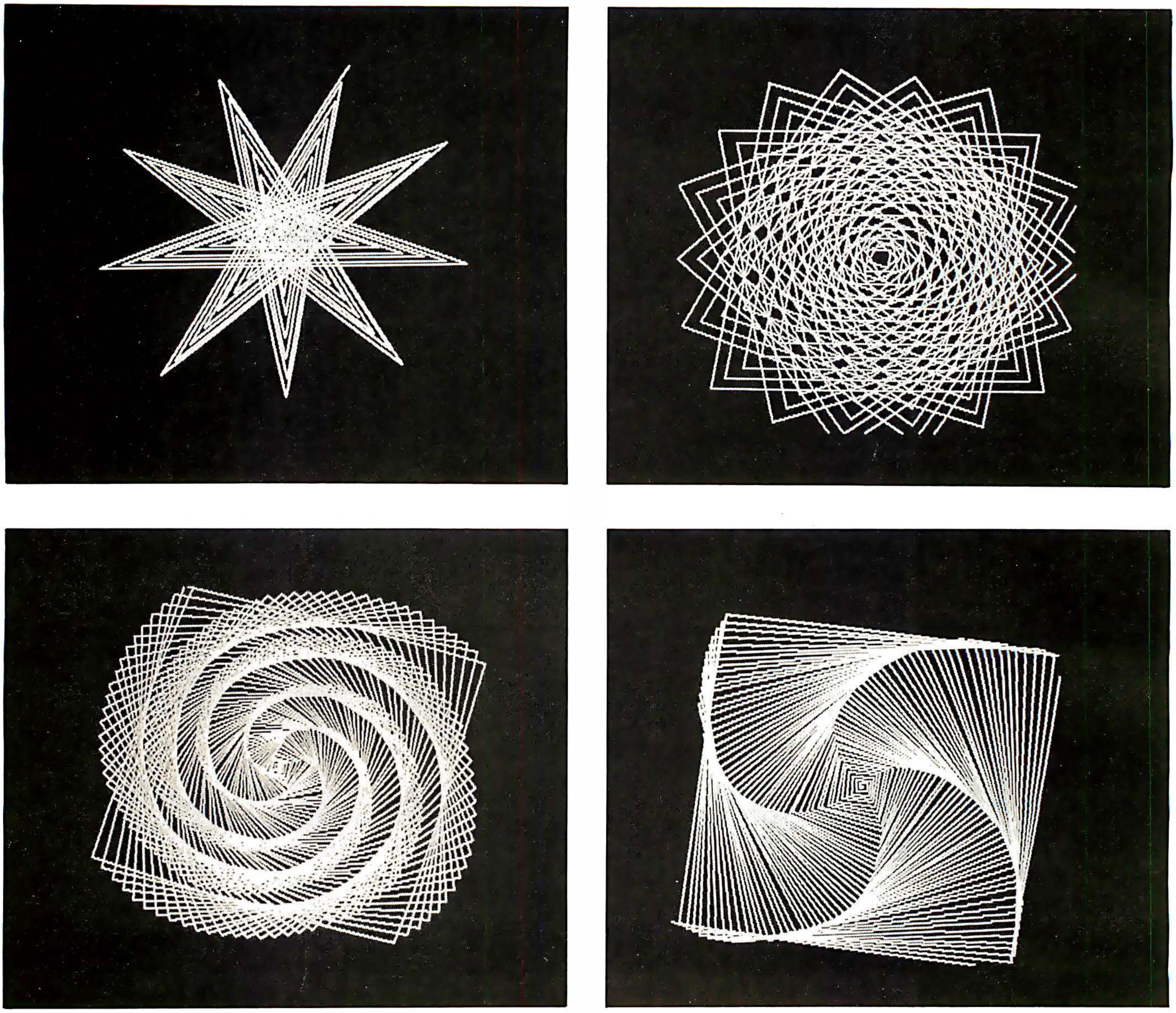
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Photos 1–4: *Examples of the GDC figure-drawing process.*

exception of the DDA drawing parameters. The following information draws a circle as eight arcs, with two per quadrant:

DC = Radius * Sin (Theta)
D = Radius − 1
D2 = 2 * (Radius −1)
D1 = −1
DM = Radius * Sin (Phi)

The starting points might be

radius, 0
0, radius
−radius, 0
0, −radius

Rectangle drawing is similar, but simpler:

DC = 3 (fixed for circles or arcs)
D = (Total number of pixels in initially specified direction) −1
D2 = (Total number of pixels in perpendicular direction) −1
D1 = −1
DM = Same as D

Applications

The 7220 GDC is not a simple device. While many of you have probably written a BIOS (basic input/output system) or CRTC (cathode-ray tube controller) handler, developing a decent assembly-language driver for this chip is nontrivial. The driver I am currently using was written by Frank Caparello under the auspices of Roger Amidon and others, the developers of the new Epson QX-10. The S-100 board I used to draw the demonstration screens was also developed by them. The Epson QX-10 uses a 7220 as a display chip but has operating-system calls to do all the fancy stuff.

The GDC design manual that NEC provides is very well written and offers you a basic tutorial on computer graphics. It includes numerous examples of parameter derivation as well as hardware-interface information. I highly recommend it.

I believe the 7220 GDC will be a standard for microcomputer displays for the next few years. If the price falls, you may even find it in arcade games and low-end terminals. ■

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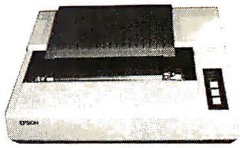


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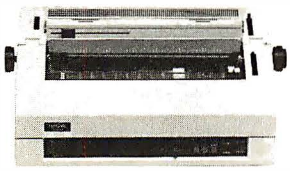
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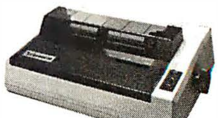


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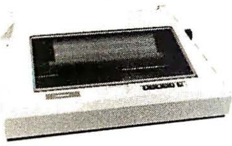


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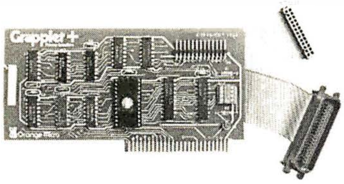
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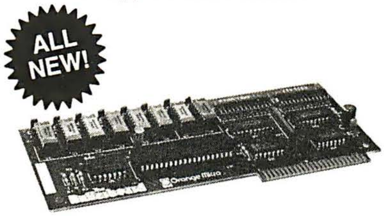
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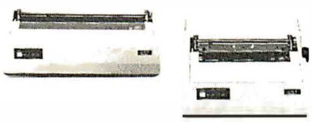
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The North American Presentation-Level-Protocol Syntax (NAPLPS) is a communications standard that can encode both text *and* graphics. The goal of this standard is to facilitate the exchange of information from one machine to another without regard to differences in the individual graphics-handling capabilities of each machine. In fact, in some ways NAPLPS can be viewed as an extension of the American National Standard Code for Information Interchange (ASCII).

Part 1 of this series presented an overview of NAPLPS. In part 2 I described the basic features of NAPLPS with an emphasis on the actual coding. In this part I will concentrate on the more advanced features of NAPLPS, specifically, Incremental Lines, Macros, Dynamically Redefinable Characters, and Fields. This article will present merely an overview of these advanced features. In order to get a complete description of them, you should obtain a copy of the actual NAPLPS document from the Computer and Business Equipment Manufacturers Association (CBEMA), whose address is listed at the end of this article.

About the Author
Jim Fleming is a member of the ANSI X3L2 Committee on Character Sets and Coding. He is an independent consultant specializing in interactive computing systems.

Incremental Lines

As we saw in part 2, line drawings and objects can be encoded by specifying the endpoints of each line using a terminal-independent coordinate system. In general, it takes about 3 bytes to encode each line in a drawing. For objects with only a few sides or a regular shape (i.e., rectangle, arc, etc.), this efficient approach makes it easy to encode lines. But if an object has an irregular shape, the normal encoding method becomes very inefficient.

NAPLPS supports a method of *chain-encoding* irregular edges of shapes. An assumption is made that the irregular edge is composed of a large number of small line segments. Each segment can be encoded using just 2 *bits* of information—a substantial reduction over the 3 *bytes* needed using the normal method.

The method for chain-encoding line segments with 2 bits is shown in table 1. The first step is to establish a pair of relative coordinates (symbolized as *dx, dy*) that determines the length of the line segments. Multiple 2-bit values are then specified that indicate directions in which to draw the line segments. As shown in table 1, a line segment can be drawn horizontally, vertically, or diagonally.

If a horizontal segment is specified, it is drawn in the direction initially set by the value *dx*. If *dx* is positive, the horizontal segment will be drawn to the right; if *dx* is negative, the segment will be drawn to the left.

If you are following closely, you may be asking how we could get lines drawn to the left if we initially specify *dx* as positive. As shown in table 2, an Escape sequence is provided to reverse the direction of the drawing. Any time a 2-bit value is 00, the next 2 bits are interpreted as an instruction to change direction. The sequence 00 01 indicates that the horizontal direction should be reversed, the sequence 00 10 changes the vertical direction, and the sequence 00 11 reverses both directions.

Two-Bit Incremental Line Instructions

Symbolic Code	Two-Bit Encoding	Result
–	00	Change dx or dy values (see table 2)
X	01	← dx → (horizontal line)
Y	10	↑ dy ↓ (vertical line)
D	11	↑ dy ↓ dx → (diagonal line) or (opposite diagonal line)

Table 1: *With the Incremental-Line features of NAPLPS, some line segments can be specified with just 2 bits of information. The values dx and dy signify relative coordinates. If dx is negative, the line will be drawn to the left; if dy is negative, the line will be drawn downward. Other lines can be drawn by using the 4-bit direction changing codes shown in table 2.*

Incremental Line Escape Sequences

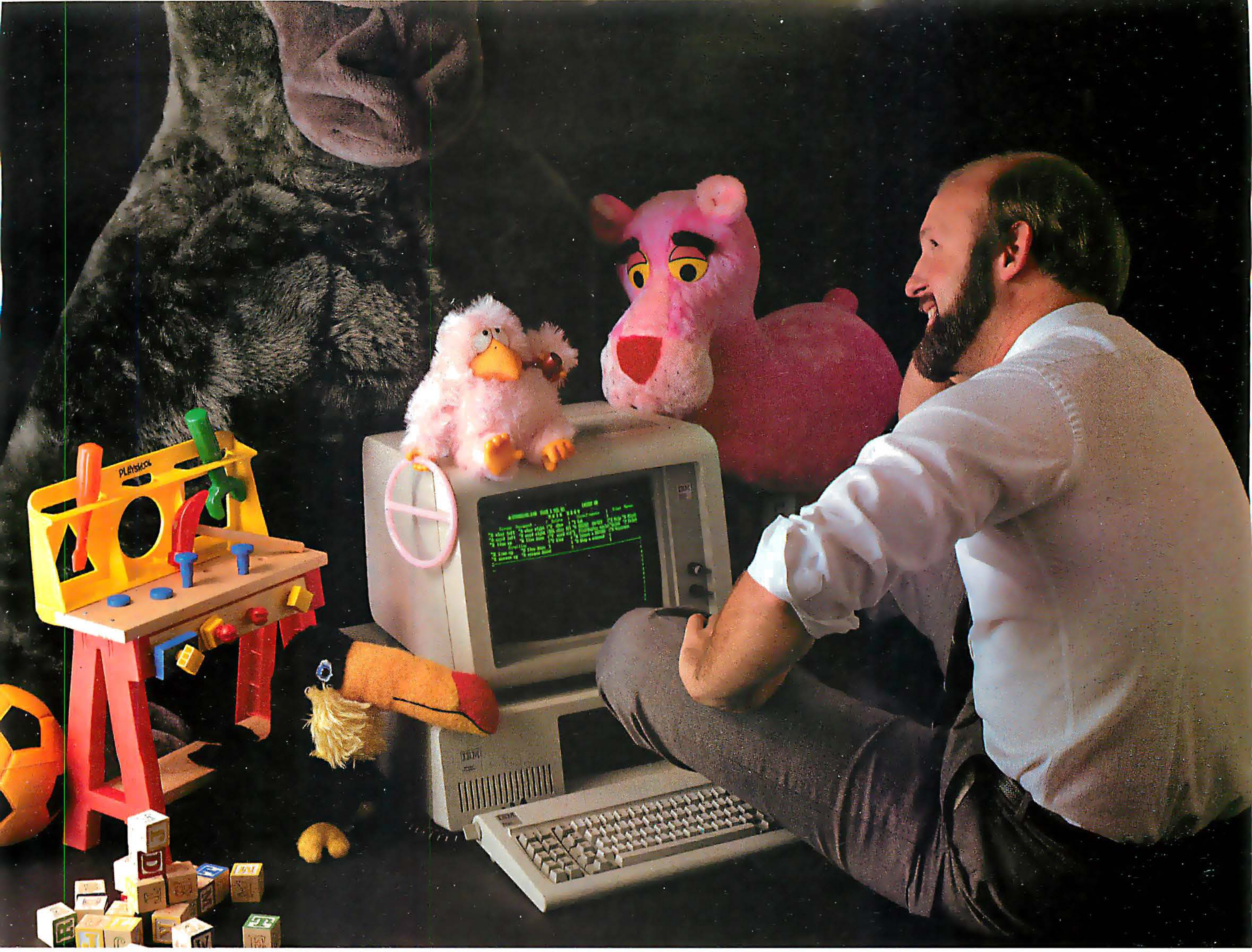
Symbolic Code	Four-Bit Encoding	Result
– –	00 00	If pen is down, then lift it up. If pen is up, then put it down.
– X	00 01	dx = –dx
– Y	00 10	dy = –dy
– D	00 11	dx = –dx, dy = –dy

Table 2: *Four-bit codes are used to change the direction of the drawing and control the pen position.*

If you are still with me, you may ask what happens when 00 is followed by 00. That sequence indicates that the state of the *pen* should be reversed. If the pen is currently *down*, it will be raised; if the pen is *up*, it will be lowered.

The 2-bit values are encoded in a series of bytes, 6 bits per byte (from left to right in table 3). The pen is assumed to be down at the beginning of a command. The last byte can be padded with a pen reversal if the number of line segments is not even.

Figure 1 shows a chain-encoded outline of the state of Indiana that is composed of 217 short line segments. These 217 segments require 87 bytes of coding in NAPLPS. If I had encoded this drawing using the normal



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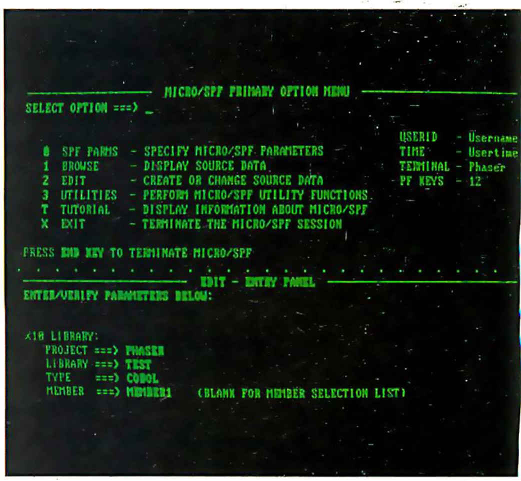
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Figure 1: *An example of an incremental-line drawing. The size can be changed simply by changing the values of the relative coordinates dx and dy. This drawing was done on a Diablo 630.*

method, 651 (217 × 3) bytes would have been needed. (Although these calculations ignore the fact that the northeast corner of the state could be efficiently drawn with normal straight lines, a large amount of memory would be required nonetheless.)

A symbolic representation of part of the chain encoding for figure 1 appears in table 3. It is the coding for part of the southwestern border of Indiana. The corresponding binary and octal values of the encoding are also included. The two outlines were produced from the same encoded data.

The scaling effect achieved in figure 1 was accomplished by changing the size of the *dx* and *dy* values. As shown in figure 2, the Incremental-Line op code (3A hexadecimal or 3/10 using a 16 by 16 column/row representation) and a relative coordinate pair (*dx*, *dy*) precede the encoded data. This (*dx*, *dy*) value can be changed to create some interesting effects. For example, it can be scaled so that the resulting drawing is larger or smaller, even though the *same* encoded data is used. Also, the values of *dx* and/or *dy* can be negative, resulting in mirror-image drawings from the same encoded data. The values of *dx* and *dy* can be very different, resulting in a stretching effect in one of the dimensions.

Besides chain-encoded outlined drawings, NAPLPS also supports chain-encoded filled polygons. These solid figures are subject to the same attributes of objects such as rectangles and arcs. These attributes can be used to draw the state of Indiana with a textured interior to help distinguish it from other objects on the screen or page.

Incremental encoding is a powerful technique for compactly representing irregular objects. The efficiency obtained by incremental encoding pays off in data-transmission time and disk storage. Another feature of NAPLPS that improves coding efficiency is the Macro capability.

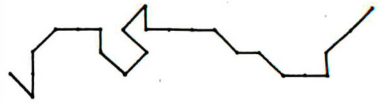
Macros

Macros provide a means of storing an arbitrary string of NAPLPS codes under one of 96 names. The string can be recalled using the 1-byte name associated with the string.

Macros are useful when a common string of NAPLPS codes is used for a particular application. For example, in a home-banking application the words Balance, Amount, and Payment will appear many times during a session. NAPLPS lets us store these words as macros and recall them by transmitting just 1 byte.

Macros can be used to store both text and graphics. Entire screens of in-

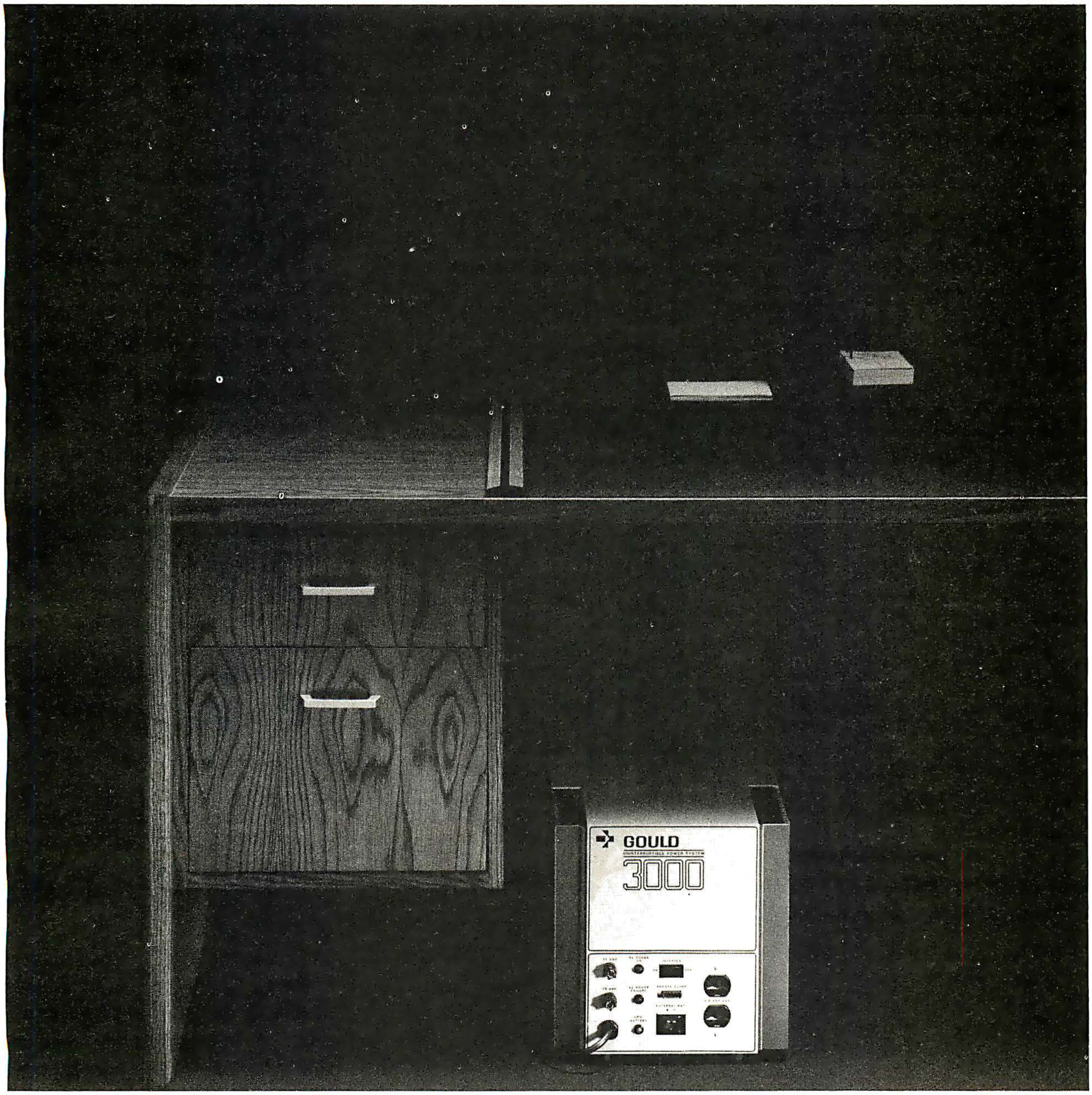
Sample of Incremental Line Encoding



Symbolic Code	Binary Code	Octal Code
- Y D	X1 00 10 11	113
- Y Y	X1 00 10 10	112
Y D X	X1 10 11 01	155
X - Y	X1 01 00 10	122
Y D -	X1 10 11 00	154
Y D -	X1 10 11 00	154
X D -	X1 01 11 00	134
X D -	X1 01 11 00	134
Y Y X	X1 10 10 01	151
X X D	X1 01 01 11	127
X D X	X1 01 11 01	135
X - Y	X1 01 00 10	122
Y D D	X1 10 11 11	157

Table 3: *An example of incremental-line coding. This is part of the coding used to produce the drawing of Indiana in figure 1.*

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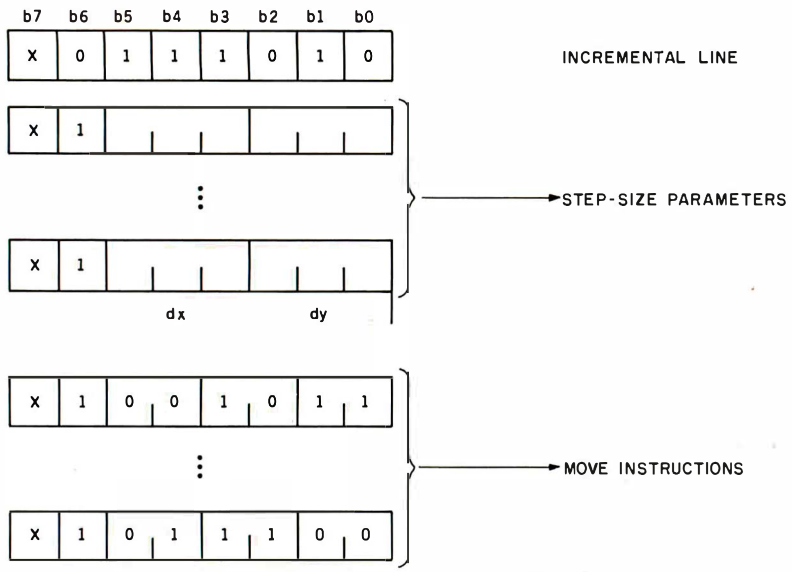


Figure 2: *Structure of the Incremental-Line instructions. The first byte indicates that a series of Incremental-Line instructions will follow. The next series of bytes indicates the size of the relative coordinates dx and dy to whatever resolution is desired. The last series of bytes is composed of the actual 2- and 4-bit drawing instructions.*

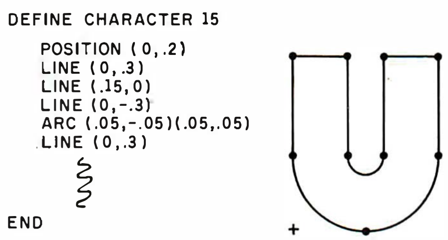


Figure 3: *Using the Dynamically Redefinable Character Set (DRCS) capability of NAPLPS, we can define our own characters.*

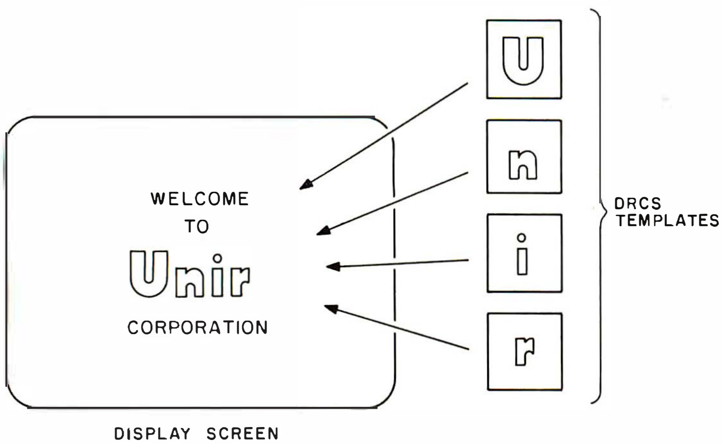


Figure 4: *Once a DRCS set has been defined, its characters can be mapped just like text characters onto the display screen.*

formation can be stored as one macro. In addition, other text and graphics can be intermixed with macros.

In applications like adventure games, each time a new room is entered, a macro can be defined with the picture of the room. If the room is reentered later in the game, the long graphics-and-text description does not have to be retransmitted. The host computer simply has to refer to the macro name and the entire room is drawn.

If the host computer is really smart, it can send down macros for all the rooms that are near the current room you are in. This can be done while you are deciding your next move. The screen will not be changed as these macros are defined. When you finally move to a new room, the host refers to the proper macro that was previously defined, and the user sees an almost instant response.

Macros can also be applied in conjunction with the Incremental-Line op code described earlier. Nothing prevents you from storing just the encoded data as a macro. If this is done, an Incremental-Line op code (3/10) can be sent followed by a (*dx*, *dy*) coordinate value followed by the macro reference. In the previous example (Indiana), the 87 bytes of encoded data would be retrieved and processed as if they had been sent after the (*dx*, *dy*) value. Thus, the size of the shape could be changed almost instantaneously.

Part 1 of this series includes an example of macro definition and reference. A NAPLPS code segment for that example is shown in listing 1. As you may recall, a macro (Macro 26) was defined that cleared the screen to blue and put the string "READY:" on the screen in white. Whenever Macro 26 is later referenced, the screen will be cleared and "READY:" will appear.

The amount of storage allocated to macros has been left open as a terminal- and application-dependent parameter. With 96 macro names and the ability to store long variable-length strings, the macro storage required could exceed the internal memory capacity of most personal

Listing 1: *A short segment of NAPLPS code (in octal form) showing how a macro can be defined and referenced. The contents of Macro 26 will be bytes 4 to 21 inclusive.*

```
BYTE    OCTAL   SYMBOLIC          DESCRIPTION
 #      FORM    FORM
--------------------------------------------------------------------
        .
        .
        ***** Define Macro 26 *****
        .
        .
1       033     ESC     Define Macro 26
2       100     DFM
3       072     M26
        .
        .
        .
4       016     SO      Select G1 (Graphics)
        .
        .
        .
5       074     SET     Set color to Blue
6       111     BLU
        .
        .
        .
7       040     RES     Clear Screen to in-use color
8       120
        .
        .
        .
9       074     SET     Set color to white
10      177
        .
        .
        .
11      044     SPA     Set Point Absolute
12      101             }
13      110             } - (x,y) = (.05078125,.25) => (13,64)
14      150             }
        .
        .
        .
15      017     SI      Select G0 (Text)
        .
        .
        .
16      122     R
17      105     E
18      101     A
19      104     D
20      131     Y
21      072     :
        .
        .
        .
22      033     ESC     End Macro Definition
23      105     END
        .
        .
        .
***** Referencing the Macro *****
        .
        .
        .
??      035     SS3     Assume 7 Bit Mode with Macros in G3
??      072     M26     Macro 26
        .
```

computers. There is absolutely no reason why disk storage cannot be used to store macros. When disks are used, a crude form of file transfer begins to emerge.

Macros thus provide a powerful capability of code reduction when using NAPLPS. The important thing to remember about macros is that a simple string replacement is performed. The resulting stream of code (after the macro expansion) is processed as if it had been sent from the host. No special scaling, rotation, or attributes are applied to the macro part of the resulting stream. In fact, in most systems, once the macro is expanded all knowledge is lost that a macro was used.

Dynamically Redefinable Character Sets

The Dynamically Redefinable Character Set (DRCS) capability in NAPLPS is similar to the Macro feature. The DRCS facility allows arbitrary streams of NAPLPS code to be associated with one of 96 names. The 96 DRCS names, however, are completely different from the macro names.

The primary difference between macros and DRCS characters is that when the DRCS image is referenced, it is scaled, rotated, and mapped to the current character field, just like a text character. In other words, a simple code replacement is not performed. Instead, the current environment of attributes and character-field size is used when the DRCS character is requested. Figures 3 and 4 show an application of the DRCS capability.

One of the primary functions of the DRCS is to define new text characters, because all TEXT command attributes (scaling, rotation, spacing, etc.) are applied when the DRCS is requested. Because of this text-character orientation, only two colors can be used when the DRCS is drawn. In other words, the drawing of the DRCS is done with a "spray-paint" technique, as with other characters. The DRCS thus acts only as a stencil.

The DRCS can also be viewed as a simplified form of the computer-graphics idea of a *window* and a *viewport*. When using a DRCS, the

Text continued on page 202

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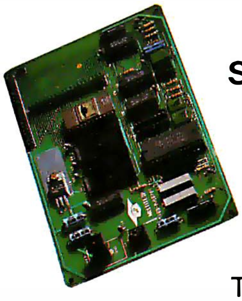
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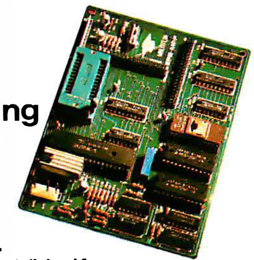
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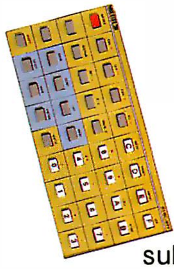
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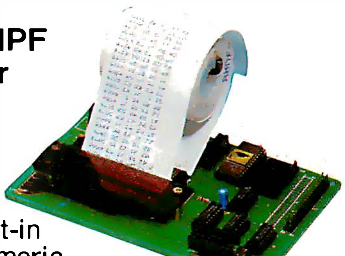
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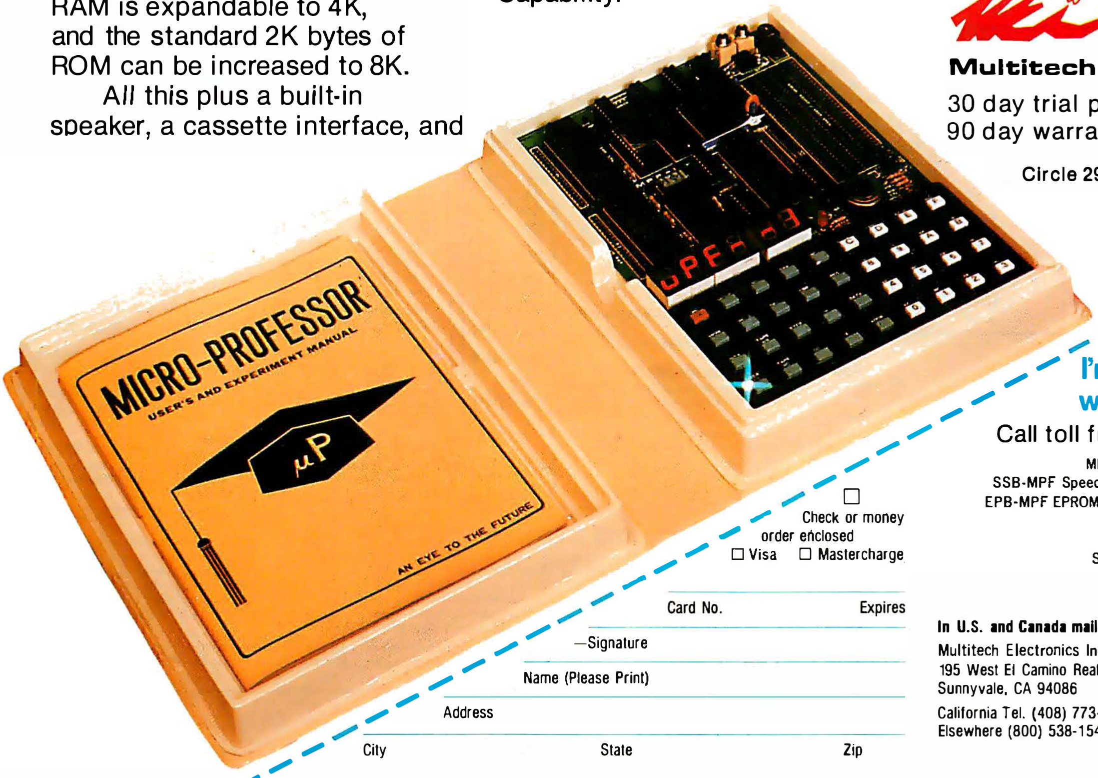
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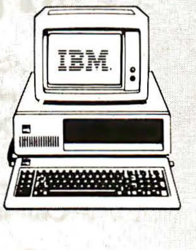
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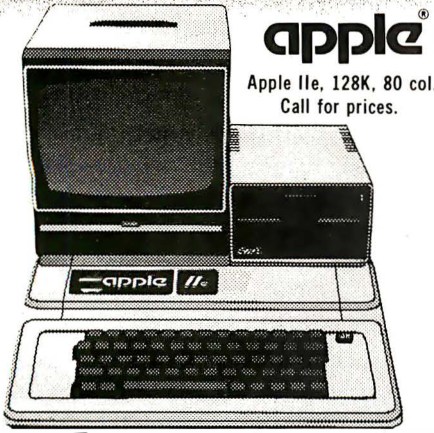
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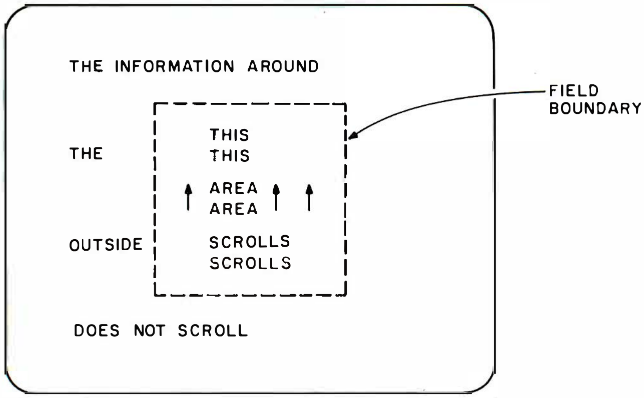


Figure 5: *In NAPLPS, some fields of the display screen can be scrolled; others remain stationary.*

window is completely mapped to the viewport, which is mapped to the character field on the screen. Figure 4 illustrates this mapping. Because the character field can cover an area from one pixel (picture element) to the entire screen, a scaling effect is achieved.

The DRCS capability is another method for reducing the transmission time of data sent from the host. In applications that require many special symbols, the symbols can be defined, given a name, and referenced with only 1 byte—even for a symbol that may require hundreds of bytes of definition. By replacing the hundreds of bytes with a single one, the transmission is compressed to the point that the users think they are connected to the host by a high-speed link.

Two popular methods of handling DRCS in terminals are available. The first method cuts the template as soon as the DRCS is defined. When the DRCS is requested, the previously cut template is retrieved and handled like any other character-definition template. The templates are usually stored on 8 by 8 or 16 by 16 grids internally in the terminal.

The second method for handling DRCS is to store the graphics commands themselves. No template is cut. When a DRCS is requested, the template is cut in a size appropriate for the current character field. The template may be 32 by 32, or even 256 by 256 for full-screen DRCS. Once this template is cut, it is mapped to the display screen using the spray-paint concept.

The primary difference between these two methods appears in the areas of speed and resolution. The first method is good when DRCS characters must be displayed very fast and with minimum resolution. If the DRCS is scaled to a much larger size, however, a crude image results from the precut template. The crude image results from the fact that some of the information may be lost when the cutting is performed, especially if the template is very small.

The second method preserves all the information by maintaining the DRCS definition in its original form. If a large DRCS is requested (i.e., the character field is large), all the original information can be used to draw the character. The disadvantage of this method is that the original definition has to be decoded each time the DRCS is requested. This can be quite time consuming for a DRCS that contains several hundred bytes of definition.

These two methods are not the only ways of handling DRCS. As with most features of NAPLPS, no restriction is placed on the method of implementation. The cleverness of the implementation will determine how much of the original information is transferred to the user. The appropriate time, space, and cost trade-offs have to be made in choosing implementation strategies. These decisions, of course, will help differentiate various companies' products. It would be an extremely boring world if NAPLPS were so restrictive that every terminal looked and performed *exactly* the same.

Fields

The last advanced feature to be discussed here is Fields. Fields are logical rectangular areas defined on the unit screen by the Field command (3/8). These areas are not visible to the user. Only one active field exists although, as will be seen, multiple fields can be defined as long as they do not overlap. Fields are used in a variety of ways in NAPLPS.

A common use of the Field capability is for setting margins. The Field command is used to establish the current active field, which is normally the entire screen. Each time a text character is placed on the screen, an internal cursor position is updated. If the boundaries of the field are exceeded, the cursor is moved to the other edge of the field in a manner compatible with most data terminals. If the cursor moves beyond the top or bottom of the field, a feature called partial screen scrolling comes into play. If scrolling is enabled, only the information inside the field is scrolled. The information around the field is not changed. Figure 5 attempts to show this concept.

Fields are also used to establish an area for high-resolution image display. The Incremental-Point command (3/9) can be used to specify the color information for each point inside a given field. In applications like real-estate listings, these features can be used to combine a photographic-like picture of a house with textual information concerning the same. Figure 6 illustrates a result that can be obtained.

But the most important use of the Field capability is for user input in systems such as videotex. As described in part 1, users are given one or more blank "sheets of paper" on their screen. The Field command is used to define where these sheets are placed.

When these so-called unprotected fields are placed on the screen, the

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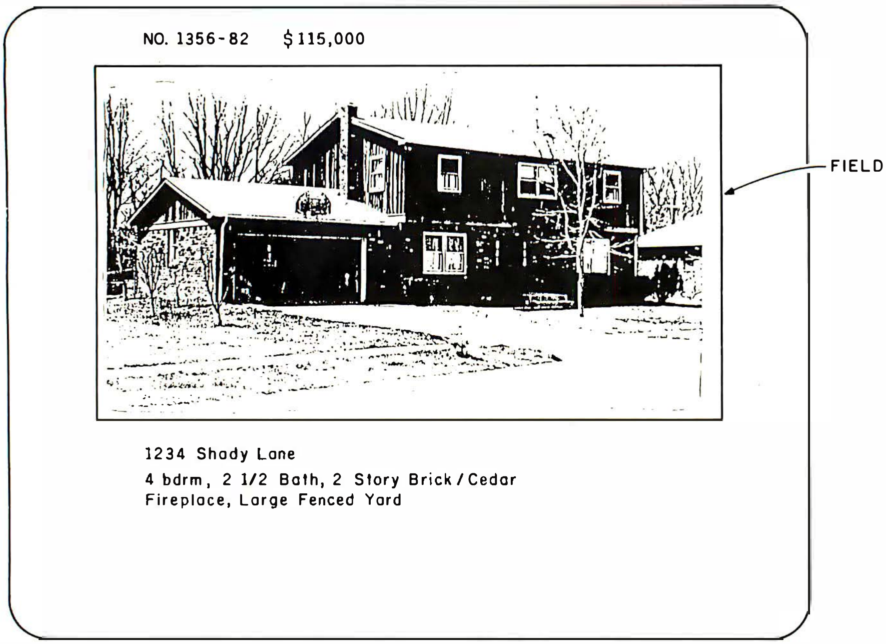


Figure 6: *The Incremental-Point command can be used to specify the color information for each point inside a field. In an application such as real-estate listings, a photographic-quality picture of a house can be included with textual information.*

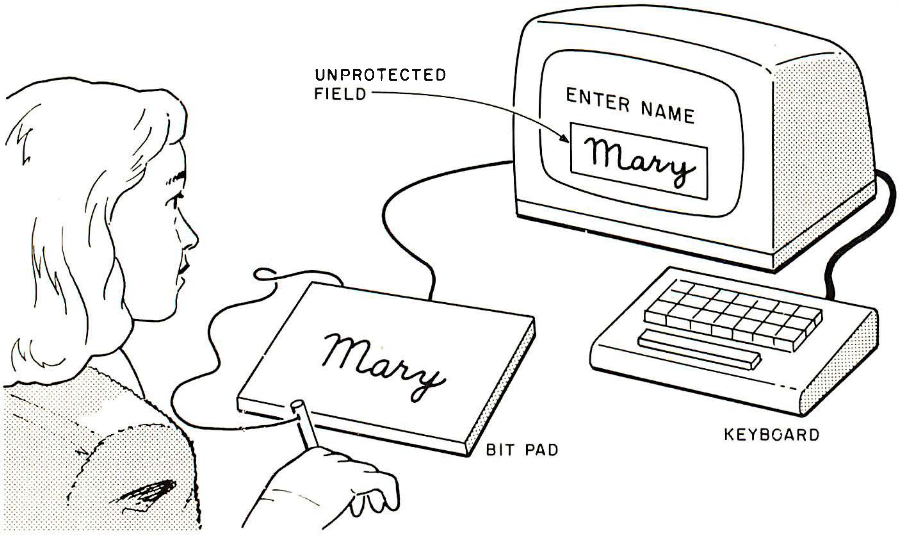


Figure 7: *Input from a bit pad can be translated into a series of Incremental-Line instructions and placed into an unprotected (user) field.*

user is allowed to enter information. The user can also edit the information with any local capabilities provided by the terminal. Once the information is entered, the user sends the contents of the field to the host.

Any legal NAPLPS stream can be placed in a field. In the example shown in figure 7, a person has used a bit pad to put a signature in the field. When the field is eventually sent to the host, the contents of the field would be an Incremental-Line command followed by a stream of data for the signature.

If, on the other hand, the user had *typed* information into the field, the information would be sent to the host as characters from the Primary Character Set.

The information that is sent to the host is identified with the location and dimensions of the field. If multiple fields are set up, the host is sent data only from the fields that are modified by the user.

The Field capability provided in NAPLPS is extremely versatile. In comparing this capability with the fields commonly found on data-processing terminals, you should note two items. First, the fields described here are true two-dimensional areas on the screen. This is quite different from the typical one-and-one-half-dimensional fields found on most terminals. Figure 8 illustrates this difference.

The other item of note is that NAPLPS places no restrictions on the user in regard to what type of information can be placed into a field. The

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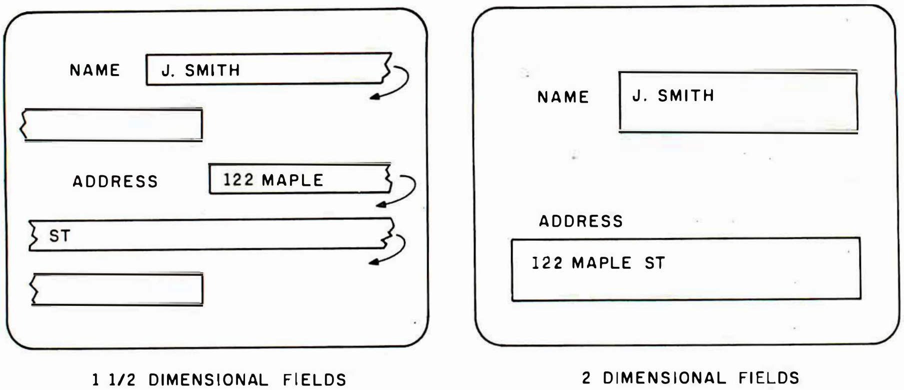


Figure 8: *An example of the one-and-one-half-dimensional fields found in most terminal systems and the true two-dimensional fields possible with NAPLPS.*

options available to the user for entering information into fields become merely terminal-dependent features. Terminal manufacturers are thus able to provide unique input and editing facilities to distinguish their products.

No facilities are available in NAPLPS to specify the type of data that can be entered into a field. Many data-processing terminals now forbid you to enter, for example, alphabetic information into a numeric field. In contrast, the spirit of NAPLPS is to allow free-form user input.

Someday host computers may become smart enough to know that "100," "One hundred," and "1 hundred" all mean the same thing. NAPLPS will be ready to accommodate this capability when it becomes available.

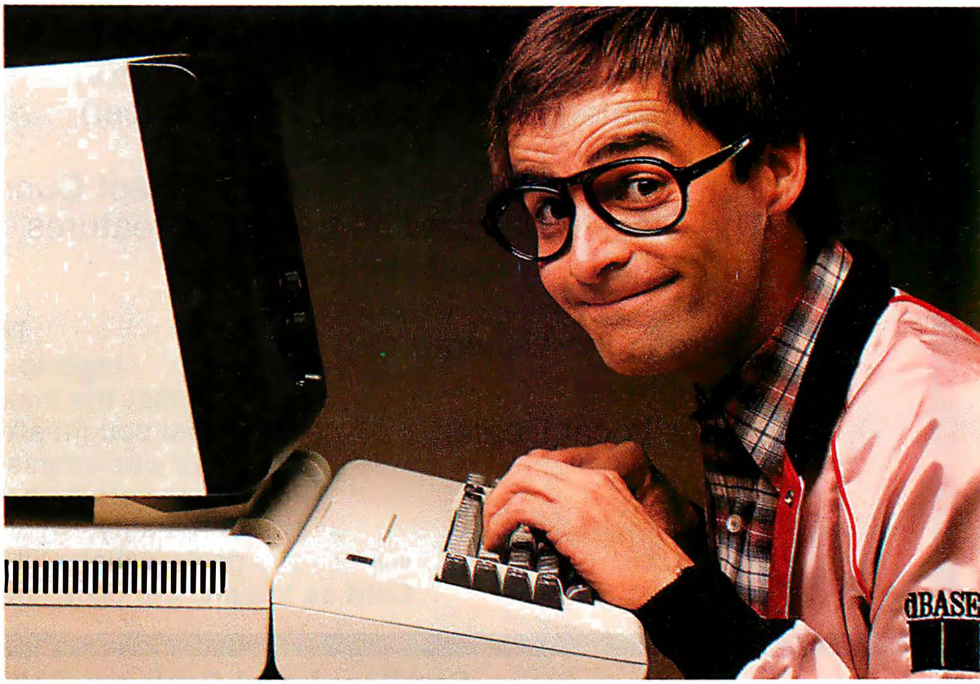
NAPLPS has many other powerful features. It is impossible to cover all the features in the context of this series of articles. As I have indicated in the past, anyone who wants more information about NAPLPS, or who is interested in doing serious work with NAPLPS, should obtain a copy of the specification. Copies are available for $18 from

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Next Month

NAPLPS offers us a powerful new communications medium, one that should have a significant impact on the amount and the *type* of information we can exchange among ourselves. Next month, I will describe some of the advanced color capabilities and speculate on the ways in which NAPLPS will affect the personal-computer user. ■

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Virtual Memory for Microcomputers

Four New Memory-Management Chips Pave the Way

Stephen Schmitt
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Not too long ago, a microcomputer system with 32K bytes of memory was considered a luxury. Because memory was very expensive, you took great pains to squeeze, pack, and cram programs into the small amount of memory that you could afford. Today, however, you can buy 256K bytes for less than $500. And new 16- and 32-bit microcomputers feature directly addressable storage spaces that are 100 to 10,000 times larger than those found in 8-bit architectures. Like the pauper who just became rich, how do you handle this vast wealth?

Another drastic change in the microcomputer world deals with software. Multitasking operating systems, high-level languages, and flexible business software have become popular. The problem is now more complex: How do we take advantage of both the increased hardware power *and* the new complex software?

Virtual-memory techniques offer one answer. Virtual memory is an automatic system for controlling very big memories. But special hardware functions are essential for building such a system. And now, single-chip memory-management units (MMUs) have been developed to provide these capabilities for microcomputers.

In the first part of this article, I will introduce some of the basic concepts of virtual memory. Next, I'll compare and evaluate four MMU chips that have recently become available: Intel's iAPX 286, Motorola's MC68451, and Zilog's Z8010 and Z8015. [This survey does not include the National Semiconductor NS16082 MMU for the NS16032 microprocessor. Because of its fairly recent introduction, the part was not evaluated for the review. The NS16082 is another interesting MMU that merits analysis.] Finally, I will discuss some implications and applications of virtual memory in microcomputer systems.

Virtual memory is a powerful concept. It allows you to consider main memory to be very large—much larger than its actual physical size.

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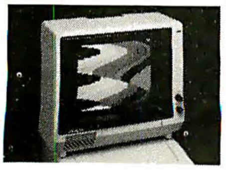
Almost every computer system has several types of memory devices that differ in speed and storage capacity. A fundamental tenet of computer technology states that memory price is directly related to its speed. Storage hierarchies thus usually represent an effective compromise between a large, slow, inexpensive memory and a small, expensive one with high access speed. Familiar examples of this are systems with relatively small amounts of fast RAM (random-access read/write memory) and larger, slower, and cheaper disk-storage devices.

Although the cost benefit of such a configuration is substantial, the efficient management of this structure presents a challenge. The movement of data between these two hierarchy levels should be minimal; otherwise, the access time for the slow memory will predominate over the speed of the fast memory. In a typical two-level system, main memory (MM) is

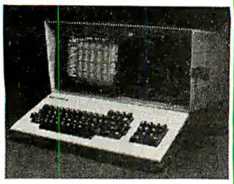
About the Author

Stephen Schmitt has worked for Hewlett-Packard and also taught at Michigan Technological University. He is now doing a review of a version of the Ada programming language for microcomputers.

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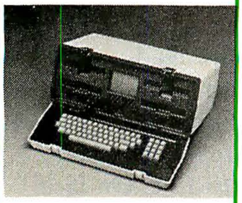


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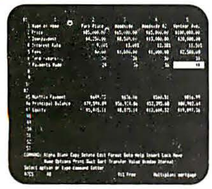
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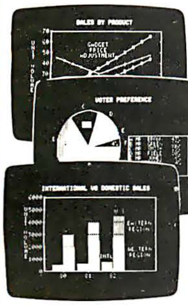
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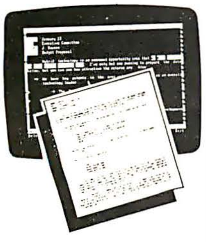


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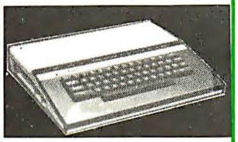
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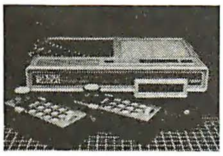


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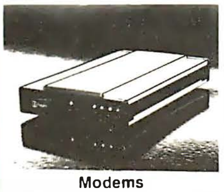


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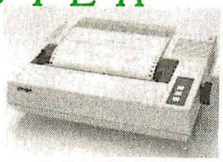
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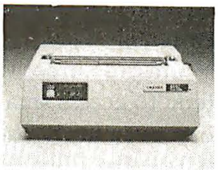
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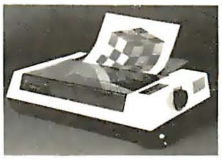


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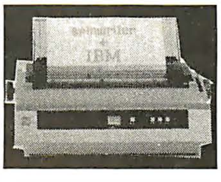


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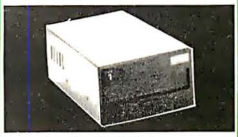


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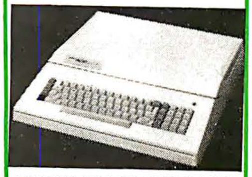
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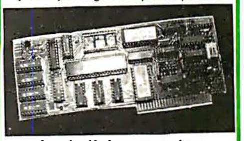
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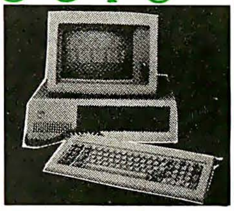
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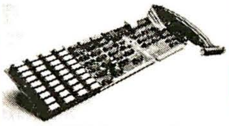


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1000 to 5000 times faster than the magnetic disks used for secondary storage. Thus, disk accesses should be as infrequent as possible if we are to take advantage of the high speed of the main memory.

Another problem is that the relatively small size of the main memory in most systems limits program size. An excessively large program must be broken into parts; each piece is loaded into main memory prior to its processing turn and returned to disk after execution. This technique is called *folding* or *overlaying*, and the task of folding programs is usually a job for the programmer. The problem is that the mechanics of defining separate program parts and adding code to control data transfer between main and secondary memory are usually cumbersome tasks. Also, the additional folding code clouds program logic. Compilers and linkers can simplify the task, but you must still design the overlay framework.

Despite these difficulties, however, folding operations are common. In fact, the word processor I'm using to write this article applies the concept twice. First, the program is too big to fit completely into memory and is divided into three overlays. Second, only a portion of my large text file resides in memory at a given time—the rest is stored on disk.

As you can imagine, manual folding consumes considerable time and effort (as much as 25 to 40 percent of programming costs). But there is a way we can take advantage of the benefits of large, sophisticated programs without spending a tremendous amount of time manually folding them to fit into small memory spaces.

Virtual Memory: Definition

Computer facilities that automatically fold programs and data between two or more memory levels are called virtual-memory systems. Virtual memory is a powerful concept. With it, you can consider main memory to be very large, much larger than its actual physical size. Intermediate files, overlays, and many file-access procedures are no longer necessary. Program logic is simpler and is focused on problem solutions, not critical resource management.

The objective of virtual memory is straightforward: to permit programs with very large address spaces to run at MM speeds. In virtual systems, main memory serves as a window (or group of windows) onto the entire address space held in secondary memory. If the window is big enough, and if it accurately reflects the active part of total memory, the technique works extremely well.

The reason for this is that programs tend to access small portions of memory over fairly long periods of computer time. This is called *clustering* or *locality of reference*. Code loops and manipulations of a data structure are examples of clusters or programs with good locality. A virtual system must detect and maintain in main memory only the *working set* of a program, that is, those locations with high activity. As activity gradually shifts to other memory regions, these areas of secondary storage are automatically accessed and brought into main memory. As you might imagine, a high rate of secondary-storage access will severely degrade performance. This is known as *thrashing*.

Address space in a typical virtual system ranges from 16 megabytes to 64 gigabytes, enough to handle very ambitious programming projects.

Benefits

Let's examine the benefits of virtual-memory management. Foremost, it removes the limit on program size imposed by main-memory size. Address space in a typical virtual system ranges from 16 megabytes to 64 gigabytes—large enough, I dare say, to handle even the most ambitious programming project! And virtual systems offer other advantages:

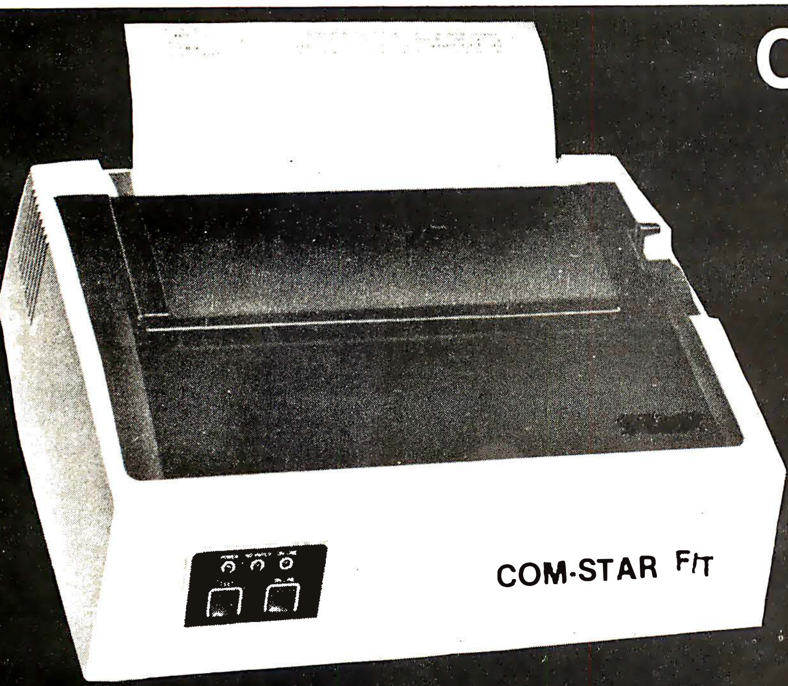
- Main memory is allocated automatically according to the demands made by a program. The user does not have to estimate memory allocation prior to execution.
- Manual folding is eliminated and replaced, in part, by high-speed hardware. Thus, programming costs tend to be lower.
- Programs execute correctly regardless of actual main-memory size. But note that the execution speed may be affected if the fast store is too small to meet average memory requirements.
- Relocation and task switching are enhanced indirectly.
- Multiprogramming environments have greater flexibility. The problem of deciding the optimal placement of programs in a fixed-size memory is reduced. More programs can execute concurrently because only the active portion of each occupies main memory. While this may induce less efficient use of the total addressable space, more effective use of the main memory is achieved.

Having outlined the motivation for virtual storage, we are ready to explore basic components of system design. The memory-control process must be transparent to normal operation and relatively efficient. On face value, you might doubt if reasonable performance is possible, but research into virtual-memory behavior clearly demonstrates the concept's potential (see reference 2). I hope to show that some practical systems can also have a remarkably simple design.

Virtual-Memory Design: Basic Concepts

Virtual storage systems require a mixture of specialized hardware- and software-control policies. I will focus on architectural features that influence virtual-memory operation. An understanding of intended applications should aid our analysis of MMU products later.

A computer's *address space* (AS) is the legal range of addresses that can be generated by its instruction set. The maximum size of this is determined by the number of bits in the processor's address register. A *logical address* is a memory specification used by the central processor. *Physical addresses*, on the other hand,



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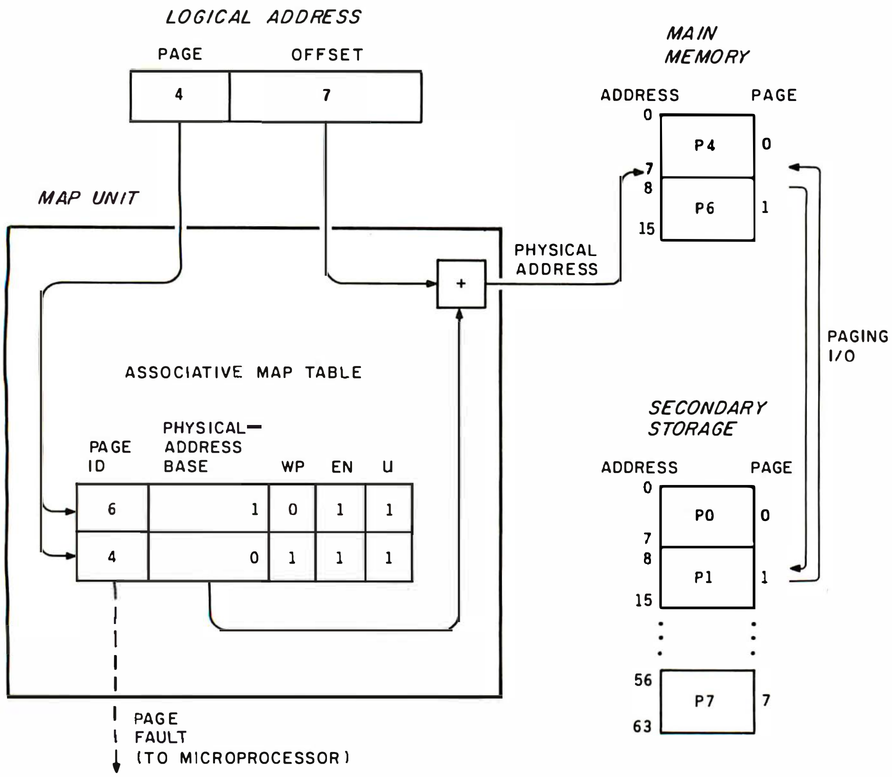


Figure 1: *The associative mapping scheme for virtual-memory systems. The central processing unit specifies a memory location with a two-part logical address that includes a page field and an offset field. The page field provides the value used for searching the map table. All cells in the table are searched in parallel. If a match is found, the selected cell's physical-address-base field is added to the offset field. A page fault occurs when there is no match. In this simple diagram, the second cell matches and translates the logical address. The attribute fields in the above map table are WP (write-protected), EN (valid main-memory page; EN = 0 only when main memory is not full), and U (used; recent page access has occurred).*

describe actual locations in the main memory. In most systems, logical and physical addresses are one and the same (as, for example, in 8-bit microcomputers). With a virtual system, however, the size of the AS can be significantly larger than main memory. The AS may be thought of as occupying a contiguous area in secondary storage; and logical addresses no longer correspond exactly to actual physical RAM locations.

In a virtual system, main memory contains changing portions of AS. At various times, an instruction may address a part of the AS that is not contained in main memory. This is known as a *page fault*. A virtual-memory system must be able to detect a page fault and move the desired part of the AS into main memory. Then, when that part is subsequently addressed by an instruction, the system must be able to translate that part's logical address into its present physical address in main memory. This is known as the *mapping process*. Both these processes, page-fault detection and mapping, are fundamental to every instruction step. They must therefore be performed by high-speed hardware.

A page fault stops execution of the current activity that the central processor is performing (e.g., fetching an instruction or processing operand data) until the absent memory is brought into MM. A page fault is similar to an interrupt except that it may occur partway through instruction processing. Thus, special processing logic is needed to handle partially executed instructions (consider the problems associated with restarting a MOVE BLOCK instruction).

In a virtual system, memory can be

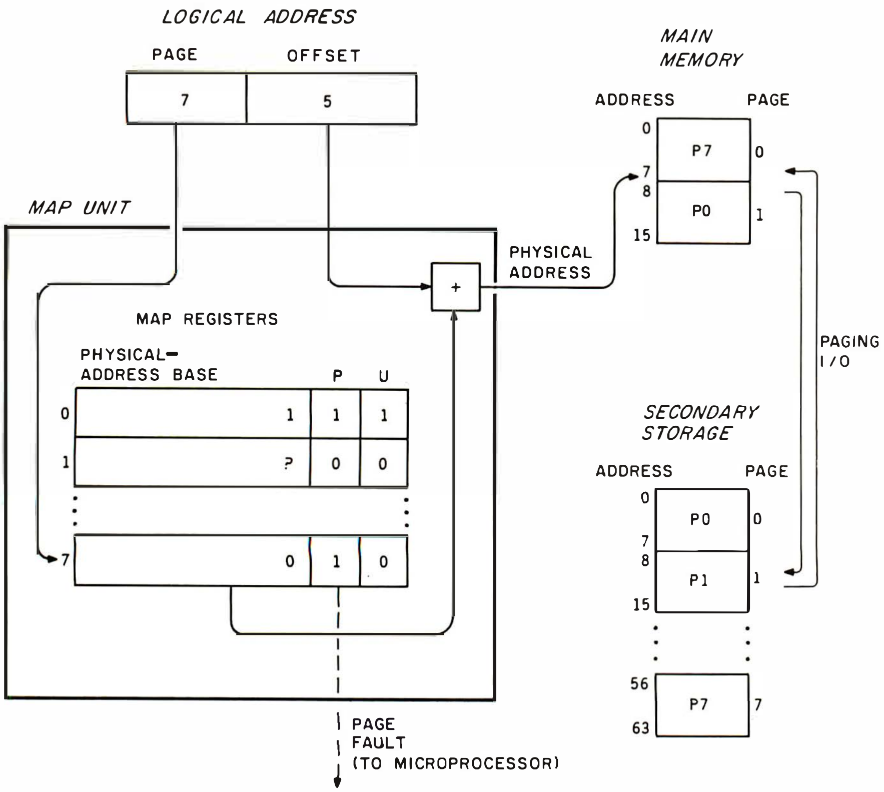


Figure 2: *The mapping-by-address (or mapping-by-register, MBR) scheme for virtual-memory systems. This is similar to associative mapping except that each map cell is a register that refers to a page in secondary storage. In this simple example, the page field in the logical address refers to register 7, which in turn refers to page 0 in main memory. If register 1 had been accessed instead, a page fault would have occurred (P = 0). Page 1 would then be placed into main memory, probably in the space now occupied by page 7, because page 7 has not been accessed recently (U = 0).*

divided into either *pages* or *segments*. A paged policy divides memory (both AS and MM) into equal-size blocks. The rationale for pages relates to the clustering principle. Memory activity occurs in scattered parts or clusters of the AS. By organizing storage into pages, you can "break out" the busy sections and place them in main memory. Paging, like disk blocking, also implies a smaller number of data transfers between disk and main memory.

Segments are merely pages of variable size. Segments can closely model program units because code modules and data structures vary in size (as do clusters). Trade-offs exist between page and segment organizations. I'll discuss these later. For now, you can ignore the distinction and call both pages.

Several mapping schemes exist for virtual systems. Figures 1 through 3 illustrate three common techniques. In the examples, logical-address fields are composed of two parts: a page field and an offset field. The logical page number is translated into a physical location by the map unit. Adding the offset field to this location forms the complete physical address. A simplistic memory model will be used to show the basic operations of each technique.

Associative mapping is shown in figure 1. The logical-address page field is compared, in parallel, to all page entries in the map table. If an entry matches, its corresponding physical-page address is combined with the offset value to form the complete physical address. A page-fault condition is raised when no match occurs. The problem with associative maps is that they are expensive. High-speed register memory with integrated comparative logic is needed; translation has to be fast and transparent. The associated map has to be as large as

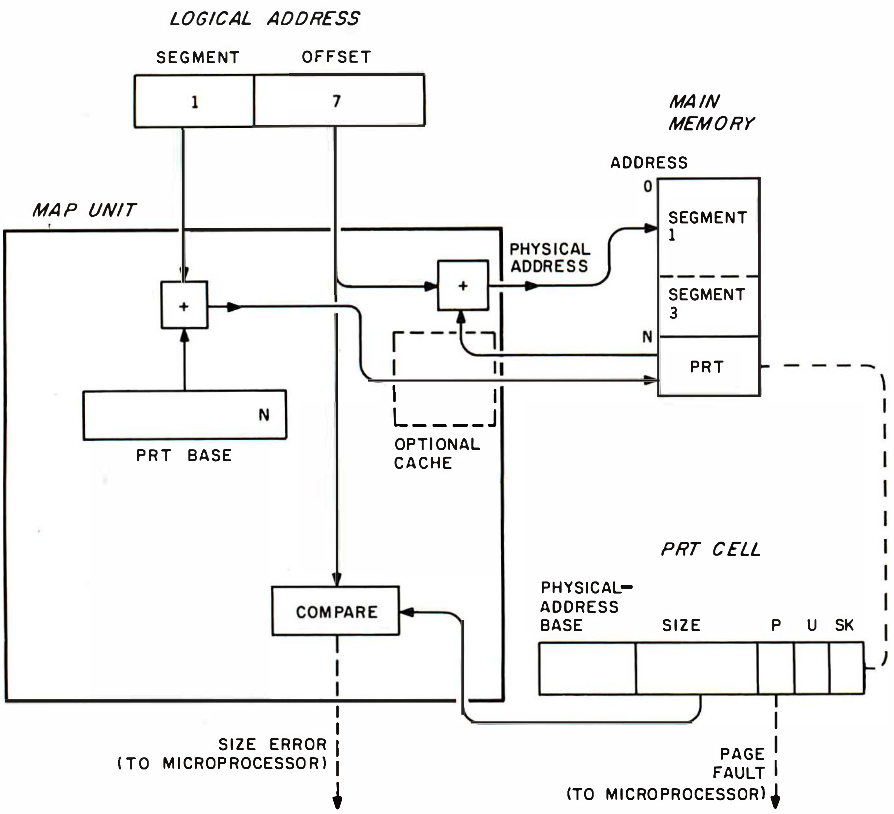


Figure 3: *The segment map table scheme for segmented virtual-memory systems. In this mapping scheme, information on each segment of a program in secondary storage is kept in a program reference table (PRT) in main memory. The location of the PRT is stored in a PRT Base register. In this simple example, the segment field in the logical address is added to the contents of the PRT Base register (N). This refers to a map cell at location N + 1. In this map cell is a physical-address base that is added to the offset to obtain the desired address in main memory. Note that bounds-checking can easily be done by comparing the offset with the size field. Also, note that things can be speeded up by placing the most active map cells in a small associative cache memory. The attribute field SK indicates a stack segment (i.e., the offset orientation is reversed).*

the number of MM page frames. If you change the size of main memory, you have to change the map size accordingly. Associative mapping works best for systems with a large number of AS pages and a moderate-sized, fixed main store.

Figure 2 illustrates *mapping by address* or mapping by register (MBR). In this technique, the logical-address page field refers to an array of high-speed registers. These registers hold status and physical-address information. Mapping by address is analogous to indirect memory addressing except that the registers permit very high processing speeds. Page faults are detected when the addressed register's "present" bit is clear. The problem is that every page in the AS requires a corresponding map register. Fortunately, the economy of conventional registers offsets the mapping array size. Note that the mapping hardware is unaffected by changes in MM size. For relatively small address spaces, mapping by address is quite attractive.

The last technique I'll present applies to segmented systems. Figure 3 defines the operational details. This design is based on the Burroughs Corporation B5500 mainframe. This approach gives you more flexibility, but is slightly more complex and necessitates additional hardware (for the

Field	Abbreviation	Description	Field Size (bits)	Memory Structure (Segment vs Page)
Present	P	Indicates if page is present in main memory	1	Both
Used	U	Indicates if page has been recently accessed	1	Both
Dirty	D	Indicates if page has been modified	1	Fixed-page
Type		Various page properties	1–4	
	RP	Read-protected		Both
	WP	Write-protected		Both
	EX	Executable code		Both
	SH	Shared		Segment
	SK	Stack memory		Segment
	OW	Overflow warning		Both
Size	SZ	Size of segment	16–32	Segment
Priority or mode	PR	Indicates task priority or system context to permit access	1–8	Both
Virtual time	LREF	Time of last access to page	12–32	Both
Task ID	TID	Identifies task(s) that owns the segment	8–16	Segment
Fix	F	Indicates that page is not to be replaced	1	Both
I/O access	IO	Protect or hold page for input/output	1	Both
Enable	EN	Indicates valid pages for access (when main memory is not full)	1	Both

Table 1: *A summary of the control and status information used by virtual-memory mapping units. Most mapping schemes use a subset of these different attribute fields.*

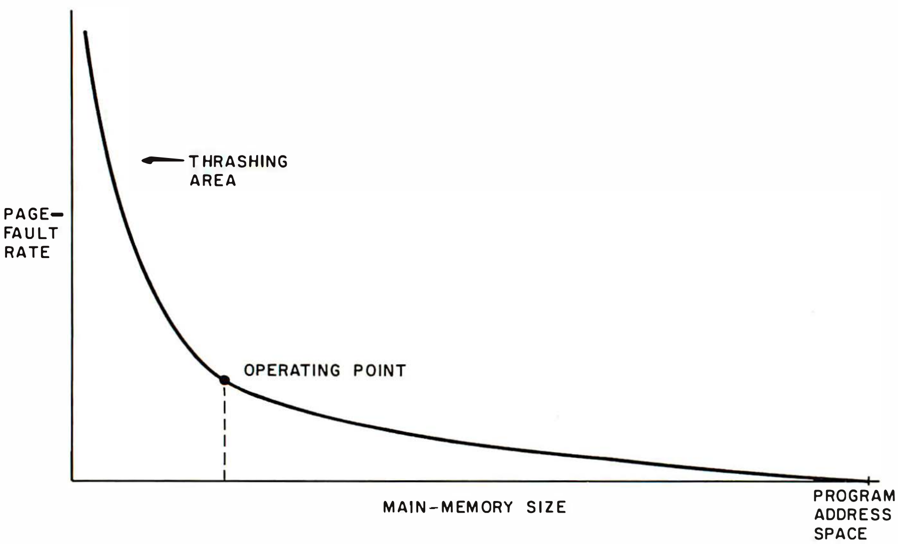


Figure 4: *A graph showing how the page-fault rate (i.e., the rate of accesses to pages not present in main memory) is related to the size of main memory. The operating point is the memory size sufficient to hold a program's most frequently accessed routines—its working set. Adding memory past this point has little effect on the page-fault rate. Of course, as the needs of a program change, the operating point will shift.*

segment-size field and the *program reference table* or PRT). A segment field replaces the logical-address page field. You can have any number of system segments; MM and AS sizes do not constrain the choice. Translation is similar to mapping by address. The program reference table contains the size and location for each segment. It resides in main memory for two reasons: (1) to allow a large number of segments, and (2) to avoid the high cost of registers that would be wide enough to hold extra mapping data. The table acts like mapping registers, with the segment field—not the page field—providing the index address. At first glance, it looks as if the scheme is twice as slow as the others because every reference needs two memory accesses (one for the PRT and one for the actual data). But this problem can be handled by putting a small buffer-register set in the MMU. Keeping copies of the most active PRT entries in this high-speed buffer greatly increases mapping speed.

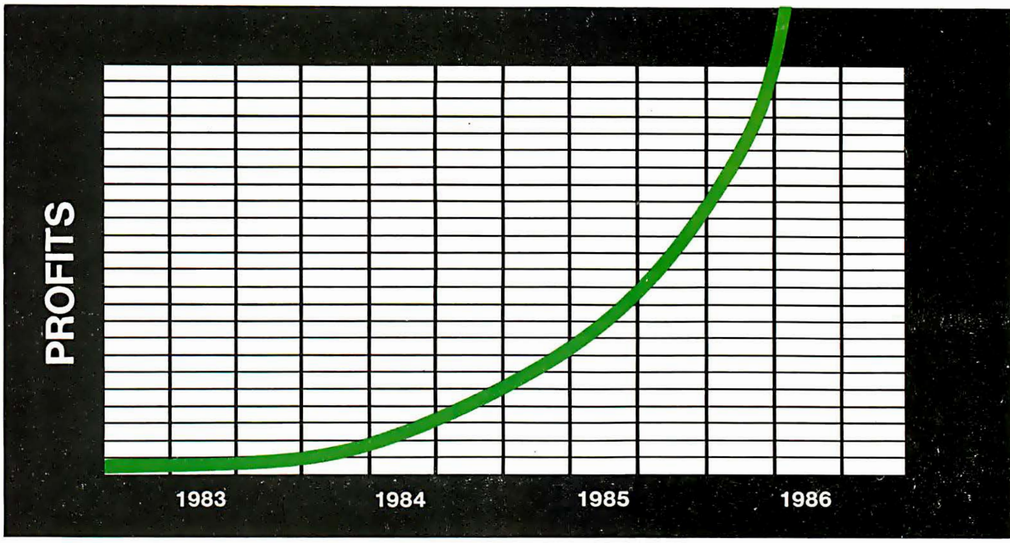
Besides translating addresses, mapping units also provide other functions. They hold information to aid memory management and data protection. Table 1 is a list of information found in various mapping systems. Each virtual system uses a subset of these items, determined by the particular mapping scheme used and the memory-control functions.

Up to now, attention has centered on the hardware aspects of virtual systems. Now, let's consider the memory-management and software requirements for virtual systems.

Paging Policies

As mentioned previously, a minimal amount of secondary-storage access is central to a virtual system's viability. Figure 4 shows a graph of disk activity versus main-memory size allocated to a program. From the graph, we see that given enough main memory, disk access approaches zero. However, a primary aim of virtual memory is to provide a huge address space while minimizing expensive main memory. To satisfy both conditions, you must operate at a point just below the "knee" of the

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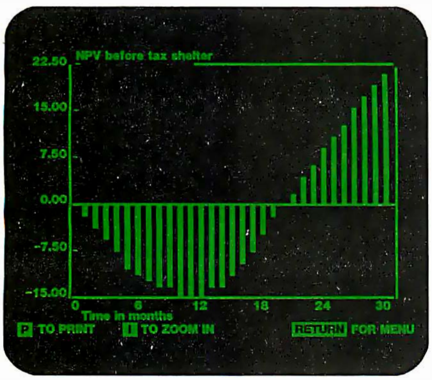
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curve (labeled operating point). The locality principle states that the amount of MM needed at any given time is but a small portion of AS. Hence, if you keep the active cluster or working set in memory, thrashing and main-memory needs are minimized.

Sounds simple, doesn't it? Alas, a few minor problems "gum up" matters. For openers, measuring a system's working set is a dynamic process. The size and contents of a working set change rapidly. Keeping track of working sets involves considerable time, resources, and problems. Just how is this working set determined? At what times do we change the working set to reflect locality movement? What happens when several programs are running or there is program I/O? All these problems are handled by a *paging policy*.

Basically, a paging policy does three things:

- Fetching—decides when to transfer pages from secondary storage to main memory
- Placement—determines which MM page frame should hold the fetched page
- Replacement—when main memory is full, chooses which MM page frame should be replaced by the fetched page

In regard to fetching, research has found that demand paging is generally best. When a page fault takes place, you fetch the desired page from secondary storage. The placement decision is resolved automatically by mapping hardware. The last issue, however, choosing which page to replace, is the hard part. The replacement policy affects how well we address the other concerns mentioned above.

Page-replacement techniques, which determine the set of main-memory pages, are all approximation algorithms. This is so because you can't calculate the best page to remove without some future knowledge of which page will be required. The optimal algorithm (OPT), or Belady's algorithm, replaces the active page that is next referenced the furthest into the future. Even though totally impractical, it is a benchmark for comparing other techniques.

Page-Replacement Algorithms

Virtual-system performance is very much dependent on the page-replacement technique that is used. Because the process selects departing pages, it indirectly determines the pages remaining in main memory. If the algorithm closely models a system's actual working-set memory demand, few page swaps will result. Algorithms usually base removal choices on prior reference activity, because the locality principle implies that past behavior approximates future needs (at least over short time periods).

Here I will discuss four specific page-replacement algorithms: Least recently used (LRU), Clock, Generalized working set (WS), and WS-Clock.

The LRU Algorithm

This page-replacement policy is conceptually related to the optimal algorithm. Instead of selecting the page with the furthest time until next access, you pick the page whose last reference occurred longest ago. If not used for a long time, the probability that the page will soon be referenced is small. When a page fault happens, you scan the map cell for each page and replace the page having the smallest (oldest) virtual time.

To implement LRU, the memory-management hardware must support two features: a virtual time register in the map unit and the ability to update the page access time during address translation. The time register should be wide enough to ensure sufficient resolution. In addition, the necessity of associating a time stamp with every memory reference dictates high-speed logic and added map complexity.

The LRU algorithm works well. Its performance is much better than that of an arbitrary replacement policy or many other paging policies. But because LRU is a *global policy*, it can exhibit anomalies in multitasking systems. For example, global LRU tends to save pages of the task last executed

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and favors jobs with smaller locality; low-priority tasks and large programs may experience reduced throughput.

Computer systems using LRU include the CDC Star-100 and the Multics drum-to-disk control. Microcomputer MMU parts lack the hardware mechanisms needed for a "pure" LRU policy.

The Clock Algorithm

This algorithm is a variation of the LRU algorithm. Main-memory pages are logically ordered in a circular list. You can envision each page as a unit marking of a clock face. A pointer or hand always points to the last page replaced. On a page fault, you advance the pointer clockwise to the succeeding page. Then you check and clear that page's *used* bit. If the bit was set (i.e., the page was used recently), scanning continues; otherwise, the frame is not recently used and replaceable. If the replaceable page has been changed (or *dirty*), you must schedule it for transfer back to secondary memory. Scanning stops when a clean, not recently used page is found, and the pointer is left at the chosen page. A replaceable page is not processed if accessed before the disk transfer.

Studies indicate that the Clock algorithm closely simulates LRU replacement, and the hardware needed is inexpensive. As implied above, only 2 flag bits per cell are required (changed and used). Software complexity and overhead are small. Calculations are trivial and the average number of scans per page fault is a fraction of total map size. Many successful mainframe systems, including the IBM 370 and Multics, use Clock algorithms. However, you should note that deficiencies of LRU apply equally to Clock. The technique offers a simple mechanism and good efficiency; but, as you shall see, other paging algorithms exhibit even better performance characteristics.

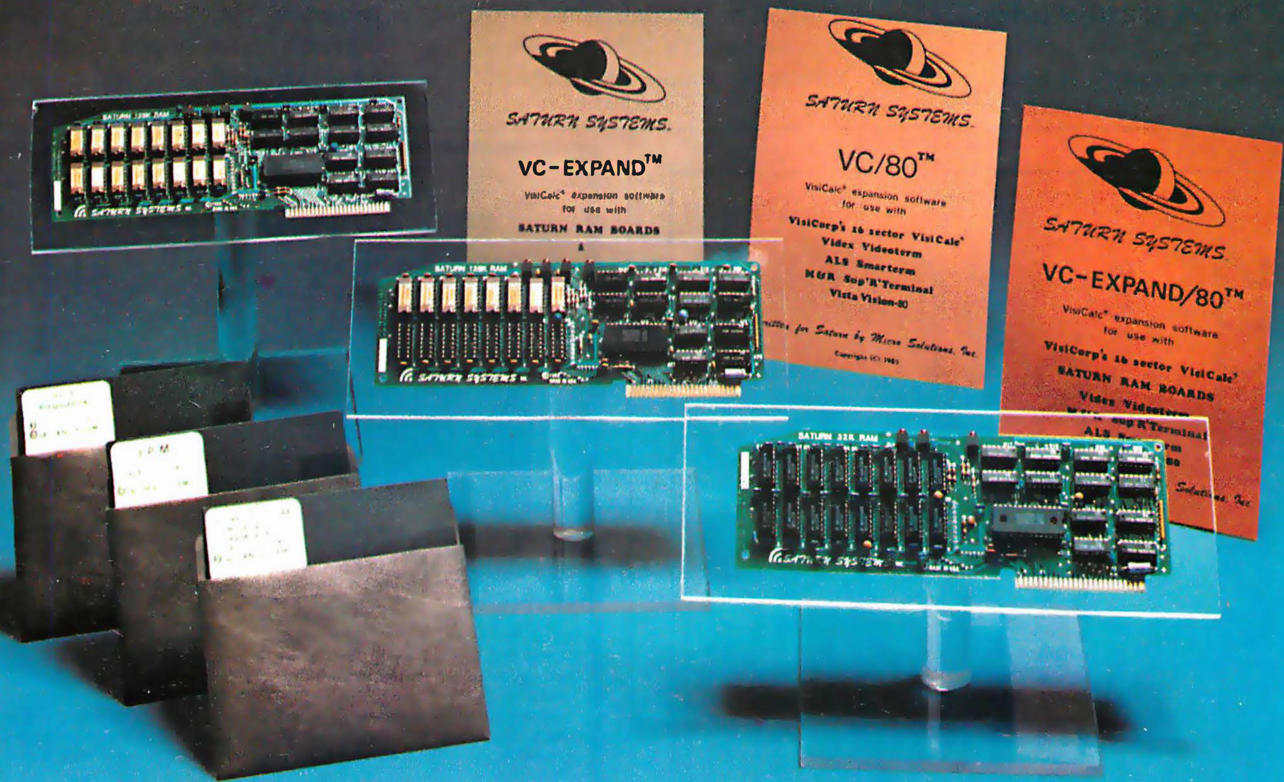
The WS Algorithm

This page-replacement algorithm represents the most practical policy according to empirical studies. WS is so named because it approximates the working-set locality model. In WS, any page referenced within a specified time (designated as Θ) is regarded as a member of the working set. Real working sets of course have variable durations, but if the WS time-control value (Θ) is properly chosen, a real working-set model can be closely approximated.

I will briefly highlight WS operation (see reference 1 for details). The WS policy defines a working set (W) to be those pages of the AS that have been referenced within the previous Θ time units. In order to determine when a page (p) in main memory is no longer in W, and thus is replaceable, we need two things: (1) a procedure to calculate a time value (L) equal to the owning task's current execution time (ET) minus the last reference time for every AS page, LREF(*p*), and (2) a scan mechanism to check for values of L greater than or equal to Θ. Calculating L can be done with page-frame counter registers. When the page is accessed, its counter register is cleared. Then, at fixed intervals, a global broadcast pulse increments all the counters. The scan operation can run at various times (e.g., at fixed intervals or when a page fault occurs). Pages marked as replaceable become part of the available pool (AP). The page-replacement algorithm merely selects some page from the AP and replaces it. If the AP is empty, the system must suspend a task to free pages.

Although WS accurately models dynamic-memory demands, the computational overhead and extra hardware support it requires diminish the algorithm's viability. Space for the LREF(*p*) field can effectively double page-table size. Moreover, the counter mechanism is relatively expensive. Scanning requires inspection of each map cell at regular intervals, and AP maintenance adds more control functions. On the plus side, the local scope of WS enforces more consistent multitasking management. And pure WS simulations perform better than other policies. Research systems have implemented practical WS schemes and observed substantial

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improvements over Clock techniques. The parameter Θ allows you to "tune" a virtual system for different applications. Also, investigations have found that use of the constant value Θ deviates less than 10 percent from an optimal WS.

WS is technically appealing, but design difficulties detract from its advantages. Like LRU, classical WS is impractical for microcomputer application. But the next technique surveyed approaches WS performance and is feasible for microcomputers.

The WS-Clock Algorithm

WS-Clock combines the best properties of Clock and WS. Additionally, the new strengths offset some problems of the separate procedures:

- the extra scanning required by WS is replaced by a simple Clock mechanism
- WS-Clock is a local policy
- LREF(p) registers are needed only for main-memory pages, not for every AS page
- the available pool (AP) is eliminated

This algorithm organizes page frames in a circular list like Clock. The clock pointer identifies the page replaced during the last scan. When a page fault occurs, the scan advances clockwise to the next page. The used bit is checked and cleared. If the bit was set, you reset the page's LREF(p) to the owning task's accumulated execution time (ET). Otherwise, if the used bit is clear and if $L = ET - LREF(p) >= \Theta$, you remove the page from W. If dirty, a replaceable page is scheduled for disk transfer and not replaced. Scanning halts when you encounter a clean, replaceable page.

WS-Clock approximates WS replacement, and W for the two policies becomes equivalent when the task executes for Θ units of time. Performance differences appear negligible and can be ignored. Thus, WS-Clock approaches WS behavior with a significantly simpler mechanism. The average number of frames examined per page fault compares favorably with WS. And to implement WS-Clock, you need minimal map hardware: a used bit, a dirty bit, an LREF field, and a task ID descriptor.

Multitasking and Load Control

In a multitasking system, virtual-memory management must coincide with general resource-sharing policies. The problem is that in a dynamic multiprocessing environment, wide variations in programming level and memory demand occur. Every active task consumes a portion of total memory (in both MM and AS). At some point, adding another task will push MM demand past the ideal operating point in figure 4 and trigger the onset of thrashing. Left unchecked, throughput diminishes rapidly. Accordingly, you must either prevent the "overcommitment" of memory or recognize the condition and make corrective adjustments. This is done by a load-control policy.

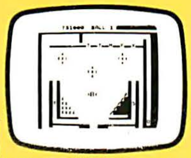
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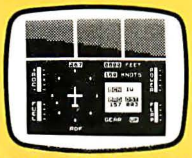
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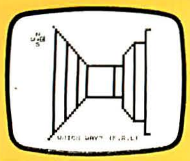
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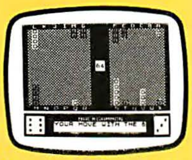
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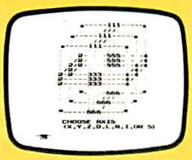
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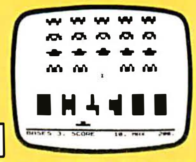
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Function or Characteristic	Memory Structure: Segments	Memory Structure: Fixed Pages
Flexibility	+ Can model pages, has more design options, promotes protection, data sharing, and so on	– Lessens "tuning" options, trade-off exists between efficient I/O blocking and memory waste
Hardware requirements	– Cost and complexity fairly high	+ Lower cost, simpler hardware
VS(1) systems	+ Better security	+ Simpler design
VS(n) systems	+ Segments are mandatory for VS(n) designs	0 Not applicable
Mapping unit		
Map-register size	– More space needed for size fields	+ Minimal
Table size	+ Fewer frames needed if segments are large	0 Larger pages result in memory waste
Memory management overhead	– Extra logic needed to close "holes" and to manage extra attributes	+ Placement simple
Allocation policy	+ Make segments the desired size	0 More complex, but no main-memory waste
Protection	+ Superior—facilitated by extra attribute fields	– Pages do not correspond to program "objects"
Sharing	+ Direct support	– Much harder
I/O efficiency	0 Depends on segment size	+ Facilitated by relating page size to disk block size
Memory usage		
Internal fragmentation	+ None	– Some main memory wasted
External fragmentation	0 Can reclaim with "garbage collection"	+ None
Page-fault rate	+ Lower rate	0 Depends on page size

Table 2: *A comparison of the relative strengths and weaknesses of segmented and fixed-page memory organizations. The +/– column indicates approximate merit: (+) good; (–) poor; (0) okay or does not apply.*

Load control is sensitive to page-replacement strategy. Local strategies estimate each task's independent memory needs and allocate sufficient main storage to hold the locality set. Global page-replacement strategies discriminate in favor of the most recent task's memory set and can lead to thrashing.

System Design: Issues and Options

Virtual memory reflects a composite of hardware, resource management, and programming processes. We now turn our attention to alternatives that can affect overall microcomputer system design.

VS(1)

A fundamental system decision is whether you treat the large virtual address space as a shared resource divided among the several active jobs or whether each process is provided a separate AS. The first class, termed VS(1), extends the idea of a conventional operating system where supervisor, system resources, and user tasks occupy one large address space. Software compatibility with nonvirtual systems is a major benefit of this system. System complexity is minimized and a single mapping table can define AS structure.

VS(n)

VS(n) systems give each executing task a unique AS. To support this feature, every job has its own mapping table. Typically, a mapping-table origin register (MTOR) points to the mapping table of a running task. When switching tasks, you change the MTOR and reload the mapping hardware. A VS(n) system gives you, in effect, several virtual machines, each using the same physical resources, running concurrently. VS(n) systems also give you improved system integrity and data protection.

Page Size

An important design consideration is block memory structure. If you select a fixed-page structure, you must determine the number and size of page frames. Secondary storage transfers data in fixed-size units. Hence, for efficient paging memory frames should be an integer multiple of a disk block. Big pages reduce disk overhead and map hardware. On the other side of the coin, however, a large number of small pages lowers page-fault rates and increases the number of locality sets. Some compromise is in order. My research indicates that 1K- to 4K-byte pages are considered optimal.

A segmented address space reflects programming features such as scope rules, data encapsulation, modularity, and so on. Pages, being constant in size, usually waste some memory, a condition termed *internal fragmentation* (e.g., a 5K-byte program takes two pages in a system with 4K-byte pages—3K bytes are unused). Although segments avoid this problem, they are prey to a form of waste called *external fragmentation*. Because variable-size units are allocated, program termination leaves holes of unused space. You must close up these areas periodically to provide sufficient space for large segments. Consequently, the procedures to reclaim these holes add to operating overhead. In general, segmented schemes offer more flexible designs while page organizations make for easier memory management. Table 2 summarizes trade-offs between page and segment organizations.

Many other topics related to virtual memory have not been covered: operating-system interaction, I/O considerations, page locking for nonswappable memory, disk-access properties, and more—the subject is rather deep. However, the topics

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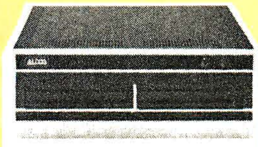
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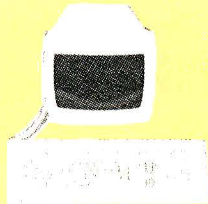
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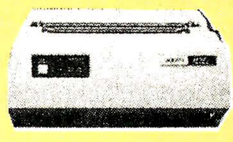
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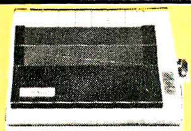
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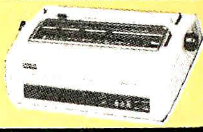
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FUNCTIONAL CHARACTERISTICS	MEMORY-MANAGEMENT UNITS			
	Intel iAPX 286	Motorola MC68451	Zilog Z8010	Zilog Z8015/PMMU
Address-translation delay (10 MHz)	0–1.5 μs	100 ns	60 ns	70 ns
Supports multiple MMUs?	No	Yes	Yes	Yes
No. of MMUs needed to map address space	1	1	2	Depends on MM size
No. of unique address spaces possible (no. of users)	Unlimited	256	8	8
VS(n) support?	Yes	Partial	No	No
Priority levels	4	0	0	0
User/supervisor modes available?	No, uses priority levels	Yes	Yes	Yes
Data sharing?	Yes	Yes	Limited	No
MMU control method	Special instructions	I/O program	I/O program	I/O program
Fault restart data	None	Limited	Moderate	Extensive
Control and status attribute names (dash indicates not supported)				
Present	P	—	CPUI	—
Used	A	U	Ref	Ref
Dirty	—	M	Chg	Chg
Write-protected	W	WP	RD	RD
Read-protected	R	—	—	—
Executable code	E	—	Exc	Exc
Shared	—	AST	—	—
Stacked memory	ED	—	DIRW	DIRW
I/O access	—	—	—	DMAI
Overflow warning	—	—	DIRW	DIRW
Virtual time	LREF	—	—	—
Task ID	(Yes)	(Yes)	(Yes)	(Yes)
Fix	F	—	—	—
Enable	—	E	—	Valid

Table 3: *A comparison of the functional characteristics of the four surveyed memory-management units.*

covered should give you the perspective to analyze the capabilities of the new memory-management units for microcomputer virtual-memory systems.

Memory Management

The need for a memory-management unit (MMU) derives from two concerns: efficient control of large memories and support for multiprocessing environments. We can summarize the major goals of memory management as follows:

- Memory allocation—Allocation policies determine what portions of memory are committed to particular tasks. Address translation allows you to treat physically separate blocks as logically contiguous. Dynamic allocation, which adds memory during execution, is a valuable feature. A virtual system's large address space makes allocation less of a concern.
- Program relocation—Relocation hardware permits a program to load anywhere in physical memory without changing the logical addresses. Systems that swap tasks to disk may need to relocate a program when it's reloaded.
- Protection—This prevents inadvertent or unauthorized destruction of data. Also, one task cannot interfere with another's operation.
- Data sharing—Controlled access to common data or code.
- Multitasking—Several tasks can logically occupy main memory during a given time frame.

Virtual memory is just one of several approaches to memory management. Another approach is *dynamic mapping*, a technique used to extend the address space of limited-address machines (e.g., the HP-1000 or DEC PDP-11 minicomputers).

A Survey of MMU Chips

The main thing we'll look for when examining these MMU products is how well they implement virtual-memory concepts. We'll review four products: Zilog's Z8010 and Z8015, the Motorola MC68451, and Intel's iAPX 286 processor/MMU. The Zilog chips are to be used primarily with the Z8003 16-bit microprocessor for virtual storage. The MC68451 MMU is designed to work with the soon-to-be-released MC68010 processor. Finally, the iAPX 286 represents a combination of both an 8086-compatible processor and an integral memory-management unit.

The Z8010, MC68451, and iAPX 286 feature segmented-memory architectures. The Z8015, however, is designed specifically for a fixed-page virtual-memory system. All four units support a 16-megabyte physical-address space. Logical-address spaces range from 8 megabytes for the Zilog chips to a whopping 1 gigabyte in the iAPX 286. Tables 3 and 4 compare the basic properties of these chips on a point-by-point basis. As the tables show, there's quite a bit of diversity. For each MMU, I'll point out its unique characteristics, operation, and programming details. Later I'll describe some applications for virtual memory.

The Zilog Z8010

The Z8010 was one of the first single-chip MMU devices on the market. As a consequence, it has a few flaws that have been corrected on newer products. In fact, virtual memory appears to have been an afterthought for this chip because you will need extra hardware to handle the Z8000 microprocessor's page-fault procedure. Still, the product does have good protection features, and it directly supports a supervisor mode for operating-system functions. Another virtue is its fast translation time.

The Z8000 architecture defines logical addresses for 128 segments,

Text continued on page 234

LET THE "ANGEL"™ DO THE WAITING........................



"ANGEL" is compatible with almost all Micro-Computers, including IBM, Apple, TRS-80, Vector Graphic, NorthStar, Altos, Xerox, Heath, Zenith, NEC, DEC, etc., with RS-232 serial, Hardware Handshaking, or Centronics compatible parallel inteface. The manufacturer reserves the right to change the product specification.

Connect an "ANGEL" between your computer and your printer, and let the "ANGEL" do the waiting ....

Your valuable computer spends 95% of its time waiting for the printer to catch up...and while the computer waits, the payroll continues.

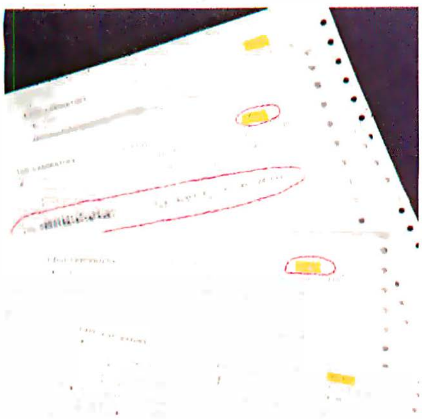
The computer sends data to the "ANGEL" at speeds up to 19.2K baud. The "ANGEL" stores data and sends it to the printer at a speed the printer can handle, and your computer is free to continue working without interruption.

A USER WRITES:

"I tried the "ANGEL" with my Altos system connected to an Epson MX-100, both set at 9600 baud. Without the "ANGEL" it takes 30 minutes to print 210 doctors' requisition forms. With the "ANGEL" installed, my computer is free after 90 seconds."

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PAGE REPRINT is another unique feature. EXAMPLE: You are printing a 32 page report, and the paper jams at page 11. Reset the printer to the top of the form, press PAGE REPRINT, and resume printing at the top of page 11. Want to restart two pages back? Press PAGE REPRINT twice, and you resume at page 10.



PAGE REPRINT

...And think of these other possibilities:

HEX DUMP. Display or printout every bit of data your computer sends out to the printer in an easy-to-read Hexidecimal and ASCII format. A must for your programmer.

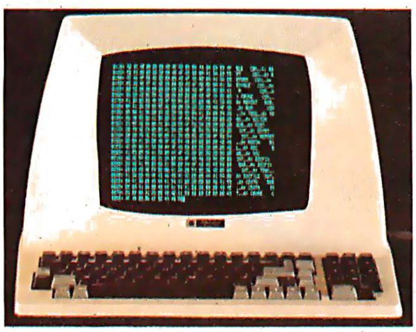
Pause and Hold for real time programs.

Page skip for selective printing. What a waste to print the entire documentation if you only need part of it.

Simple external switch settings, let the "ANGEL" accept either RS-232 serial or Centronics parallel data and can output either/or in any combination, (S-S,S-P,P-S,P-P). The "ANGEL" is compatible with almost all Micro-Computers, and can be installed by anyone in minutes. Switches are clearly marked for ease of operation, and a concise, USER FRIENDLY operator reference card is included with each unit.

The "ANGEL" has a full one year limited warranty.

THE "ANGEL" WILL NEVER KEEP YOU WAITING!



HEX DUMP

The chart shown here illustrates the features of the "ANGEL" compared to other buffer devices. When compared with the "ANGEL", the others just don't measure up. Sorry guys.

Feature	ANGEL	MICRO-FAZER **	SPOOL/64	MICRO-BUFFER IN-LINE	SOOPER SPOOLER SERIAL **
Price	295.00	330.00	319.00 w/o serial	349.00	603.00
Memory Size	64K	64K	64K	64K	62K
Max Baud Rate	19.2K	?	N/A	19.2K	?
Serial-Parallel	Yes	*	No	*	*
Parallel-Serial	Yes	*	No	*	*
Parallel-Parallel	Yes	*	Yes	*	*
Serial-Serial	Yes	Yes	No	Yes	Yes
Copy	Yes	Yes	No	Yes	No
Reset/Clear	Yes	Yes	No	Yes	Yes
Pause/Hold	Yes	No	No	Yes	No
Page Skip	Yes	No	No	No	No
Page Reprint	Yes	No	No	No	No
Continuous Copy	Yes	?	No	?	No
Self-Diagnostics	Yes	?	?	?	?
Hex-Dump	Yes	No	No	No	No

* Can only be configurated for one of the four Modes:

**Information based on available specifications from manufacturer's advertisement as of December, 1982

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You could draw attention to yourself by writing programs *for* the IBM Personal Computer *on* the IBM Personal Computer. Because all our advanced features (see the box at right) make it faster and easier to do so.

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Have musical accompaniment as well.

It's easy, because BASIC controls the built-in speaker with a single command.

Utilize the ten, programmable function keys. Try F3 to paint. F4 for lines. F5 for circles. Or F6 for boxes.

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User Memory
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Microprocessor
16-bit, 8088*

Auxiliary Memory
2 optional internal diskette drives, 5¼" 160K bytes or 320K bytes per diskette

Keyboard
83 keys, 6 ft. cord attaches to system unit*
10 function keys*
10-key numeric pad
Tactile feedback*

Diagnostics
Power-on self testing*
Parity checking*

Display Screens
Color or monochrome
High-resolution*
80 characters x 25 lines
Upper and lower case

Operating Systems
DOS, UCSD p-System, CP/M-86†

Languages
BASIC, Pascal, FORTRAN, MACRO Assembler, COBOL

Printer
All-points-addressable graphics capability
Bidirectional*
80 characters/second
18 character styles
9 x 9 character matrix*

Permanent Memory
(ROM) 40K bytes*

Color/Graphics
Text mode:
16 colors*
256 characters and symbols in ROM*
Graphics mode:
4-color resolution: 320h x 200v*
Black & white resolution: 640h x 200v*
Simultaneous graphics & text capability*

Communications
RS-232-C interface
SDLC, Asynchronous, Bisynchronous protocols
Up to 9600 bits per second

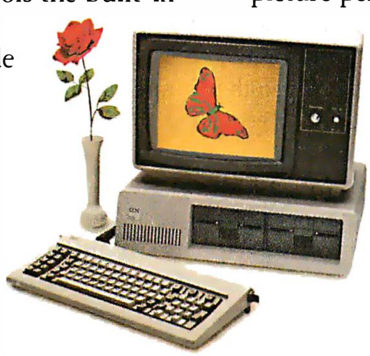
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Remember that these function keys make your program more "friendly" to the user and, therefore, more appealing to us.

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Circle 193 on inquiry card.

PHYSICAL CHARACTERISTICS	Intel iAPX 286	Motorola MC68451	Zilog Z8010	Zilog Z8015/PMMU
	MEMORY-MANAGEMENT UNITS			
No. of pins	68	64	48	48
Integrated processor?	Yes (8086)	No	No	No
Dimensions (mm)	24 by 24	22 by 81	15 by 51	15 by 51
IC process	HMOS	HMOS	NMOS	NMOS
Power (W)	3	1	1.5	1.5
Compatible processors				
Model	Integral	MC68010	Z8001/3	Z8003/4
Clock rates (MHz)	8, 10	4, 6, 8, 10	4, 6, 10	4, 6, 10
Cost per unit (10 MHz)	$237	$111	$383	$137
Logical addresses				
Virtual size	1 gigabyte	16 megabytes	8 megabytes	8 megabytes
Address width (bits)	32	24	23	23
Memory structure				
Segment or page?	Segment	Segment	Segment	Page
Size field (bits)	16 limit	16 mask	8 limit	NA
Size range	1 byte – 64K bytes	256 bytes – 16 megabytes	256 bytes – 64K bytes	2K bytes
Resolution	1 byte	Power of 2	256 blocks	Adjustable
Page boundary	1 byte	256 bytes	256 bytes	2K bytes
Map organization (mapping scheme)	Segment map table	Associative lookup	Mapped by address	Associative lookup
Maximum no. of pages or segments per MMU	16,384	32	64	64
Map cell width (bits)	64	72	32	32
Physical-address base field width (bits)	24	16	16	13
Attribute field (bits)	8	8	8	7
No. of high-speed registers	4	32	64	64
MMU address-generation unit	24-bit adder	16-bit logical	16-bit adder	13-bit concatenation
Global control-register set	1 byte (7 bits)	4 bytes	3 bytes	3 bytes
Global status-register set	0 (status pushed on stack for faults)	18 bytes	6 bytes	9 bytes

Table 4: *A comparison of the physical characteristics of the four surveyed memory-management units. All four have the same physical-memory limit: 16 megabytes.*

and the Z8010 has 64 map registers. If you use the mapping-by-address technique, you will need two MMUs to map AS. The user/supervisor flag can be used as an extra addressing bit to increase memory size to the full 16 megabytes. With this type of organization, four MMU chips are necessary (i.e., 128 segments in two separate address spaces).

You can assign four protection attributes: read-only, data/code, system reserved, and I/O enable. If you do sophisticated I/O processing, you'll appreciate the I/O flag. Another feature, the direction and warning (DIRW) attribute, indicates the orientation for a stack segment. When set, offsets can be negative. DIRW also provides a warning if you are accessing the last 256 bytes of the segment. The warning allows the system to dynamically extend segments during execution, making allocation procedures easier to implement.

Programming the MMU is accomplished through 22 special I/O instructions. By placing the MMU into command mode, you can manipulate map cells and global status registers in a manner similar to programming DMA or peripheral controllers. Z8000 instructions permit you to send a block of commands and data to speed up the process.

Provisions for virtual memory are marginal at best. Only three attribute flags aid paging policies: present, accessed, and changed. Up to eight separate users are possible, but this requires additional MMUs and external hardware. The Z8010's limited number of segments has two major drawbacks. First, it discourages small segment size. The segment-size resolution may not reflect program modularity (studies indicate that median module size is about 50 words). More important, the number of pages it can handle may be insufficient for working-set purposes. Although you can share data, utility is minimal. Many of the benefits of a segmented design are not fully realized.

The Clock page-replacement policy would probably work well with the Z8010. Without an LREF field and strong multiuser support, WS-Clock is likely to be inefficient. Poor sharing and task switching make a VS(n) design impractical. Time required for MMU programming and the page-fault recovery procedure is partially offset by translation speed. I can't see the Z8010 finding much use outside of systems with few users or nonvirtual environments.

The Zilog Z8015

The Z8015 is most notable for its paged-memory strategy. Although markedly different in mapping and logical block structure, most of its features borrow heavily from the Z8010 design. Protection, programming, and multiprocessing components are virtually identical. This MMU's main selling point is the simplified allocation and storage mechanism inherent in a paged system. Also, several mistakes found in the Z8010 are corrected in the Z8015.

The Z8015 employs an associative lookup mapping scheme. Each Z8015 MMU chip can map 64 pages, each 2K bytes in length. Thus, each unit directly maps 128K bytes. Up to 64 units can be grouped together, giving you a total of 4096 page frames (8 megabytes)—ample room for system expansion.

If you don't like 2K-byte pages, simple wiring alterations allow different size options. Page attributes are the same as a Z8010's except that I/O enable is omitted—too bad, it's a handy feature. Translation time is about 15 percent slower.

As with the Z8010, you should stick to the Clock replacement algorithm and a VS(1) design. The MMU supplies all the information necessary

to recover from a page fault; extra hardware is not required. The increased number of page frames is noteworthy: you can achieve a higher degree of multitasking, and it is easier to expand storage. But with the Z8015's fixed-page policy, you sacrifice some degree of flexibility. Adequate support for virtual memory and system security yield the components of a virtual microcomputer. On top of all this, you can use the Z8015 to implement dynamic mapping for the Z8004, the 16-bit-address version of the Z8000 processor.

The Motorola MC68451

Motorola has come up with an excellent memory-control product. The MC68451 furnishes the horsepower to construct a serious virtual computer system. In combination with the MC68000, which I think is the best 16-bit microprocessor around, the MC68451 is quite impressive. Before getting too worked up, however, I should mention that I do have a few reservations about the device. Despite this, the MMU uses some intriguing methods to build the functions that constitute a virtual-memory scheme.

Like the Z8015, the MC68451 relies on associative mapping. Address translation takes place in two stages consisting of an address range and user-space comparison. A clever technique accomplishes both lookup and segment bounds-checking in one fell swoop. Normally, logical page numbers and each map cell's page number are compared bit-wise for a match. Instead, the MC68451 employs a mask field that selects which address bits to check against a map cell's page number. The mask effectively turns some of these bits into "don't cares." The end result is that several logical-address page values can map to a single cell entry.

Motorola's excellent MC68451 furnishes the horsepower to construct a serious virtual computer system.

Each map cell contains a user-space number and associated mask. A valid memory reference must match the active processor user number. The masking function allows a range of user numbers (or just one) to use the same segment; sharing among users becomes almost a trivial task.

One worrisome point is the map-table size. You get merely 32 map cells per MMU, and physical limitations restrict you to a total of eight MMU devices (or 256 cells). You need more than that. Also, the MMU design is complex; it has too many internal registers and multiple MMU coordination is complicated. You have your work cut out for you programming this hardware.

Status registers contain used and changed bits to aid virtual paging routines. But there's no provision for an LREF attribute. Curiously, some bits cause an interrupt to be generated whenever reference is made to the segment. The purpose of this feature eludes me—maybe it's for debugging.

Protection and data typing are practically nonexistent. You can only write-inhibit segments. Any distinction between code and data or user and supervisor happens at the processor level—this makes security less effective.

The MC68451's multiuser facilities and fast context switching make WS-Clock a possible paging strategy. But you must build an extra data structure to hold reference times to support this approach. Though the MC68451 is short on facilities to fully protect data resources, you are compensated by more features for virtual memory. Also, its architecture delivers functions conducive to VS(n) designs.

The Intel iAPX 286

The Intel iAPX 286 constitutes a complete virtual-memory processor that I believe supplies the best features available in the microcomputer world today. What I consider most amazing is the fact that the memory-control unit is practically identical to a Burroughs B5500 mainframe system—a highly touted segmented architecture. Benefits are numerous and problems sparse. To summarize, I'll list the principal advantages:

- it has an integrated processor/MMU design using the 8086 microprocessor, one of the most popular 16-bit processors, making it compatible with existing software
- it has a gigantic (1-gigabyte) address space
- memory segments can be sized with a resolution of 1 byte, making it ideal for program modules
- it features advanced data-protection measures: four priority levels and several data attributes
- it can completely support WS-Clock and VS(n) designs

The iAPX 286's local data table (LDT) register points to a map table residing in MM. There's also a global equivalent of this (GDT) for shared segments. You can define up to 16,384 active segments per user. The number of users is almost boundless. Four fast internal processor registers hold the most recently accessed segment descriptors (called a cache). If you reference a map cell held in one of these registers, there's no translation-time penalty.

Because the iAPX 286, like the 8086, uses segment registers, your program must load these registers prior to memory access. Only branching instructions allow you to specify a full 32-bit virtual address. Segment-register management has two negative aspects: segment-control code clutters a program and net translation time grows. Compilers normally solve the first problem. The time problem is more of a nuisance.

The iAPX 286 features excellent virtual-memory support. Map cells have 16 undefined bits that you can use for several purposes. For instance, 12 to 14 bits would be sufficient for an LREF field. You could also allocate a fix bit to lock special pages into MM (e.g., a supervisor kernel program or an LDT table). Used and segment present bits are supplied, but a changed bit is noticeably absent.

The Intel product represents a superb tool for building virtual memory. Drawbacks are minor: small cache size, the need for segment-register management, and no changed bit. And the device is easy to program. Instead of an I/O program to operate a separate MMU, you do simple loads and stores of memory. The iAPX 286's integrated approach, its numerous features, and its regular design comprise an impressive computing engine.

Evaluation

Which MMU should you choose? The answer depends on various factors. Above all else, the companion microprocessor sways this decision. Get a system with a processor you like—it influences your software and operating-system selections. Performance requirements and intended applications are important. Is the multitasking level a factor? Do you want the flexibility of segmentation or the simplicity of paging? What software policies or peripheral components fit your needs? Table 5 compares the MMU products. The evaluation offers a yardstick for

Fox & Geller asks dBASE II™ users: Which would you prefer?

Annual Report, 1982
Unit Sales and Dollar Volume

PRODUCT A, Quarterly Unit Sales, $39.95/unit net:

	1981	1982	
1st	821	1037	
2nd	510	600	
3rd	385	530	
4th	1020	1298	
	2736	3465	TOTAL UNITS
	$109,303.20	$138,426.75	TOTAL SALES

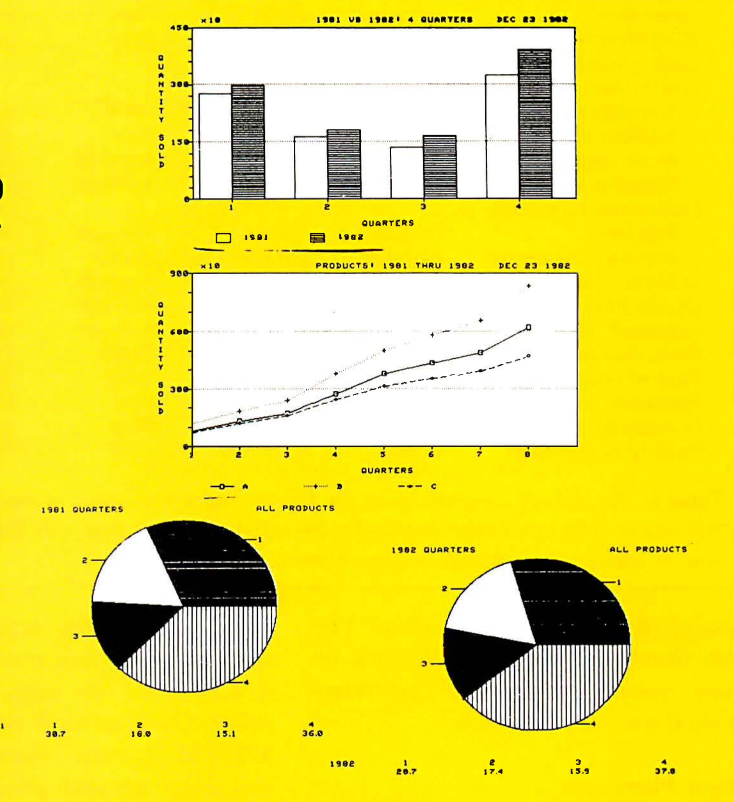
PRODUCT B, Quarterly Unit Sales, $24.95/unit net:

	1981	1982	
1st	1196	1240	
2nd	624	803	
3rd	590	752	
4th	1365	1810	
	3775	4605	TOTAL UNITS
	$ 94,186.25	$114,894.75	TOTAL SALES

PRODUCT C, Quarterly Unit Sales, $49.95/unit net:

	1981	1982	
1st	745	697	
2nd	485	401	
3rd	380	365	
4th	851	812	
	2461	2275	TOTAL UNITS
	$122,803.90	$113,636.25	

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MEMORY-MANAGEMENT UNITS				
OVERALL RATINGS	Intel iAPX 286	Motorola MC68451	Zilog Z8010	Zilog Z8015/PMMU
Virtual-memory features	Excellent	Good	Poor	Average
Support for the Clock page-replacement algorithm	Excellent	Excellent	Good	Excellent
Support for the WS-Clock algorithm	Excellent	Good	Poor	Poor
VS(n) architecture	Excellent	Good	Poor	NA
Device features and performance				
Translation speed	Excellent	Poor	Good	Average
Address space	Excellent	Good	Poor	Average
Block resolution	Excellent	Good	Average	NA
Mapping strategy	Good	Excellent	Average	Excellent
Companion processor				
Popularity	Excellent	Good	Average	Average
Architectural design	Average	Excellent	Good	Good
Multiuser capability	Excellent	Excellent	Average	Average
Design flexibility	Good	Good	Average	Poor
Expansion potential	NA	Good	Average	Good
Protection features	Excellent	Average	Good	Good
Ease of programming	Excellent	Average	Good	Good
Hardware requirements	Excellent	Good	Poor	Good
Complexity (board level)	Excellent	Good	Poor	Average
Page-fault overhead	Good	Excellent	Poor	Poor

Table 5: *An overall comparison of the four memory-management units surveyed in this article. This evaluation highlights the differences between each MMU and gives you an idea of the application possibilities.*

analyzing potential applications. You can draw your own conclusions on how well each device addresses virtual-memory concepts.

New Horizons

Virtual memory opens up a whole new world for microcomputer systems. The expanded address space accommodates traditional large-scale software applications: database-management systems, sophisticated operating systems, and complex high-level-language translators. Moreover, some unique applications of virtual memory exist for microcomputer systems.

Virtual storage streamlines database operations. For example, you don't have to use complex file-access techniques to locate data. A 1-gigabyte address space defines an enormous amount of information. Applications can be much bigger and retrieval time much faster.

A VS(n) design has very exciting implications for microcomputers. You may have observed the trend among microcomputer vendors to offer a choice of several of the leading operating systems with their hardware. With a VS(n) organization, several different operating systems could run in the separate logical-address spaces concurrently. Think of it, CP/M for one user, Xenix for another, Oasis-16 over there. The IBM 370/VM (virtual machine) applies this approach with good success.

Virtual microcomputers give you many other unique software avenues. Consider the memory needs of a 1K- by 1K-byte color graphics system. With various shades and colors, you will quickly consume 1 megabyte of memory. And how about the trend toward integrated business environments? Word processing, report generation, spreadsheet analysis, electronic filing, etc., collectively take a sizable amount of storage.

When will virtual microcomputers be available? They are right now. Altos Computer Systems, Integrated Business Computers (IBC), and Plexus all feature virtual systems designed around the Motorola MC68000 processor. IBM has been looking at the iAPX 286 with some interest, and its future microcomputer systems should prove interesting. The trend is just beginning.

Conclusion

Virtual memory will play a vital role in the evolution of microprocessor-based computer systems. The memory-management units I've reviewed here lay the foundation by supplying the essential hardware components.

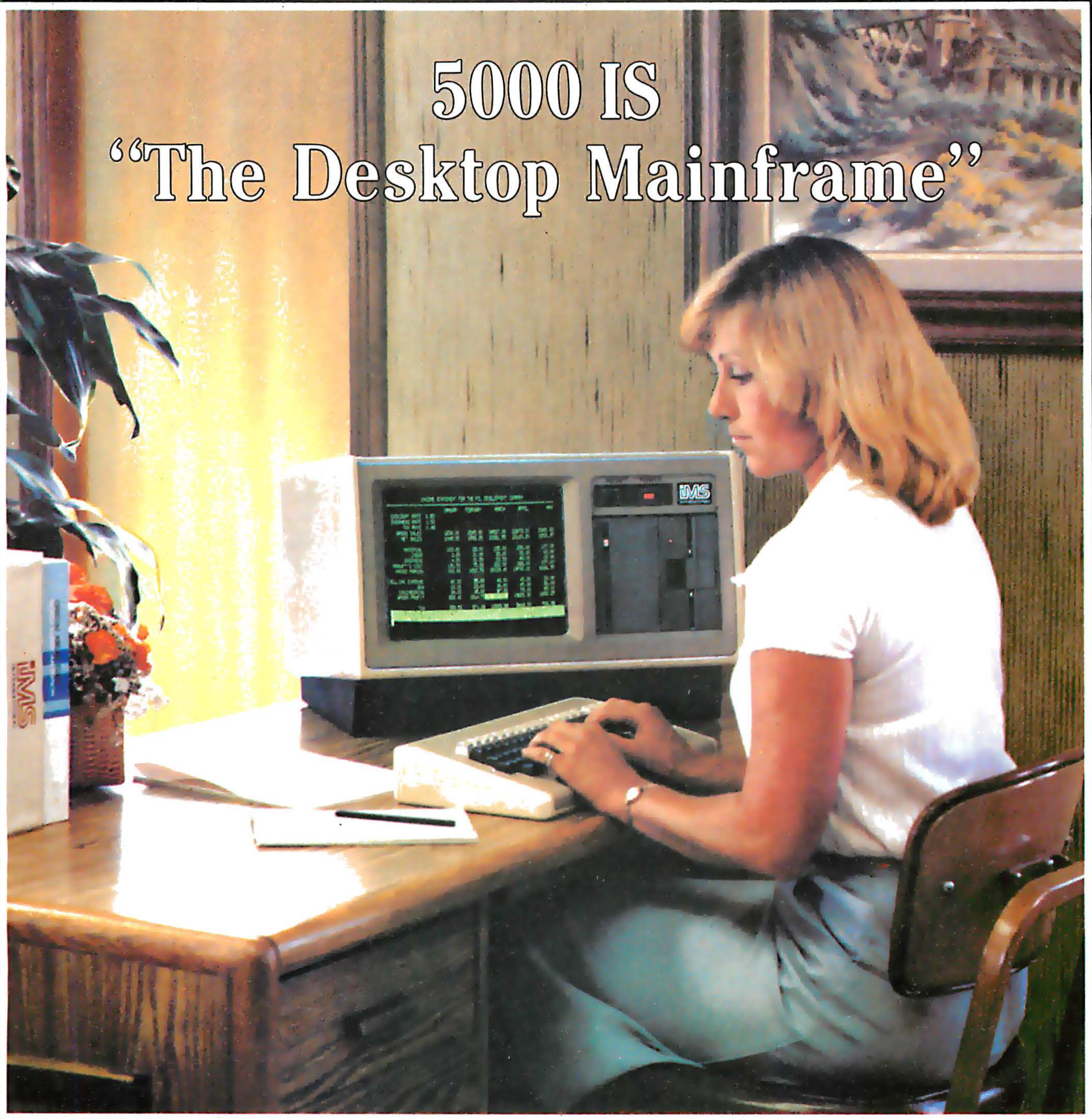
Some people claim that virtual memory fails to provide good performance. I disagree. A carefully designed unit, properly tuned (e.g., with the proper Θ parameter for the WS-Clock algorithm), should actually improve a system's operation. MMUs, sophisticated microprocessors, and simple management policies collectively supply the elements that make virtual systems viable and inevitable. A wider range of advanced applications becomes feasible.

Which MMU is the best is not totally clear. Obviously, the iAPX 286 offers some outstanding features. However, your intended applications and software considerations should figure prominently when you make your determination.

A big memory space presents a new software frontier. With these new MMU devices, it will soon be possible to have the processing power of a mainframe in the size of a desktop. ■

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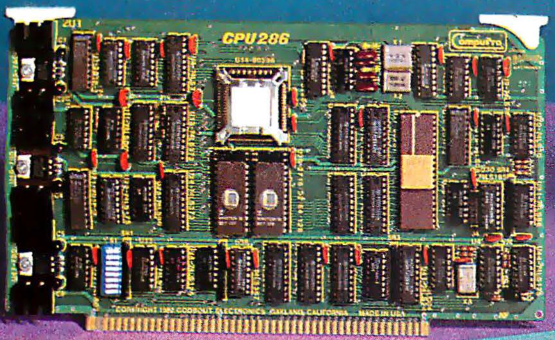
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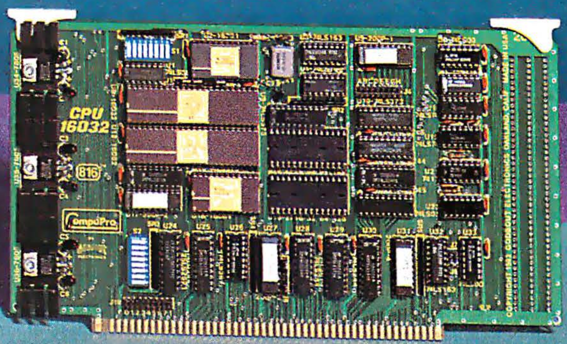
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Power? This one crunches catalogs for breakfast. **CPU 16032** is based on National Semiconductor's NS16032 16-bit microprocessor, with provisions for on-board memory management unit, floating point arithmetic unit, and up to 32K bytes of ROM. Although its internal architecture is 32-bit all the way, **CPU 16032** accepts 8-and/or 16-bit memories and peripherals meeting IEEE 696/S-100 standards.



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Hard Choices for Software Houses

Phil Lemmons
West Coast Editor

The memory-addressing range of the 16-bit microprocessors presents a grand vista to programmers, but an empty one, like the Grand Canyon. The addressing range of these processors extends from 1 to 16 megabytes and up—far enough to hold an applications programmer's grandest dreams: to increase speed of execution, to integrate functions previously done by separate applications programs, to make software easier to use, to design whole new software architectures that revolutionize the way people use computers.

But the actual memory in most of today's 16-bit microcomputers is usually 64K bytes, or sometimes 128K bytes. The present contrast between addressing range and actual memory places software houses in a dilemma. Not to use more than 64K bytes of memory is to waste the greatest asset that the 16-bit microprocessors offer. But if software houses do decide to use more than 64K byes, how much memory should they require? Answering this question is not a simple matter of surveying the installed base of 16-bit systems to determine the average amount of memory owned. Software houses can use additional memory to make software more attractive. If the software is attractive enough, people will order the amount of memory necessary to run it at acceptable speed. In other words, software can not only exploit memory but also sell it.

Nevertheless, there is a limit to the amount of memory that most microcomputer users can afford to buy. Software houses must somehow divine that limit to determine how much memory they will have to work with. Whether the amount of memory is 128K bytes, 192K, 256K, or even 512K, software houses will still have to set priorities for its use. How much memory should they devote to increasing speed, how much to integrating functions, and how much to increasing ease of use? Has the time yet come for software that revolutionizes the "user interface" at affordable prices?

Increasing the speed of execution is the easiest and most obvious way to use additional memory, and it is also an important way. In systems with 64K bytes of memory—the most that an 8-bit processor can address—complex programs had to be divided into modules kept on disk. As the user called for specific functions, the program would go to the disk and bring the necessary module of code into RAM (random-access read/write memory), overwriting another module. Users of the program had to wait for these modules, called "overlays," to be read in. In most cases, 128K bytes of RAM is enough to hold an entire applications program at one time and to eliminate the delays caused by overlays. In addition to eliminating overlays, memory in excess of 64K bytes will also provide room for more of the user's data. Text-editing programs will therefore be able to edit more text more quickly, databases to sort more data more quickly, and so on.

Depending on their priorities, software designers may continue to use overlays, choosing to integrate functions rather than increase speed. Using virtual memory is another strategy for integrating more functions than system memory can hold at one time. In this case, the operating system rather than the applications program swaps modules of software from disk to semiconductor memory and back again. While techniques exist to minimize the delays caused by the use of virtual memory (see "Virtual Memory for an Object-Oriented



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Language" by Ted Kaehler, August 1981 BYTE, page 378), some delays are inevitable.

Integrating functions can make programs so big as to cause delays in managing memory, yet integration can also eliminate delays of another kind. By integrating a number of functions that formerly had to exist in separate programs, software can spare users the inconvenience of exiting one program and loading another and of transferring data from one program to another.

Integrating functions can also make software easier to use. The more the combined functions have the same user interface, the more the user will find the integrated program easier to work with than a set of equally powerful programs that call for different function keys, control codes, and overall methods to perform similar functions.

In an 8-bit program running in 64K bytes of memory, the use of menus, mnemonics, and online textual help is the highest degree of friendliness available. But 16-bit processors can address enough memory to transform the user interface into something never seen in the 8-bit world. Graphics-based guidance and selection by pointing let the user perform a function without learning special terminology. Moving a pointer or cursor onto the symbol of a function is easier than remembering and typing the name of the function or the number or letter that represents the function.

Be-All and End-All

To illustrate the sort of hard decisions software houses face, let's consider a hypothetical integrated software package called Be-All and End-All. The entire package will fit in system memory at one time, leaving at least 64K bytes free for data. Overlays and virtual memory are unnecessary, and there are no delays for disk accesses except as needed for the user's data.

Be-All and End-All includes a word processor (which incorporates a mailing-list program, a spelling checker, a thesaurus, and other writers' aids to spot clichés and other flaws of style); a financial spreadsheet, which has all the functions included in Visicalc, Multiplan, or Supercalc; a graphics program that can take figures marked in the spreadsheet or the databases and generate bar graphs, pie charts, and line graphs; a fully relational database manager that has all the functions of dBASE II; a communications package that permits asynchronous file transfers and conversations with other computers; and a datebook that keeps track of appointments, deadlines, and expenses and generates reminders automatically and reports on demand.

The user interface of Be-All and End-All is organized on the same principles throughout. It permits the user to see, point, and do. All the programs it incorporates can run simultaneously, and the user can view the different processes through adjustable windows on each. "Cut-and-paste" procedures make data transfer between programs as easy and quick as moving a block of text in a simple word processor. Be-All and End-All may integrate more functions than any one person is ever likely to need, but no matter; it will someday be available for only $500.

Suppose you are the programmer and you receive one added specification for Be-All and End-All: it must run at an acceptable speed in 128K bytes of memory. "Impossible!" you say. "Well, get as much of it in as possible," your boss says. "Take all the time you need, as long as it isn't more than six months." What do you include? What do you leave out? What if you could argue for having 192K bytes of memory—would things be any better? What about 256K? Half a megabyte? What if you are told that Be-All and End-All's speed must be sensational rather than acceptable? How many more possible improvements must you then leave out?

Bright people at software houses across the land have been facing similar questions and coming up with different answers. Not surprisingly,

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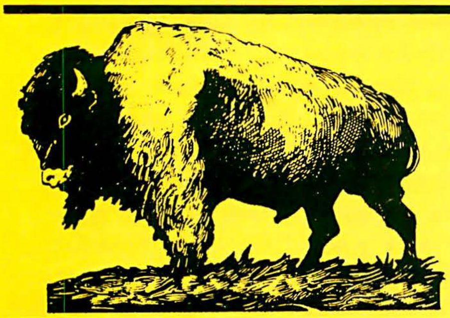
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few of these software houses have targeted their software for the same amount of memory, and even those who agree about the amount of memory available disagree on how to use it.

To date, the software houses that have placed the greatest emphasis on enhancing the user interface have been understandably slower in bringing their products to market. They seem to be centering their new user interfaces on the object/verb "desktop manager" approach developed at Xerox PARC (Palo Alto Research Center). The screen becomes a metaphor for a desktop, and users select first what they want to work on (the object) and then the action that is to be performed on the object (the verb). (For a fuller description of a desktop manager, see "The Smalltalk Environment" by Larry Tesler, August 1981 BYTE, page 90, and "The Lisa Computer System" by Gregg Williams, February 1982 BYTE, page 33). To select both object and verb, you usually point at them with a mouse or a similar device.

Software houses are responding to the issues of integration and ease of use in several different ways. Three general approaches prevail: the all-in-one approach, which combines all major applications in a single program; the separate-but-compatible approach, which provides fully functional independent programs with some mechanism for data interchange among them; and the desktop-manager approach described above, which gives the user access to all applications, entirely hiding from him the problem of data interchange.

The products described in the pages that follow are among the most important ones under development now.

All-in-One

Context Management's MBA: If the question is "Which integrated program currently incorporates the most functions?" the answer can only be MBA. Written in Pascal for easy portability to different processors, MBA is a full-featured spreadsheet, a business graphics program that lets you choose one of nine different kinds of graphs for a set of data, a database that permits sorting data on as many as eight keys, a word processor that takes advantage of function keys to implement its 13 commands, and a communications program that takes data from big computers and automatically loads it into an MBA spreadsheet. The database is relational and lets you add, delete, and rearrange fields at any time. Moreover, you can query the database by typing an example of the sort of thing you want to search for. It can also support databases as large as 16 megabytes, if disk capacity permits.

Although the early version of MBA ran rather slowly on the IBM Personal Computer, it was faster than loading and unloading several different programs to get a job done. The more recent version of MBA shown at last November's Comdex in Las Vegas ran much faster on the IBM PC and faster still on the new Hewlett-Packard Series 200 Model 16, a 68000-based system.

Aside from integrating the user interface for its constituent programs, MBA is not especially innovative. Most commands are invoked by typing a mnemonic preceded by the "/" that Visicalc uses. The program provides online help. MBA organizes data as "folders" containing up to 28 files each—somewhat like the desktop-manager file concept. MBA uses virtual memory to permit documents to refer to data in other documents. When it's in the spreadsheet "context," MBA will divide the display into as many as four windows, any of which may be text, data, a model, or graphics. MBA automatically redraws graphics after changes in data.

Jim Peterson, director of development at Context Management, says that integrating functions was the highest priority in creating MBA partly because integration itself is the main issue in achieving both ease of use and speed. "You have to look at overall speed including telecommunications and the time required to complete an overall task such as producing a report," he notes. Peterson adds that Context has made MBA run faster by reducing the number of

overlays and keeping some memory free for user workspace.

Peterson distinguishes MBA from Lotus Development's 1-2-3 (see below) by saying that "having graphics and numbers and text all on the screen at the same time is important. 1-2-3 doesn't do that. MBA uses more function keys and works in a window while other things are on the screen. The time required to go into and out of a word processor is another drawback for 1-2-3." As for Visicorp's forthcoming Visi On, Peterson expects that its use of a desktop manager will significantly slow execution speeds. He also observes that, while mice are useful when you are just looking at data, you still have to use the keyboard when you're entering data. Mice are expensive, too, he adds.

Lotus Development's 1-2-3: Gregg Williams has already fully described this program (see December 1982 BYTE, page 182), so I will cover it only briefly here. Lotus Development's 1-2-3 runs in 128K bytes and runs fast because it is written entirely in assembly language. The program incorporates three general functions: spreadsheet, graphics, and database management, but the database is quite limited. Lotus plans to add a word processor later. For the most part, the user interface of 1-2-3 is a good implementation of the command-line-plus-online-help strategy familiar from the 8-bit world, but highlighting and selection by cursor do simplify some aspects of the program. The program has some delays while it goes to disk for help text, which also takes up a lot of disk space. As a result, you can't run 1-2-3 on single-sided drives in the IBM PC. For the present, 1-2-3 is best classified as an enhanced spreadsheet.

Separate but Compatible

Micropro's Star Series: Micropro International Corp. introduced Infostar, a relational database manager, at Comdex. Infostar is now available only for 8-bit systems. Seymour Rubinstein, Micropro's president, is proud of the company's achievement in producing a series of compatible programs that let users program applications without knowing a programming language. Users must understand what they want to do but need to know nothing about the grammar, syntax, or command structures that overwhelm many computer users.

The user interface of all the Micropro application programs seems to be based on the enormously successful Wordstar word processor. All versions of Wordstar to date use the same control-code-based user interface Wordstar first introduced some years ago. The most common control codes are shown in on-screen help menus that can be suppressed once the user learns the codes. Like other programs that require the user to enter control codes to execute commands, Wordstar is difficult to learn. Once learned, however, it is powerful. Micropro's strategy for integrating software seems to be to make data movable between applications but to keep each application program independent. This seems to result in a powerful set of programs. Curiously, the 16-bit version of Wordstar uses as many overlays as the 8-bit version regardless of how much memory is present in the 16-bit machine.

The current 16-bit version of Wordstar runs in 64K bytes, but Seymour Rubinstein believes that 256K bytes of RAM will become standard because "the standard memory size [of a system] has always been determined by the size of the standard memory chip." Most recently, the standard chip has been 64K bits (8 chips make 64K bytes of memory). Next year the standard chip will be 256K bits. "Memory has two big applications," Rubinstein says. "Graphics and networking."

Rubinstein also anticipates continual improvements in the user interface. To the extent that these improvements use graphics, they will demand memory. Rubinstein adds, "There will be breakthroughs in input beyond the keyboard." Whether Micropro is preparing such a breakthrough remains mysterious, but Rubinstein does point out that Micropro owns a Xerox Star, the first commercial computer system with a mouse-driven desktop manager. Furthermore, rumors abound that Micropro will make major announcements at the National Computer Conference in May. When the 16-bit version of Infostar becomes available, however, using the Micropro programs under Concurrent CP/M-86

might result in the highest degree of integration of the Micropro product line.

Sorcim's Superware: Sorcim's Supercalc is an excellent electronic spreadsheet that provides good textual online help on demand. Sorcim has recently expanded its product line (called Superware) by introducing Superwriter, a word processor; Superdata-File Manager, a database management system; Superchart, a business graphics program; and Superdata Interchange, a program that permits data interchange among the Sorcim programs. Superdata Interchange converts Superware files into either a common BASIC file format or a Superware format. Supercalc can manipulate data stored by Superdata, Superwriter can include Supercalc data in a text file, and Superchart can generate graphics from Supercalc data.

Each of the Superware programs uses conditional overlays. If memory is scarce, overlays are read in from disk when needed; if memory is abundant, overlays reside in memory rather than on disk. This approach takes advantage of the additional memory that 16-bit machines may have but does not require it.

Each Sorcim application program is powerful. Superwriter, for example, incorporates an excellent spelling checker and a mailing-list feature for producing form letters. Superdata File Manager can sort on 16 fields at once and can manage files of up to 32,000 records each and 1023 bytes per record. In addition, Superdata permits the linking of files to form larger files and the creation of new file formats from old ones. All the Superware programs have user interfaces much like Supercalc's. The Superware series will run under Concurrent CP/M-86, which means that you can have multiple Superware programs running simultaneously and switch at will among them.

Richard Frank of Sorcim sees three main problems in achieving the next step toward greater ease of use and integration: creating an underlying data structure, providing sufficiently powerful applications programs, and writing good drivers for I/O (input/output). He says that Sorcim is now at work in all three of these areas, and he argues that neither CP/M-86 nor Unix will support the solution of all three problems.

Because Visi On works atop MS-DOS and CP/M-86, Frank believes that the new Visicorp software cannot properly address the problem of the underlying data structure; it deals only with the I/O process. Sorcim will be developing its future software for machines running MS-DOS but will create its own data structure. It will be interesting to see how much of Sorcim's "data structure" resembles traditional operating systems.

If the I/O drivers are done well, Frank says, they will handle keyboards, mice, touch panels, and other types of I/O devices. Frank believes that the design of the software should not require a mouse. "The hardware people are trying to make the machines' 'footprints' [the amount of desk space an object occupies] smaller," Frank observes, "while software people are trying to make footprints bigger by requiring space for a mouse to roam." He notes that people have enough trouble just managing the keyboard, and adding a mouse

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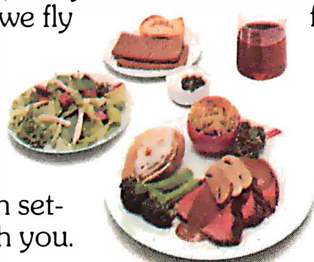
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with its own buttons won't make matters easier.

As for concurrency, Frank argues—as does Microsoft's Bill Gates—that simultaneously running more than one application program on a single microprocessor is neither necessary nor desirable. What he believes users really need is *interruptability*—the ability to switch quickly from one application to the next. Frank also discounts the usefulness of splitting the screen among four applications. There is no need, he says, to run a spreadsheet while running a word processor; the real need is to run one after the other in rapid succession. That is the end toward which Sorcim is working.

Concurrency for Separate-but-Compatible Programs

Digital Research: Digital Research's Concurrent CP/M-86 provides a mechanism that can help integrate separate application programs. Under Concurrent CP/M-86, you can run several independent application programs (or other kinds of software) at one time. Instead of having windows on each application, Concurrent CP/M-86 permits easy switching from one "virtual terminal" to another. Each virtual terminal is the whole-screen display of one of the application programs that is running. You can get information from one program while running another by switching briefly from one virtual terminal to the next. More direct integration of data from one program into another depends on their data structures. By choosing application programs from a single vendor who has created a common data structure and a common user interface for all the programs, you should be able to achieve a high degree of integration under Concurrent CP/M-86.

Digital Research has often expressed a commitment to making computers accessible to more people, and president Gary Kildall suggests visual aids as one means to that end. There is a lot of speculation about Digital Research's plans for making computers easy to use, but the company has not announced any plans that extend beyond creating tools to increase the productivity of programmers working for independent software vendors.

Desktop Managers

Microsoft's Multi-Tools Series: Microsoft chairman Bill Gates says, "You can do a lot in 192K." While he offers few details about the company's forthcoming Multi-Tools series of integrated applications programs, Gates notes that Charles Simonyi, formerly of Xerox PARC, is Microsoft's manager of end-user software. Simonyi and Larry Tesler, who was instrumental in the development of Apple's Lisa applications software, spent some time together at Xerox PARC disputing the number of buttons that a mouse should have. Tesler said one, and Lisa has a one-button mouse. Look for Microsoft to use a two-button mouse.

The Multi-Tools series will be available in two versions: one will run on all machines, and one will run on advanced hardware. The Multiplan that runs now on the IBM Personal Computer probably shows what the run-on-anything series will be like. Even without a mouse, the program lets users select functions by cursor movement. For those who prefer words to formulas, Multiplan's ability to let users refer to cells by English labels rather than alphanumeric coordinates (i.e., "Sales*Unit-price" instead of "C15*C16") is an important convenience.

The advanced-hardware version of the Multi-Tools series requires a non-keyboard input device (such as a mouse), high-resolution graphics, and a 16-bit processor. This version will provide a desktop manager and windows on more than one application at a time. Each application will have a separate window and its own verbs (as opposed to all applications sharing the same window and verbs).

Gates remarks that software shown to date has "ignored the metaphor of how you see data. In a spreadsheet, remembering formulas in cells is a problem. Popping graphs out of windows is also unsatisfactory. You need

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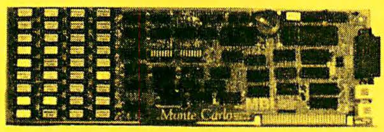
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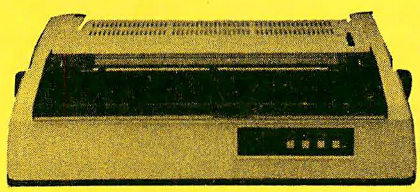
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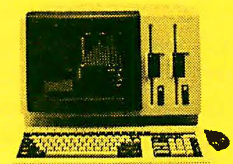


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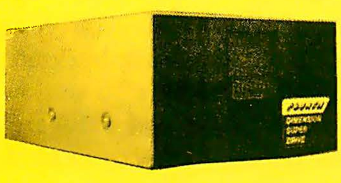
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a more substantial metaphor." His comments suggest that Microsoft conceives of the window on each application not just as a means of gaining access to data but also as a way to provide user aids uniquely suited to the particular application. The idea is to integrate the user interface as much as possible for different applications without sacrificing coherence or intuitive appeal.

Gates also argues that true concurrency is not really desirable. Instead of needing to run more than one application program on the same microprocessor at the same time, Gates says, users need to be able to switch rapidly from one application to the next. "You need interruptability," Gates says, "but not simultaneity." The argument is that timesharing a single microprocessor is less efficient than having the microprocessor run only one application program at a time and switch from one to the next quickly as the user requests. [In many cases, users would have trouble perceiving any difference between interruptability and simultaneity (concurrency).] Nevertheless, Microsoft's MS-DOS will support true concurrency in a future release.

Visi On from Visicorp: When Dave Clough, project manager at Visicorp, was asked how much memory a system would need to resolve the conflict between ease of use and added functionality, he said, "That conflict will never go away." Clough also said that when forced to choose between ease of use and additional functions, Visicorp would choose ease of use.

The prototype of Visi On shown at Comdex was a desktop manager that appeared to integrate substantial functionality and great ease of use. While the Visi On desktop manager lacks the Lisa's pictorial detail, it still allows the user to choose from items shown on the desktop by using a mouse to point at one item. The mouse used with Visi On has two buttons.

Visi On's windows let the user view different applications in progress simultaneously. Nine verbs will be common to all applications under Visi On, and other verbs are specific to each application.

The word processor shown with Visi On, presumably a relative of Visi Word, resembles Multiplan in that it enables the user to select a function by pointing at an item in a list. Visicorp has a whole new series of applications, not yet shown or described, that will run under Visi On.

Visi On will permit users to install applications modules as needed. If you need a database and a word processor but not a spreadsheet, you can buy only what you want. If your needs change, you can install an additional module yourself.

Visi On, described as an "operating environment," occupies an interesting territory between conventional operating systems and application programs. It runs on top of either CP/M-86 or MS-DOS and provides concurrency independently of the underlying operating system. Because Visicorp will make technical details about Visi On available to applications programmers, software written outside Visicorp should be available to run in the Visi On environment. Visi On will be portable to different machines, and different application programs can be written to be portable under Visi On.

Apple Computer's Lisa: It's easy to see that a company like Apple Computer Inc., which produces both its new Lisa computer and the Large-scale Integrated Software Architecture to run on it, has an advantage over software houses in producing new-generation software. (For full descriptions of Apple's Lisa and its software, see the February 1982 BYTE.) Apple can change the software and the hardware to suit each other. Knowing that Lisa will have a megabyte of memory has enabled Apple to succeed in a remarkably ambitious project. For combined integration of function and ease of use, Lisa is the leader by far. Lisa's drawback is its high price—not high in relation to function or value, but in absolute terms. While a toolkit will permit programmers to write application programs that run on the Lisa, the Lisa's software cannot be transferred to MS-DOS and CP/M-86 systems. Apple has plans to implement fuller database functions on the Lisa but ad-

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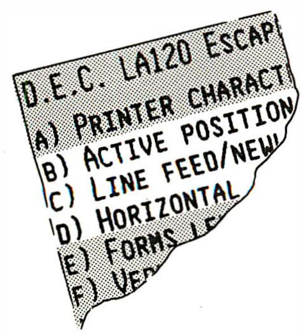


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mits that the present database manager is somewhat limited. For ease of use, however, Lisa's database manager is unrivaled.

Summing Up

Most of today's software falls far short of our hypothetical Be-All and End-All package. Such a large and friendly software package is likely to remain hypothetical for some time. But inexpensive memory and 16-bit processors may make many of today's hypotheses real surprisingly soon. For those who have spent years struggling to coordinate unrelated application programs in the past, any of the approaches to integrating software represents real progress and welcome relief.

As for deciding what software to buy now, the choice is difficult. The revolutionary graphics-based software has great appeal as long as it doesn't sacrifice one of the specific functions that you happen to need, decrease the operating speed of the program beyond your tolerance, or increase the price of a system beyond your means. When specific products meet your needs, you will buy one of the new software packages whether it has been announced today or not.

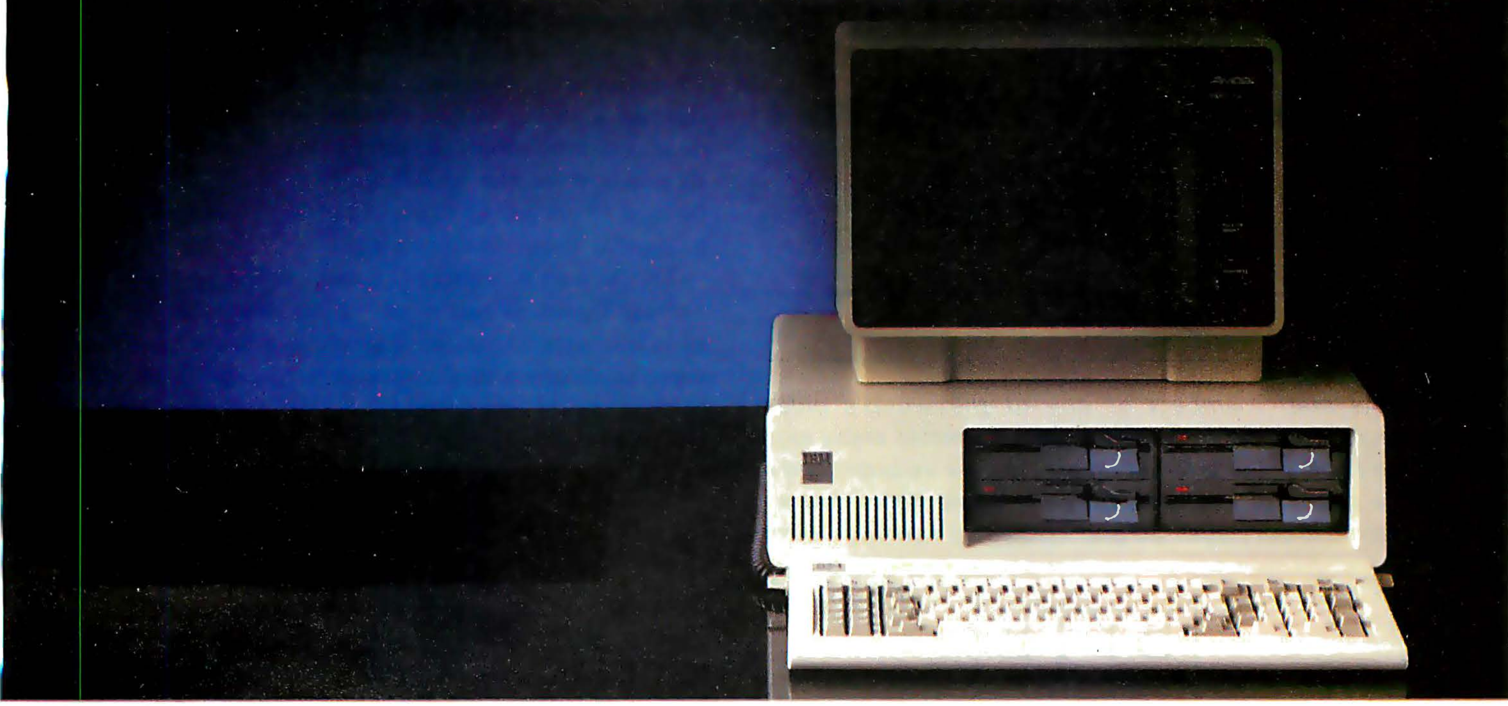
If none of the revolutionary products meets your specific requirements in function, speed, and cost, you must choose between the separate-but-compatible approach to application software (as in Sorcim's Superware) and the all-in-one approach (as in Context Management's MBA). In making this choice, the most important factor will probably be whether the all-in-one program offers all the features and all the power that you happen to need. If you do buy separate application programs, the best course is probably to buy from one software house and hope for increased integration in subsequent releases. If an all-in-one program has almost but not quite everything you need, you might ask its publisher whether future versions will include what you need.

Advances in hardware technology may hasten the triumph of the revolutionary software by reducing the price of very fast mass storage and thus reducing the penalty paid for using overlays and virtual memory. But no revolution is perfect or final or above criticism. A small skeptical voice inside me keeps raising three questions:

- Should all software be written so that it's easy for a novice to learn, or so that it is most useful and productive in the long term?
- Will the metaphor of the desktop remain a good one? It seems appropriate for the transition from paper work to computer work, but once we grow accustomed to working with computers, why should we want our computers to emulate desks?
- Can the mouse compete with the efficiency of programmed function keys in all fundamental operations like deleting characters? To delete characters with the Delete key, you just put the cursor on the characters to be deleted and press the key. Auto repeat makes swift deletion of more words and sentences easy: you just hold the Delete key and watch the cursor swallow the characters to its right. To delete characters with the mouse-driven systems that I have seen, you put the mouse's pointer on the character you want, press a button on the mouse to select the character, and press a button on the mouse to choose the verb Delete. That seems to add a step. Selecting larger blocks of text may require you to press more buttons (or the same button more times) on the mouse.

To date, ingenious software designers have debated these and the other issues of integrated and friendly software. All their conclusions remain as hypothetical as Be-All and End-All. Only the marketplace can say which hypotheses are true. The decision of the marketplace is uncertain because the people who will constitute most of the market have never touched a computer. Technology will determine how these people will first touch computers, but from then on they as new users will decide everything on nontechnical grounds. ■

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50 and 100 Years Ago in BYTE

Edited by Rich Malloy

As staff members of one of the world's oldest microcomputer magazines, we sometimes enjoy looking back at the interesting articles we've published in the past. For example, here are some items that appeared in our pages 50 and 100 years ago this month.

BYTE

APRIL, 1933: The International Business Machines Company of Elmira, New York, announced last month that, although it will continue to manufacture typewriters and adding machines, most of its resources will be devoted to the development and sale of fire alarm systems.

"We figure that the most important device in a business office is the fire alarm," said Thomas Watson, the president of the company. "After all, if there's a fire, who cares whether you have a typewriter or not. In fact, in future years, when you think of International Business Machines, the first thing that'll come to your mind will be fire alarms."

In a related item, film star Charlie Chaplin turned down a request by International Business Machines to appear in its promotional literature. "It's a great company," said the mustachioed comic, "but frankly the idea of having me promote business machines is one of the most ridiculous things I've ever heard."

* * *

Things continue to heat up in the adding-machine market. Following the introduction last year of the mini-adding machine, rumors have reached us that the Japanese are ready to market a "micro-adding machine." This new invention, said to employ VLSS (very large-scale smallness) technology, has an incredibly light weight of only 47 pounds. To combat the threat of this new small machine, American adding-machine manufacturers are said to be at work incorporating deluxe features into their new models. One rumor has it that work is almost complete on a machine that can multiply.

* * *

The Acme Calculating Company of Piscataway, New Jersey, has just announced a machine which it calls a "Disk Storage Device." The machine consists of a disk-drive mechanism called a "turntable" and a series of interchangeable data disks, or "records." The disk is read by placing it on a rotating platform located on top of the disk drive. A pin, called a stylus, is inserted into one of dozens of grooves etched on the disk. Under proper conditions, a voice-like sound can be heard. This voice can be used to encode all types of data and can even be used to portray music-like sounds.

The Acme Calculating Company will market the Disk Storage Device as part of an "Office System," which will include a typewriter, an adding machine, a typist, and someone to crank up the turntable. Also included will be software by Al Jolson and Rudy Vallee and His Connecticut Yankees.

BYTE

APRIL, 1883: Professor Eaton Zweiback of Slippery Rock University recently announced the discovery of a new number system called the "Binary System." This system uses only two numerals, 0 and 1, as opposed to the decimal system which uses ten. Professor Zweiback claims that the binary system will have absolutely no practical value and will be used mostly as a mathematical novelty.

* * *

Harvard anthropologists have discovered the remains of an ancient Arabian city just 75 miles north of where ancient Babylon once stood. Little is known about the inhabitants of this city except for the fact that for some unknown reason they wrote the numeral zero with a slash through it. The anthropologists are completely puzzled as to why these people used such a strange symbol.

* * *

Agricultural experts have abandoned efforts to develop farm land in the valley south of San Francisco, California. The experts claim that is difficult to grow crops in the soil because there is too much silicon. There is so much silicon present that some residents of the valley have started gathering it together and melting it into "chips," which they then plan to dump somewhere near Boston, Massachusetts.

* * *

Missionaries near Peking have discovered a very small abacus, which the Chinese call "Mei Kro." This extremely small device, about the size of a postage stamp, is said to be extremely fast for computations. One of its drawbacks, however, is that the operator must use a pair of tweezers to manipulate the beads.

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The Enhanced VIC-20
Part 3: Interfacing an MX-80 Printer

Joel Swank
12550 SW Colony #3
Beaverton, OR 97005

To do any serious programming with the Commodore VIC-20, you need a printer. Commodore markets two that plug directly into the VIC serial port: the VIC-1515 and the VIC-1525 graphics printers. Both form characters with a 6 by 7 dot matrix and operate at 30 characters per second.

For most uses these printers are satisfactory. But if you look closely at a VIC character on the screen, you can see that it is composed of an 8 by 8 matrix of dots. Neither Commodore printer can print true VIC characters or graphics. And because the VIC has only a serial printer port that uses a DIN (Deutsche Industrie Norm) connector, you can't interface printers that have standard Centronics-style parallel ports with the VIC.

This article will show you how to select an alternative printer for use with the VIC and how to interface it with the computer to get true VIC characters and graphics.

Selecting a Printer

The first consideration is which printer to buy. A large number of low-cost dot-matrix printers offering a wide range of features and capabilities are now available. Two features in particular are necessary to adapt the printer to the VIC. First, the printer must have graphics capability so that the VIC character patterns can be formed in memory and then sent to the printer. Second, the printer must have 8 or more wires in its print head if it is to print the VIC's 8 by 8 characters efficiently.

Many printers use a 7-wire print head and normally print a character that is only 7 dots high. These printers can print only 7 dots vertically on each pass of the print head across the paper. Because the VIC character is 8 dots high, the print head would have to make two complete passes to print the entire VIC character, slowing the effective printing speed by one-half. Making two passes can also distort the VIC character because horizontal alignment is not always perfect on some printers.

The Epson MX-80 is one of the more popular printers. It has a 9-wire print head, and with the Graftrax option, it can do graphics. The MX-80 also offers italics, several print sizes, and proportionally spaced characters. To give you an idea of some of its features, I have included a summary of its escape sequences and control codes in table 1. These are the commands that the computer uses to tell the printer the desired print format. The MX-80 meets the requirements for use with the VIC and is moderately priced.

Interfacing the Printer

The next consideration is how to connect the printer to the VIC. The most obvious way is through the user I/O (input/output) port, which is the opening at the left rear of the VIC case. The logic assignments of each pin on this port are given in table 2 (see figure 1 on page 288 for user port I/O connections). Some of the pins are already assigned to other uses, but a full 8-bit parallel I/O port that is capable of driving a printer does exist. This is actually the B port of a 6522 VIA (versatile interface

Editor's Note: *The VIC-20 is one of the new breed of low-cost computers that offer a surprising amount of computing power for the money. But its low cost also means that it lacks some of the features we've come to take for granted. In this series of articles, author Joel Swank will "enhance" the VIC-20 and in so doing increase the utility of this very interesting computer. . . S. J. W.*

Epson MX-80 Escape Sequences

ESC 0	Sets line spacing to 8 lines per inch (LPI)
ESC 1	Sets line spacing to 7/72 inch per line
ESC 2	Sets line spacing to 6 LPI
ESC 3 n	Sets line spacing to n/216 inch per line
ESC 4	Selects italics character set
ESC 5	Selects standard character set
ESC 8	Enables paper transfer even if out of paper
ESC 9	Cancels paper out function
ESC :	Sets Radio Shack mode
ESC ;	Cancels Radio Shack mode
ESC <	Moves print head to left end of carriage
ESC =	Clears the M.S.B. function
ESC >	Sets the M.S.B. in the printer
ESC ? n1 – n37	Redefines all escape codes
ESC @	Resets the printer
ESC A n	Sets line spacing to n/72 inch per line
ESC B n1 n2...null : 255	Sets vertical tabs
ESC C n	Sets form length to n lines
ESC D n1 n2...null : 255	Sets horizontal tabs
ESC E	Selects emphasized printing mode
ESC F	Cancels emphasized printing mode
ESC G	Selects double strike printing mode
ESC H	Cancels double strike printing mode
ESC J n1 n2	Bit image graphics—960 DPL mode, 480 speed
ESC K n1 n2	Bit image graphics—480 DPL mode
ESC L n1 n2	Bit image graphics—960 DPL mode
ESC P	Selects compressed-character print mode
ESC Q	Cancels compressed-character print mode
ESC S	Selects expanded-character print mode
ESC T	Cancels expanded-character print mode

Epson MX-80 Control Codes

CTRL G	Bell character
CTRL H	Backspace character
CTRL I	Horizontal tab character
CTRL J	Linefeed character
CTRL K	Vertical tab character
CTRL L	Formfeed character
CTRL M	Carriage-return character
CTRL N	Selects expanded-character print mode
CTRL O	Selects compressed-character print mode
CTRL Q	Selects the printer
CTRL R	Cancels compressed-character print mode
CTRL S	Deselects the printer
CTRL T	Cancels expanded-character print mode

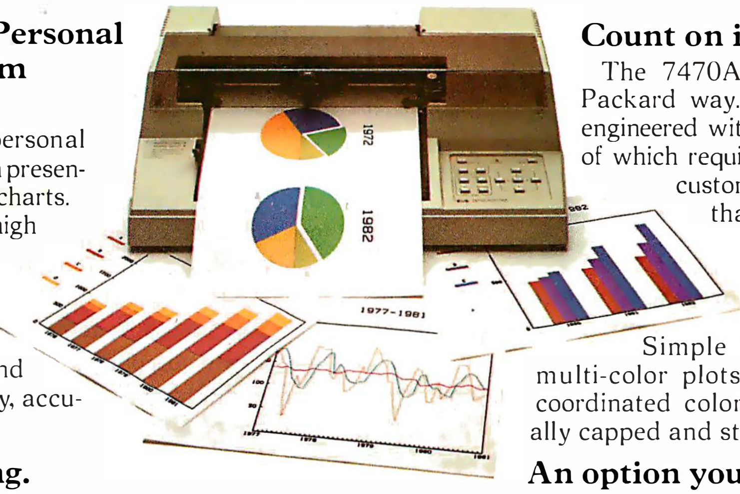
Table 1: *The Epson MX-80 printer escape sequences and control codes. By having the VIC-20 send these escape and control codes to the MX-80, you can control the output from the printer.*

Pin #	Type	Note	Pin#	Type
1	GND		A	GND
2	+5V	100mA max.	B	CB1
3	$\overline{\text{RESET}}$		C	PB0
4	JOY0		D	PB1
5	JOY1		E	PB2
6	JOY2		F	PB3
7	LIGHT PEN		H	PB4
8	CASSETTE SWITCH		J	PB5
9	SERIAL ATN IN		K	PB6
10	+9V	100mA max.	L	PB7
11	GND		M	CB2
12	GND		N	GND

Table 2: *VIC-20 user port I/O pin designations. Printer output is taken from pins A through M by means of the VICEPS program.*

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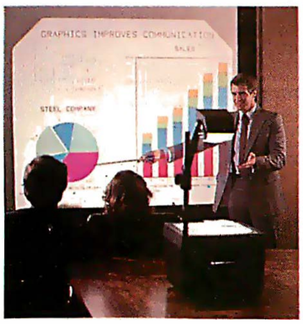
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VIC to Epson Connections

VIC Via Pin #	VIC User Port	Signal	Epson 36-Pin Connector
	A	GND	19
CB1	B	Acknowledge	10
PB0	C	D0	2
PB1	D	D1	3
PB2	E	D2	4
PB3	F	D3	5
PB4	H	D4	6
PB5	J	D5	7
PB6	K	D6	8
PB7	L	D7	9
CB2	M	Data Strobe	1

Table 3: *VIC-20 to Epson MX-80 connections. This illustrates the output pins from the VIC versatile interface adapter (VIA) chip, the connections from the VIC user port, the signals involved, and the corresponding pins on the MX-80.*

adapter) chip, a very powerful I/O device that is used on many computers that have the 6502 microprocessor. The VIC programmer's reference manual gives a complete description of it starting on page 229.

Most printers, including the MX-80, come equipped with an "industry-standard parallel interface." This interface is not actually a standard, but all versions are similar, and all of those I've seen can be driven with a 6522 VIA. Table 3 shows the physical connections you need to connect the MX-80 to the VIC via the user port. Eleven wires must go from the VIC to the printer; one to ground it, 8 for the 8 bits of data, and 2 for handshaking. Handshaking lines are used to keep the printer and the VIC synchronized. The VIC uses the DATA STROBE line to tell the printer when a character is ready. The printer uses the ACKNOWLEDGE line to tell the VIC when it has accepted the character. The 6522 VIA, when used in the handshake output mode, takes care of these signals.

The least expensive way to connect the VIC and the MX-80 is with a ribbon cable. To do so, keep the length of the wire as short as possible. I have used an 8-foot cable with no problems. The VIC end of the cable must be a 24-pin card-edge connector that has contacts on 0.156-inch centers. The MX-80 end must be a 36-pin Centronics-style male printer connector. I have a standard printer cable with a male connector on each end. To use this cable, I wired a short ribbon cable from the VIC connector to a female 36-pin connector. My VIC can now be connected to the standard printer cable. These connectors are available at many electronics stores and from mail-order companies.

The interface as shown in table 3 does not take full advantage of all of the features of the MX-80. Seven other signals on its connector are not used. These provide, among other things, an out-of-paper signal and a busy

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Circle 291 on inquiry card.

VICEPS Commands and Open Options

SYS(7168)	OPEN printer for graphic output of VIC characters. Select the following options before calling:
POKE 780,1	Select 8 lines per inch (LPI).
POKE 780,2	Select graphic LPI (no space between lines).
POKE 780, (anything else)	Select 6 LPI.
POKE 781,1	Select double horizontal density. Uses 960 graphics mode. Slows printer 1/16 ASCII mode. Good for work to be photocopied.
POKE 781, (anything else)	Select single density. Uses 480 mode graphics. Slows printer 1/4 over ASCII mode.
SYS(7188)	OPEN printer for ASCII output. All printer escape sequences and control codes are under user control. Some standard VIC characters are also Epson control codes.
SYS(7202)	CLOSE the printer and restore the output vector. If in graphics mode the end of the last line must be sent to the printer.

Table 4: *VICEPS program commands. The SYS commands open and close the VIC user port for output to the printer. The POKE commands select various printer options.*

signal. You don't need to use these signals to get the MX-80 to work. Because the VIC has no more user I/O pins available, the extra signals are ignored.

Software Interface

Listing 1 is the VICEPS program, which allows the VIC to communicate with the MX-80. Written in 6502 assembly language, it occupies about 400 bytes of memory. It is accessed with a BASIC SYS command. To use the program, you must first enter the command SYS (7168) to start the OPEN routine (see line 36). This routine initializes the VIA and the printer and inserts the address of the printer output routine into the VIC's display vector as well. The display vector is the pointer to the VIC's program to display a character on the screen. All screen output comes through this vector. It was provided by the designers of the VIC for just such an application as this. After the initialization routine has been started, all characters that are displayed on the screen will also be sent to the printer.

Before entering the SYS command you can also give some information to the OPEN routine. This information is passed via the SYS register area at memory locations 780 and 781. Table 4 lists a summary of the VICEPS program options. Location 780 is used to select the vertical print density—how much space is left between lines of print. Entering 1 into location 780 produces a vertical density of 8 lines per inch (LPI). This leaves one blank row of dots between lines. Entering a 2 into location 780 results in graphic density. This leaves no space between lines so that graphic characters will connect, as they do on the VIC screen. Entering any other number into location 780 produces the default print density of 6 LPI, which makes for the most readable program listings and text.

Text continued on page 280

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Listing 1: *The VICEPS program is a software interface between the VIC-20 and the MX-80. It controls output to the printer.*

```
LOC   CODE       LINE

0000             ;     VICEPS ; VIC-20 INTERFACE TO THE EPSON MX-80 PRINTER
0000             ;             VIA THE VIC PARALLEL USER PORT
0000             ;             THE EPSON MUST HAVE GRAFTRAX

0000             ;     ZERO PAGE LOACTIONS

0000             RVSMOD =$C7            ;REVERSE MODE FLAG
0000             QUOTMO =$D4            ;QUOTE MODE FLAG
0000             VICPAT =$FB            ;TEMPORARY ZERO PAGE POINTER

0000             ;     VIC PIA LOCATIONS
0000             IORB1  =$9110          ;I/O REG B
0000             DDRB1  =$9112          ;DATA DIRECTION REG B
0000             PCR1   =$911C          ;PERIPHERAL CONTROL REG
0000             IFR1   =$911D          ;INTERUPT FLAG REG
0000             IER1   =$911E          ;INTERRUPT ENABLE REG

0000             ;     TV CONTROLLER LOCATIONS

0000             TVCTL5 =$9005          ;CHARACTER SET/SCREEN BUFFER PORT

0000             ;     VIC SUBROUTINES

0000             VICOUT =$F27A          ;ROUTINE TO SEND CHAR TO SCREEN

0000             ;     VIC RAM

0000             SYSA   =$30C           ;A REG STORAGE FOR SYS COMMAND
0000             SYSX   =$30D           ;X REX STORAGE FOR SYS COMMAND
0000             DISVEC =$326           ;VECTOR TO SCREEN DISPLAY ROUTINE

0000             ;     EQUATES

0000             CR     =$0D            ;RETURN CHAR
0000             INSDEL =$14            ;INSERT-DELETE CHARACTER
0000             ESC    =$1B            ;ESCAPE CHARACTER
0000             LF     =$A             ;LINE FEED CHARACTER
0000             LINLIM =60             ;MAX CHARACTERS PER LINE
0000             LPIGRF =8              ;PRINTER GRAFIC DENSITY CODE
0000             LPI8   =9              ;8 LINES PER INCH CODE
0000             LPI6   =12             ;6 LINES PER INCH CODE

0000                    *=$1C00

1C00             ;**
1C00             ;***   OPENG : ENTRY POINT TO TURN ON ROUTINE TO
1C00             ;**            ECHO CHARACTERS TO THE PRINTER IN
1C00             ;              IN FULL VIC GRAPHICS

1C00  20 26 1D   OPENG  JSR INITOT      ;INIT THE PIA FOR OUTPUT
1C03  A9 30             LDA #<GRFOUT    ;MOVE OUTPUT ROUTINE ADDRESS
1C05  8D 26 03          STA DISVEC
1C08  A9 1C             LDA #>GRFOUT
1C0A  8D 27 03          STA DISVEC+1
1C0D  20 6A 1D          JSR INITPR      ;INITIALIZE THE PRINTER
1C10  20 40 1D          JSR INILIN      ;INITIALIZE FOR FIRST LINE
1C13  60                RTS

1C14             ;**
1C14             ;***   OPENA : ENTRY TO TURN ON ROUTINE TO ECHO
1C14             ;**            CHARACTERS TO PRINTER IN ASCII

1C14  20 26 1D   OPENA  JSR INITOT      ;INIT PIA FOR OUTPUT
1C17  A9 16             LDA #<ASCOUT    ;MOVE ADDRESS OF ASCII DISPLAY
1C19  8D 26 03          STA DISVEC      ;ROUTINE TO DISPLAY VECTOR
```

Listing 1 continued on page 270

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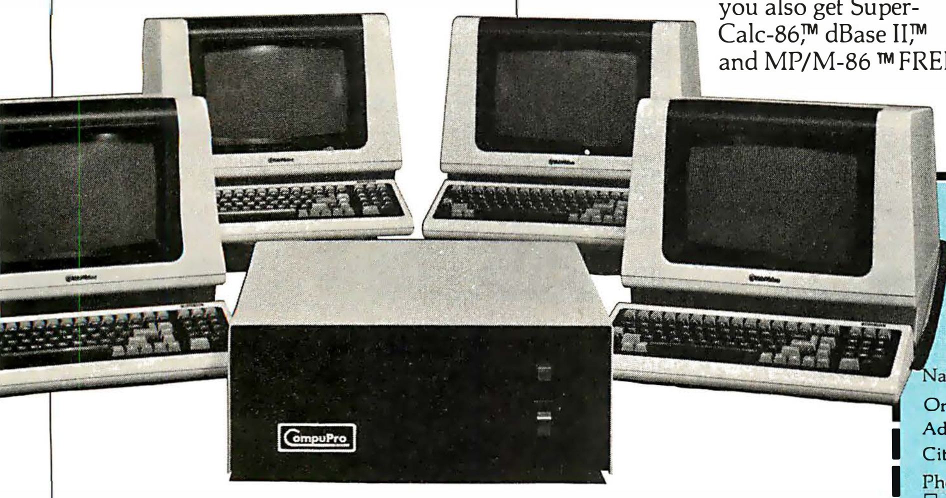
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Circle 180 on inquiry card.

```
1C1C  A9 1D                LDA #>ASCOUT
1C1E  8D 27 03             STA DISVEC+1
1C21  60                   RTS

1C22             ;**
1C22             ;***      CLOSE : ENTRY TO TURN OFF EITHER ECHO ROUTINE
1C22             ;**

1C22  A9 7A      CLOSE     LDA #<VICOUT      ;RESTORE VECTOR TO SCREEN
1C24  8D 26 03             STA DISVEC        ;DISPLAY ROUTINE
1C27  A9 F2                LDA #>VICOUT
1C29  8D 27 03             STA DISVEC+1
1C2C  20 A9 1C             JSR FILLIN        ;FINISH CURRENT LINE
1C2F  60                   RTS

1C30             ;***      GRFOUT : ROUTINE TO GENERATE VIC GRAPHICS
1C30             ;                  ON THE PRINTER

1C30  8D 9D 1D   GRFOUT    STA ASAVE         ;SAVE CHARACTER
1C33  48                   PHA
1C34  8A                   TXA               ;SAVE ALL REGS
1C35  48                   PHA               ;ON STACK
1C36  98                   TYA
1C37  48                   PHA
1C38  AD 9D 1D             LDA ASAVE         ;GET CHAR BACK
1C3B  20 7A F2             JSR VICOUT        ;SEND TO VICS SCREEN

1C3E             ; NOW CONVERT THE ASCII CHARACTER INTO A VIC
1C3E             ;POKE CODE. KEY ON CR TO END LINE.
1C3E  AA                   TAX               ;HI BIT ON?
1C3F  10 1C                BPL BITOFF        ;NO
1C41  29 7F                AND #$7F          ;YES, TURN IT OFF
1C43  C9 7F                CMP #$7F          ;CONVERT $7F TO $5E
1C45  D0 02                BNE NOT7F
1C47  A9 5E                LDA #$5E
1C49  C9 20      NOT7F     CMP #$20          ;CONTROL CHAR?
1C4B  B0 0C                BCS NOTCTL        ;NO
1C4D  C9 0D                CMP #CR           ;RETURN?
1C4F  F0 4B                BEQ FINLIN        ;YES
1C51  A2 D4                LDX #QUOTMO       ;IN QUOTE MODE?
1C53  F0 4D                BEQ GRFBAK        ;NO, THEN IGNORE IT
1C55  09 C0                ORA #$C0          ;ON 2 HI BITS
1C57  D0 26                BNE SAVPOK        ;TO MAKE POKE CODE
1C59  09 40      NOTCTL    ORA #$40          ;TURN ON BIT 6
1C5B  D0 1C                BNE CKRVS         ;AND GO CHECK REVERSE

1C5D  C9 0D      BITOFF    CMP #CR           ;RETURN CHAR?
1C5F  F0 3B                BEQ FINLIN        ;YES, END OF LINE
1C61  C9 20                CMP #$20          ;CONTROL CHARACTER?
1C63  B0 0A                BCS NOCTL         ;NOPE
1C65  C9 14                CMP #INSDEL       ;YES, IS IT DELETE?
1C67  F0 39                BEQ GRFBAK        ;YES, IGNORE IT
1C69  A6 D4                LDX QUOTMO        ;NO, IS QUOTE MODE ON?
1C6B  D0 10                BNE HIBIT         ;YES, THEN PRINT IT
1C6D  F0 33                BEQ GRFBAK        ;NO, IGNORE IT
1C6F  C9 60      NOCTL     CMP #$60          ;OVER $60?
1C71  90 04                BCC LOWER         ;NO
1C73  29 DF                AND #$DF          ;YES, OFF BIT 5
1C75  D0 02                BNE CKRVS
1C77  29 3F      LOWER     AND #$3F          ;TURN OFF BITS 6 & 7
1C79  A6 C7      CKRVS     LDX RVSMOD        ; 'EVERSE MODE ON?
1C7B  F0 02                BEQ SAVPOK        ;NO
1C7D  09 80      HIBIT     ORA #$80          ;ON BIT 7 TO REVERSE CHARACTER
1C7F  8D 9D 1D   SAVPOK    STA ASAVE         ;SAVE POKE CODE

1C82             ;  CHECK FOR FULL LINE
1C82  AD 9E 1D             LDA LCOUNT        ;CHECK CHARACTER COUNT
1C85  C9 3C                CMP #LINLIM       ;AT LIMIT?
1C87  D0 08                BNE NOTFUL        ;NO, SKIP
1C89  A9 0A                LDA #LF           ;SEND LINE FEED TO PRINTER
1C8B  20 19 1D             JSR PUTCHR
```

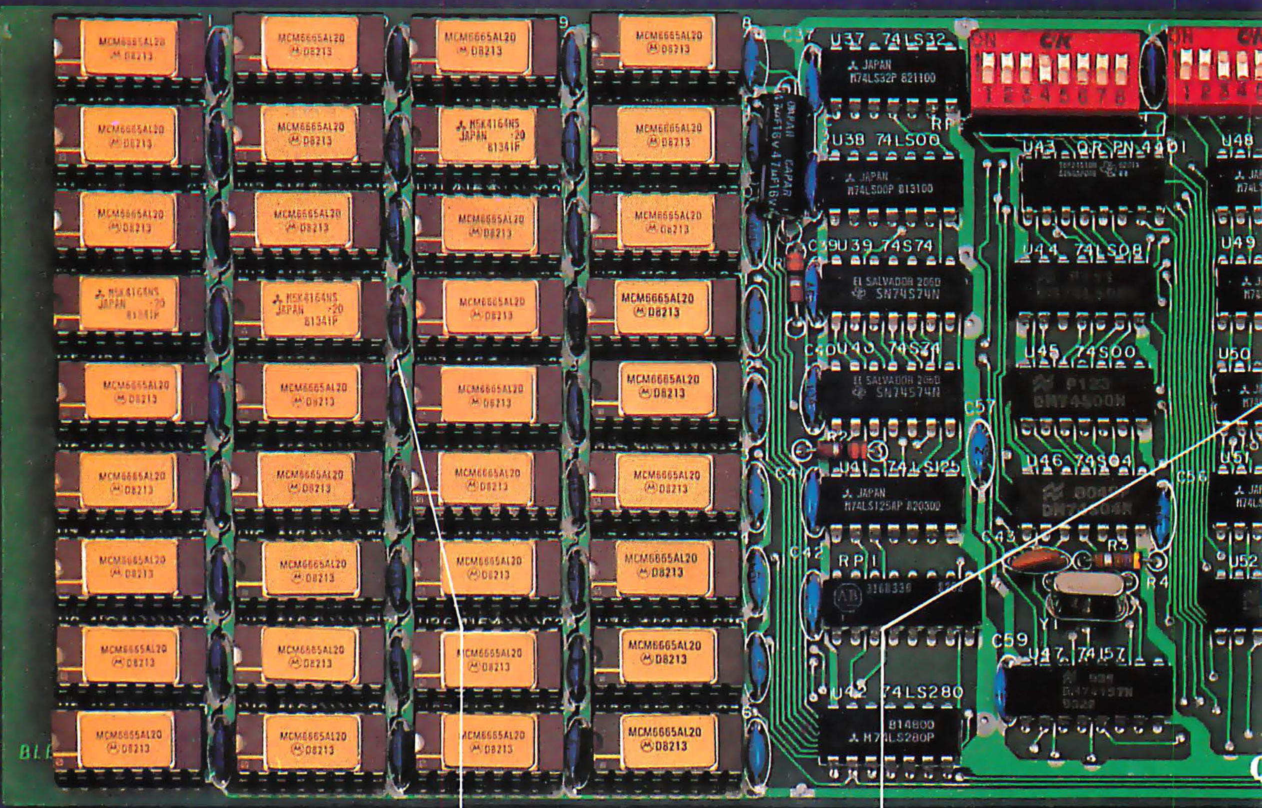
Listing 1 continued on page 274

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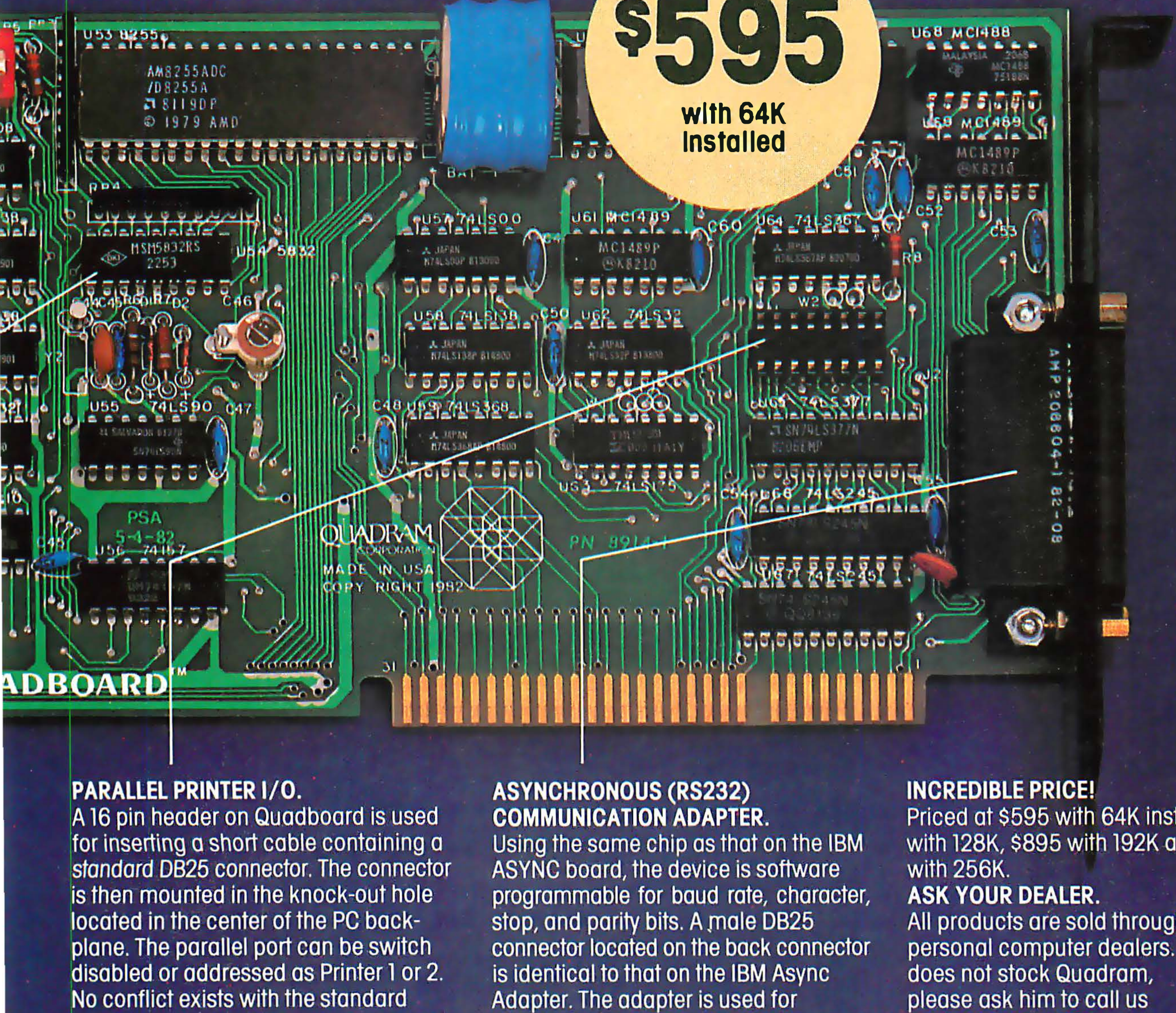
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Quadboard eliminates the hassle of manually inputting the date on system boot-up by providing for the clock and all software routines necessary for inserting the appropriate programs on your diskettes. The internal computer clock is automatically set for compatibility with most software routines which utilize clock functions. On-board battery keeps the clock running when the computer is off.

SEE OUR AD ON PAGE 78

BY QUADRAM

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Circle 357 on inquiry card.

Listing 1 continued:

```
1C8E  20 40 1D          JSR INILIN        ;SETUP FOR NEW LINE
1C91  AD 9D 1D   NOTFUL LDA ASAVE         ;RETRIEVE POKE CODE
1C94  20 BF 1C          JSR SEND          ;SEND CHAR TO PRINTER
1C97  EE 9E 1D          INC LCOUNT        ;COUNT IT
1C9A  D0 06             BNE GRFBAK        ;SKIP TO END

1C9C             ;FINISH LINE
1C9C  20 A9 1C   FINLIN JSR FILLIN        ;FILL LINE WITH BLANKS
1C9F  20 40 1D          JSR INILIN        ;INITIALIZE NEW LINE

1CA2  68         GRFBAK PLA               ;RESTORE ALL REGS
1CA3  A8                TAY
1CA4  68                PLA
1CA5  AA                TAX
1CA6  68                PLA
1CA7  18                CLC
1CA8  60                RTS               ;AND RETURN

1CA9             ;***   FILLIN : FILL REMAINDER OF LINE WITH BLANKS
1CA9  AE 9E 1D   FILLIN LDX LCOUNT        ;GET CHAR COUNT
1CAC  E0 3C             CPX #LINLIM       ;AT LIMIT?
1CAE  B0 0A             BCS NXTLIN        ;YES, QUIT
1CB0  A9 20             LDA #32           ;NO, SEND A BLANK
1CB2  20 BF 1C          JSR SEND
1CB5  EE 9E 1D          INC LCOUNT        ;COUNT IT
1CB8  D0 EF             BNE FILLIN        ;REPEAT
1CBA  A9 0A      NXTLIN LDA #LF           ;SEND LINE FEED TO PRINTER
1CBC  4C 19 1D          JMP PUTCHR

1CBF             ;***   SEND : ROUTINE TO USE VIC POKE CODE TO FIND
1CBF             ;             THE CHARACTER PATTERN, CONVERT IT TO
1CBF             ;             THE PRINTERS FORMAT AND SEND TO PRINTER

1CBF             ;   FIRST CALC THE ADDRESS OF THE CHARACTER
1CBF  85 FB      SEND   STA VICPAT        ;SAVE POKE CODE
1CC1  A9 00             LDA #0            ;IN PATTERN POINTER
1CC3  85 FC             STA VICPAT+1
1CC5  A0 02             LDY #2            ;LOOP TO MULTIPLY THE POKE CODE
1CC7  18         MULT8  CLC               ;BY 8 TO GET OFFSET INTO CURRENT
1CC8  26 FB             ROL VICPAT        ;CHARACTER SET
1CCA  26 FC             ROL VICPAT+1
1CCC  88                DEY
1CCD  10 F8             BPL MULT8         ;THREE TIMES THRU
1CCF  A2 80             LDX #$80
1CD1  AD 05 90          LDA TVCTL5        ;USE DATA FROM TV CHIP TO
1CD4  29 0C             AND #$C           ;DETERMINE LOCATION OF
1CD6  F0 02             BEQ NOALT         ;OF CURRENT CHARACTER SET
1CD8  A2 10             LDX #$10
1CDA  8A         NOALT  TXA               ;ADD IN HI NYBBLE
1CDB  18                CLC               ;OF CHARCACTER SET ADDRESS
1CDC  65 FC             ADC VICPAT+1
1CDE  85 FC             STA VICPAT+1
1CE0  AD 05 90          LDA TVCTL5        ;CALC SECOND NYBBLE VALUE
1CE3  29 03             AND #$3
1CE5  18                CLC
1CE6  0A                ASL A
1CE7  0A                ASL A
1CE8  65 FC             ADC VICPAT+1      ;AND ADD IT IN
1CEA  85 FC             STA VICPAT+1

1CEC             ;   CONVERT VIC PATTERN TO PRINTER PATTERN
1CEC  A0 07             LDY #7
1CEE  B1 FB      BYTLUP LDA (VICPAT),Y    ;GET A VIC PATTERN ROW
1CF0  A2 00             LDX #0
1CF2  0A         BITLUP ASL A             ;SHIFT EACH BIT INTO A
1CF3  7E 95 1D          ROR PRTPAT,X      ;COLUMN OF THE PRINTER PATTERN
1CF6  E8                INX
1CF7  E0 08             CPX #8            ;GOT ALL 8?
1CF9  90 F7             BCC BITLUP        ;NO, DO ANOTHER
1CFB  88                DEY               ;YES BUMP Y TO NEXT ROW OF VIC PATTERN
1CFC  10 F0             BPL BYTLUP        ;DO ALL 8

1CFE             ;   SEND CONVERTED PATTERN TO PRINTER
```

Listing 1 continued on page 276

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Listing 1 continued:

```
1CFE  A2 00              LDX #0
1D00  BD 95 1D   OUTLUP  LDA PRTPAT,X      ;GET A DOT COLUMN
1D03  20 19 1D           JSR PUTCHR        ;SEND TO PRINTER
1D06  AC 9F 1D           LDY DOTFLG        ;DOUBLE DOT MODE?
1D09  C0 01              CPY #1
1D0B  D0 03              BNE NOZDOT        ;NO, SKIP
1D0D  20 19 1D           JSR PUTCHR        ;YES, SEND IT AGAIN
1D10  E8         NOZDOT  INX
1D11  E0 08              CPX #8            ;DONE ALL?
1D13  90 EB              BCC OUTLUP        ;NO, REPEAT
1D15  60                 RTS

1D16             ;***    ASCOUT : ROUTINE TO SEND ASCII CHARACTER TO PRINTER

1D16  20 7A F2   ASCOUT  JSR VICOUT        ;SEND TO SCREEN

1D19             ;   SEND BYTE TO PRINTER
1D19  48         PUTCHR  PHA               ;SAVE CHARACTER
1D1A  A9 10              LDA #$10          ;TEST INTERRUPT BIT
1D1C  2C 1D 91   WAITO   BIT IFR1          ;IN FLAG REG
1D1F  F0 FB              BEQ WAITO         ;WAIT UNTIL IT TURNS ON
1D21  68                 PLA
1D22  8D 10 91           STA IORB1         ;THEN SEND CHARACTER
1D25  60                 RTS

1D26             ;***    INITOT : INITIALIZE PIA FOR OUTPUT

1D26  AD 1C 91   INITOT  LDA PCR1          ;GET PCR
1D29  29 0F              AND #$0F          ;CLEAR B PORT BITS
1D2B  09 A0              ORA #$A0          ;SET IT TO AUTO PULSE MODE
1D2D  8D 1C 91           STA PCR1          ;AND STORE IN PCR
1D30  A9 10              LDA #$10          ;DISABLE INTERRUPT
1D32  8D 1E 91           STA IER1
1D35  A9 FF              LDA #$FF          ;SET ALL BITS TO OUTPUT
1D37  8D 12 91           STA DDRB1
1D3A  A9 00              LDA #0            ;START WITH A NULL
1D3C  8D 10 91           STA IORB1
1D3F  60                 RTS

1D40             ;***    INILIN : PREPARE FOR SENDING A LINE

1D40  A9 00      INILIN  LDA #0            ;CLEAR LCOUNT
1D42  8D 9E 1D           STA LCOUNT
1D45  A9 1B              LDA #ESC          ;START ESCAPE SEQ
1D47  20 19 1D           JSR PUTCHR
1D4A  AD 9F 1D           LDA DOTFLG        ;DOUBLE DOT MODE REQUESTED?
1D4D  C9 01              CMP #1
1D4F  D0 08              BNE ONEDOT        ;NOPE
1D51  A9 4C              LDA #'L'          ;YES, 960 MODE
1D53  A0 C0              LDY #<960         ;LOAD 960 INTO X AND Y
1D55  A2 03              LDX #>960
1D57  D0 06              BNE PUTREG        ;GO SEND
1D59  A9 4B      ONEDOT  LDA #'K'          ;480 MODE
1D5B  A0 E0              LDY #<480         ;480 INTO X & Y
1D5D  A2 01              LDX #>480
1D5F  20 19 1D   PUTREG  JSR PUTCHR        ;SEND CODE
1D62  98                 TYA
1D63  20 19 1D           JSR PUTCHR        ;AND THEN COUNT
1D66  8A                 TXA
1D67  4C 19 1D           JMP PUTCHR

1D6A             ;***    INITPR : STARTUP INITIALIZATION FOR PRINTER

1D6A  A2 00      INITPR  LDX #0
1D6C  BD 92 1D   IPRLUP  LDA PRTAB,X       ;GET A BYTE
1D6F  F0 06              BEQ IPDUN         ;QUIT IF 0
1D71  20 19 1D           JSR PUTCHR        ;SEND IT
1D74  E8                 INX
1D75  D0 F5              BNE IPRLUP
1D77  AE 0C 03   IPDUN   LDX SYSA          ;GET A REG
1D7A  A9 09              LDA #LPI8         ;GET 8 LPI CODE
1D7C  E0 01              CPX #1            ;1=8LPI
1D7E  F0 08              BEQ PUTDEN        ;YES, 8LPI
1D80  A9 08              LDA #LPIGRF       ;LOAD GRAPHIC DENSITY CODE
1D82  E0 02              CPX #2            ;2=GRAPHIC DENSITY
```

Listing 1 continued on page 278

WESTICO — The Software Express Service that really delivers:

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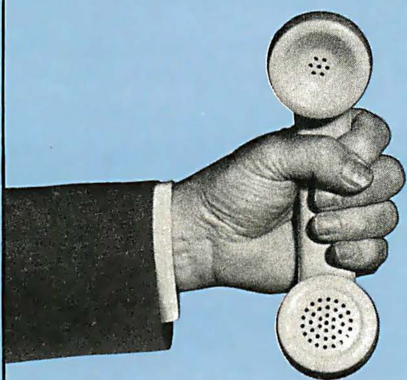
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Listing 1 continued:

```
0246  1D84  F0 02           BEQ PUTDEN       ;YES
0247  1D86  A9 0C           LDA #LPI6        ;ELSE DEFAULT TO 6 LPI
0248  1D88  20 19 1D  PUTDEN JSR PUTCHR
0249  1D8B  AD 0D 03        LDA SYSX         ;SAVE DOT MODE FLAG
0250  1D8E  8D 9F 1D        STA DOTFLG
0251  1D91  60              RTS

0252  1D92            ;   PRINTER PARM TABLES

0253  1D92  1B        PRTAB  .BYT ESC,'A',0
0254  1D93  41
0255  1D94  00

0256  1D95            ;  DATA AREAS

0257  1D95            PRTPAT *=*+8           ;PRINTER PATTERN AREA
0258  1D9D            ASAVE  *=*+1           ;CHARACTER TEMPORARY
0259  1D9E            LCOUNT *=*+1           ;CHARACTER IN LINE COUNTER
0260  1D9F            DOTFLG *=*+1           ;DOT MODE FLAG

0261  1DA0            LAST    .END
0262  1DA0             ERRORS= 0000

SYMBOL CROSS REF FOR VIC TO EPSON MX-80 INTERFACE    PAGE 05

SYMBOL DEFINED REFERENCES

A        0000   0172 0165 0164
ASAVE    0258   0115 0107 0070 0064
ASCOUT   0192   0050 0048
BITLUP   0172   0176
BITOFF   0090   0075
BYTLUP   0170   0178
CKRVS    0104   0102 0089
CLOSE    0056
CR       0023   0090 0082
DDRB1    0010   0209
DISVEC   0021   0059 0057 0051 0049 0040 0038
DOTFLG   0260   0250 0218 0183
ESC      0025   0253 0216
FILLIN   0130   0136 0120 0060
FINLIN   0120   0091 0083
GRFBAK   0122   0118 0098 0095 0085
GRFOUT   0064   0039 0037
HIBIT    0106   0097
IER1     0013   0207
IFR1     0012   0196
INILIN   0214   0121 0114 0042
INITOT   0202   0047 0036
INITPR   0234   0041
INSDEL   0024   0094
IORB1    0009   0211 0199
IPDUN    0240   0236
IPRLUP   0235   0239
LAST     0261
LCOUNT   0259   0215 0135 0130 0117 0109
LF       0026   0137 0112
LINLIM   0027   0131 0110
LOWER    0103   0100
LPI6     0030   0247
LPI8     0029   0241
LPIGRF   0028   0244
MULT8    0147   0151
NOALT    0157   0155
NOCTL    0099   0093
NOT7F    0080   0078
NOTCTL   0088   0081
NOTFUL   0115   0111
NO2DOT   0187   0185
NXTLIN   0137   0132
ONEDOT   0225   0220
OPENA    0047
OPENG    0036
OUTLUP   0181   0189
PCR1     0011   0205 0202
PRTAB    0253   0235
```

Listing 1 continued on page 280

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Listing 1 continued:

```
PRTPAT  0257   0181 0173
PUTCHR  0194   0248 0237 0232 0230 0228 0217 0186 0182 0138 0113
PUTDEN  0248   0246 0243
PUTREG  0228   0224
QUOTMO  0006   0096 0084
RVSMOD  0005   0104
SAVPOK  0107   0105 0087
SEND    0143   0134 0116
SYSA    0019   0240
SYSX    0020   0249
TVCTL5  0015   0161 0153
VICOUT  0017   0192 0071 0058 0056
VICPAT  0007   0170 0167 0166 0160 0159 0149 0148 0145 0143
WAITO   0196   0197
X       0000   0235 0181 0173
Y       0000   0170
```

Text continued from page 266:

Location 781 passes the horizontal density to the OPEN routine. The MX-80 offers two horizontal densities in graphic mode: 480 dots per line (DPL) and 960 DPL. Entering a 1 into location 781 produces the 960 DPL mode, and entering anything else in 781 produces the 480 DPL mode. In both modes 60 VIC characters are printed on a line. In 960 DPL mode, each dot of a VIC character is printed twice, resulting in a very black, dense printout. In 480 DPL mode each dot is printed only once, resulting in lighter print.

Printing in graphics mode slows the speed of the MX-80 considerably. It cannot print bidirectionally in graphics mode, thus halving the normal printer speed. It takes two passes to print a line in 480 DPL mode, slowing printer speed to one-fourth the normal rate. In 960 DPL mode the printing speed is reduced by one-half and it takes four passes to print each line, resulting in one-sixteenth of normal printing speed.

Once the OPEN routine has been executed, any character that is displayed on the screen will also go to the printer. Characters that are entered directly into the screen buffer with a POKE command will not be printed. When you have finished printing, you can turn off the printer by entering the command SYS (7202) to execute the CLOSE routine, which restores the display vector. No

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S-100 World News

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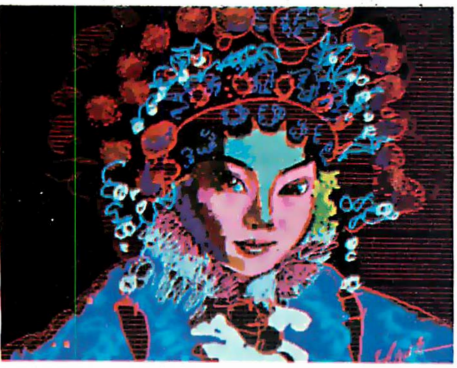
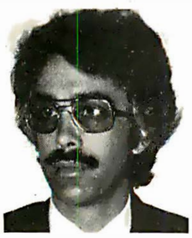


Image achieved by DGS' CAT 1600 Series color video graphic workstation. Picture courtesy of Digital Graphic Systems, Inc. See story below.

GRAPHICS: NOW MAX-IMIZED

CANOGA PARK—March 30, 1983—The decreasing costs and increasing density of memory made possible the present boom in digital graphics. Graphic systems designers are now able to take another major step with the introduction of MAX-M, a one megabyte memory board for $1983. As large size system memory and multi-megabyte Virtual Disk, MAX-M opens up major new low cost implementations.



Wayne Maw, Director of R&D for RGB Dynamics, Salt Lake City, Utah, reports, "My application is dependent on speed. With the Macrotech dynamic board, I have the needed speed." The RGB system is a Z80-based, high resolution color directory system for shopping malls, due for April release.

Empirical Research Group of Kent, Washington, creates a state-of-the-art high resolution color video graphics system by integrating their fast 68000 computer, Macrotech system memory, and the color video image processor from Digital Graphic Systems, Inc., Palo Alto, California. Radcliffe Goddard of Digital Graphics states, "High speed image processing requires large system memory to provide instantaneous display frame paging."

The demand for MAX-M by the graphics industry was nearly instantaneous following the initial Macrotech announcement.

MAX—256K to 1M S-100 Memory

CANOGA PARK—March 30, 1983—Mike Pelkey, Macrotech International president, today released details of the revolutionary MAX line of S-100 memory boards. Pelkey stated: "IEEE-696 now has a new standard for dynamic memory. The MAX product line offers 256K to 1M, at a price that ranges down to less than $0.00023 per bit." Pelkey continued, "The MI product line now includes our ultra fast (70 ns) 128K static memory, with battery backup capability, plus the 150 ns dynamic memories—in every 128K step from 256K through 1M (1024K) bytes, and add-on kits to permit field upgrade of sizes."

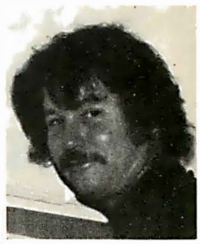
The extreme density of the MAX family is made possible through the use of proprietary PALs (programmable array logic). Also stated as available for add-on to any size MAX is Macrotech's popular M³ memory mapping architecture. M³ permits the 16-bit address space of an 8-bit processor to be dynamically mapped in 4K pages into as much as 16 megabytes of physical memory.

Parity error detection and 8/16 bit data transfer capabilities are provided as standard on the MAX series memory board.

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Dynamic Memory	256K	MAX-256	$1108
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Addressing	512K	MAX-512	1647
	768K	MAX-768	1815
	896K	MAX-896	1899
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	256K/768K	MKT-2/7	876
	256K/896K	MKT-2/8	967
	256K/1M	MKT-2/M	1060
	384K/512K	MKT-3/5	600
	384K/768K	MKT-3/7	784
	384K/896K	MKT-3/8	876
	384K/1M	MKT-3/M	968
	512K/768K	MKT-5/7	284
	512K/896K	MKT-5/8	376
	512K/1M	MKT-5/M	468
	768K/896K	MKT-7/8	192
	768K/1M	MKT-7/M	284
	896K/1M	MKT-8/M	192
M³ option		MKT-M3	121
Software (provided on 8" disk) Virtual Disk for MP/M II* and CP/M 2.2, CP/M 3.0* Bios modules, CP/M memory tests			$ 25
Manuals (sold separately) 128/ST			$ 15
MAX Technical Manual			15

Software for M³ Available



BURBANK—March 30, 1983—"M³ bank switching for 8-bit processors is much more useful with the new creative systems programs," states Dan West of Westcom Systems Inc. MP/M II* disk intensive applications are greatly improved with the new Virtual Disk routines now available through Macrotech OEM's and dealers for their M³ memory boards.

Westcom Systems, as the software consulting firm for Macrotech, has also provided subroutine listings to easily incorporate M³ mapping into the new CP/M 3.0* (CP/M Plus*) Biosmodule. The advantages of CP/M 3.0* with disk buffering, hashed directories, and user program expansion go hand in hand with Macrotech's flexible "bank switched" memory capabilities.

All Macrotech software and manuals are available through Dan West's Compuserve account #70250,102.
Leave comments/questions as E-Mail.

These new techniques can combine the above features with custom needs of the future, such as printer buffering, multi-page display and memory-intensive graphics displays.

The software listings are included in the Macrotech memory board manuals and are optionally available on 8" diskettes.

*CP/M 3.0, CP/M Plus, and MP/M II are registered trademarks of Digital Research Inc.

Circle 242 on inquiry card.

more characters will be printed until the OPEN routine is executed again.

A second OPEN routine, called by the command SYS (7188), is provided to allow the VIC to communicate with the MX-80 directly in ASCII (American National Standard Code for Information Interchange) instead of VIC character patterns. This enables the VIC to take complete control of all of the MX-80's features. If you want complete control, remember to initialize the printer as necessary for your application. Notice that some of the VIC control characters for color change and cursor movement are also command codes to the printer (see table 1). If you aren't careful, you could get some strange results.

Listing 2 is the CHARACTER SET program that prints the entire VIC character set in the various modes. A sample of its output follows the program listing. The entire listing was printed with an MX-80 by the VIC.

The main routine in the VICEPS program is a subroutine called GRFOUT (see line 64). It is executed each time a character is sent to the VIC screen. It must convert the ASCII code into a VIC screen POKE code so that it can find the VIC character pattern in memory. A routine in the VIC KERNAL ROM at location E756 hexadecimal converts ASCII to VIC screen codes. Unfortunately, this routine is part of the display routine and cannot be called externally. GRFOUT is based on the logic in this routine. After converting ASCII to screen code, GRFOUT calls the subroutine SEND to convert the screen code to a graphic image and send it to the printer. SEND finds the character pattern the same way that the VIC TV controller chip finds the pattern; as a result, any character that can be displayed on the screen can be printed. If you've designed your own characters for the VIC, this routine will find them and print them.

After the appropriate character pattern is found, it must be converted into printer format. The VIC stores its character patterns in memory as rows of dots. Each of the 8 bytes of the pattern represents one row of dots of the character. The printer requires that the character be sent a column at a time. Row patterns must be converted into column patterns. Next, each column must be sent to the printer, which requires sending 8 bytes in the 480 DPL mode and sending 16 bytes in the 960 DPL mode.

VICEPS should be fairly easy to convert for use with another printer whose print head has 8 or more wires. Any changes required will be in the subroutines INILIN and INITPR (see lines 214 and 234). These routines send to the printer the commands to set the LPI and initialize the graphics mode. These commands will be different for another printer.

Some printers may represent a column of dots differently from the MX-80. The MX-80 uses the high-order bit of the byte to represent the top dot in the column and the low-order bit to represent the bottom dot. Other printers might do the reverse, which would make all characters come out upside-down. You can correct the situation by reversing the direction of the Y register-loop index in the pattern-conversion routine in the subroutine SEND. It currently starts Y at 7 and decrements through

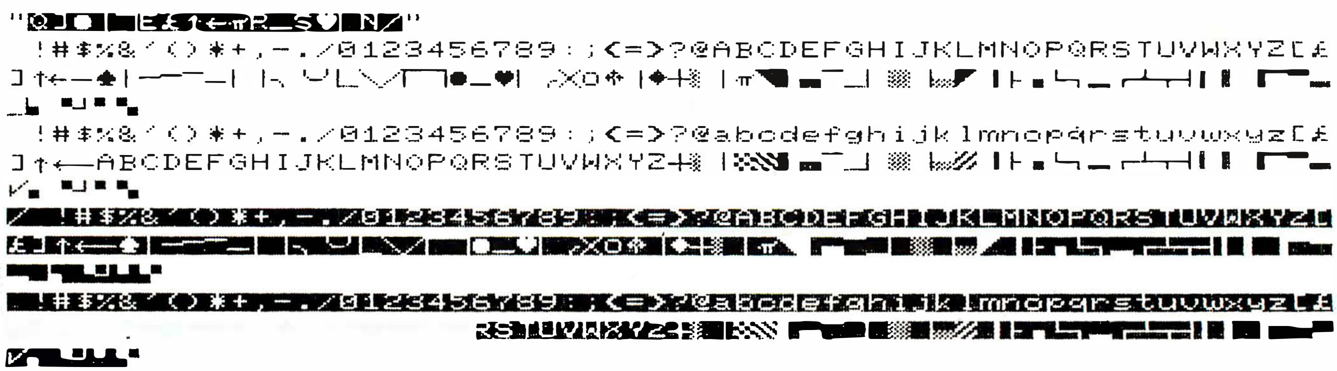
Text continued on page 286

Circle 61 on inquiry card.

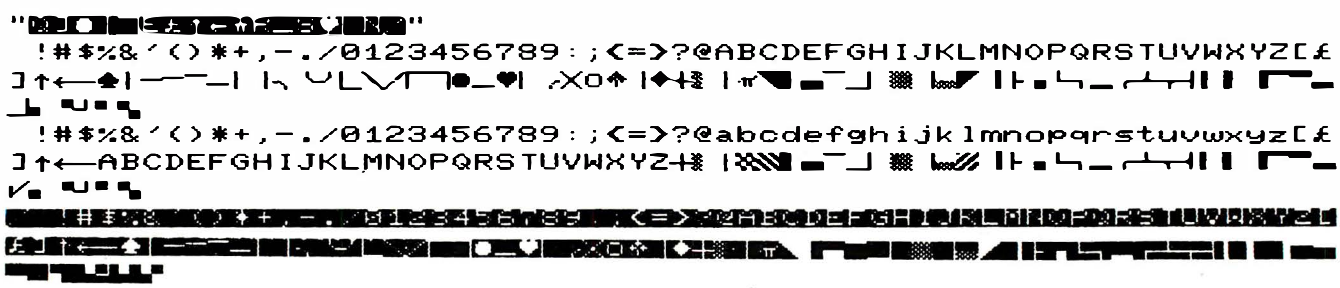
Listing 2: *The CHARACTER SET program will print the entire VIC-20 character set. You can select the print density and line spacing. A sample of each print mode is shown below the listing.*

```
100 REM PROGRAM TO PRINT ALL VIC CHARACTERS
110 INPUT "480 OR 960 MODE";MO$
120 IF MO$="480" THEN MO=0:GOTO140
130 MO=1:IF MO$<>"960" THEN 110
140 PRINT "6 LPI, 8 LPI OR"
145 INPUT "GRAPHIC";LP$
150 IF LP$="6" THEN LP=0:GOTO200
160 IF LP$="8" THEN LP=1:GOTO200
170 LP=2:IF LP$<>"G" THEN140
200 POKE 780,LP:POKE 781,MO:SYS(7168)
250 PRINT:PRINTMO$;" MODE AT ";
260 IF LP$="G" THEN LP$="GRAPHIC DENSITY":GOTO 280
270 LP$=LP$+" LPI"
280 PRINT LP$:PRINT
300 PRINTCHR$(34);"[illegible]";
350 PRINT CHR$(14);CHR$(142);CHR$(34)
400 GOSUB1000
500 PRINT CHR$(14);:GOSUB1000
600 PRINT CHR$(142);CHR$(18);:GOSUB1000
700 PRINT CHR$(14);CHR$(18);:GOSUB1000
800 SYS(7202)
850 PRINTCHR$(142);
900 END
1000 FOR I=32TO 127
1010 IF I=34 THEN NEXTI
1020 PRINT CHR$(I);
1030 NEXTI
1100 FOR I=161TO191
1110 PRINT CHR$(I);
1120 NEXTI
1130 PRINT
1140 RETURN
READY.
```

480 MODE AT 6 LPI

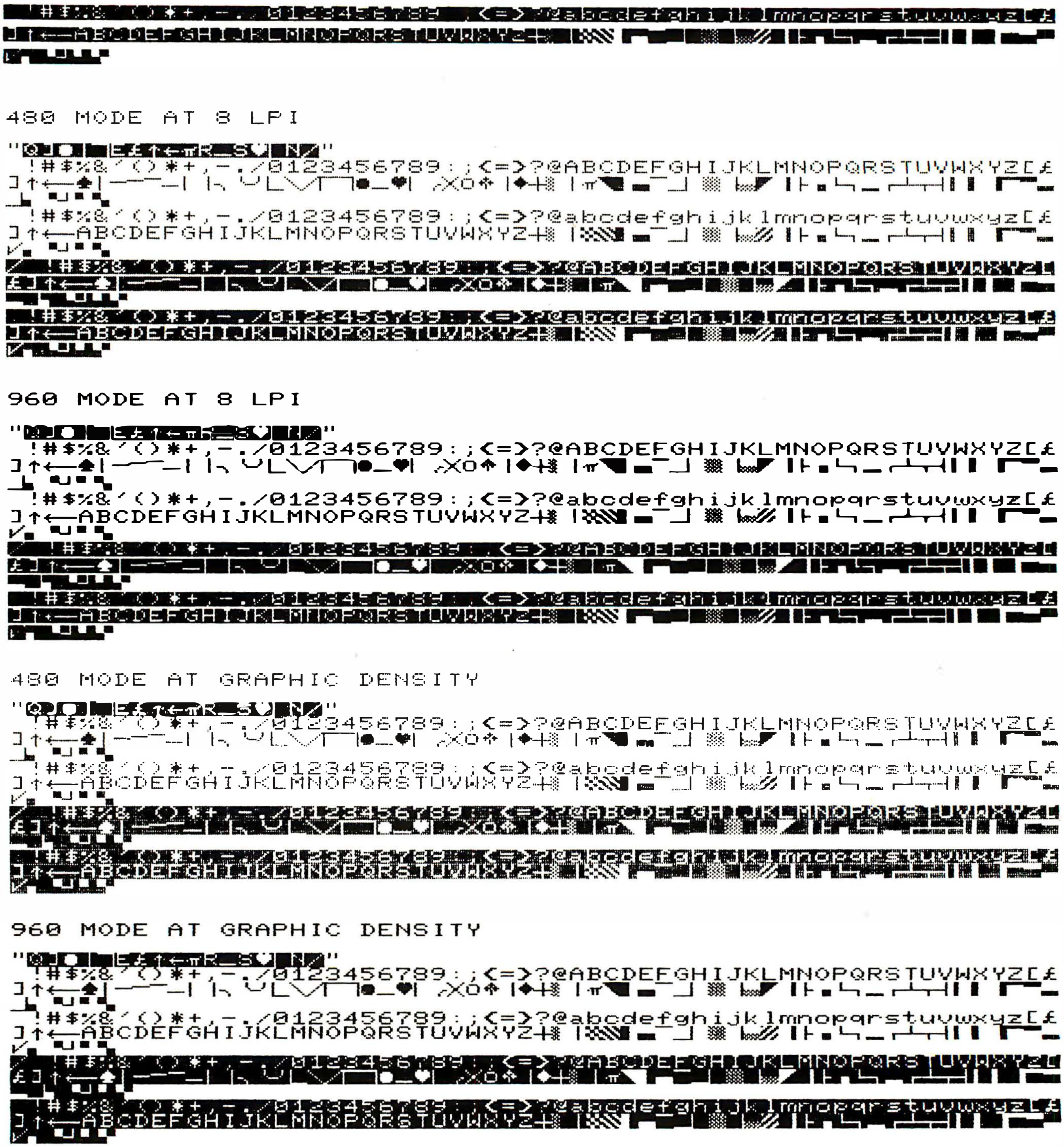


960 MODE AT 6 LPI



Listing 2 continued on page 286

Listing 2 continued:



Text continued from page 282:

0. To invert the characters, you could change it to start at 0 and increment through 7. Listing 3 is an example of how you could rewrite this section of VICEPS for such a printer. Notice that this routine requires slightly more memory than its counterpart in VICEPS.

It is possible to print full VIC graphics with a 7-wire printer. To do this, the program would have to store an entire line of character patterns in memory, then send them in two lines to the printer. The top half of each character would be printed on the first line, then the paper would be advanced half the height of a character, then the bottom half of each character would be printed. If the alignment were perfect, the characters would look as if they had been printed with an 8-wire printer. Printing this way would require an extra 480 bytes of memory to store all the patterns.

If you have a 7-wire printer you'd like to use with the VIC, you might consider another solution. It's possible to achieve acceptable results by printing only the top 7 dots of the VIC character and eliminating the bottom row altogether. The VIC capital letters and numbers don't use the bottom row of dots, anyway. Graphic characters

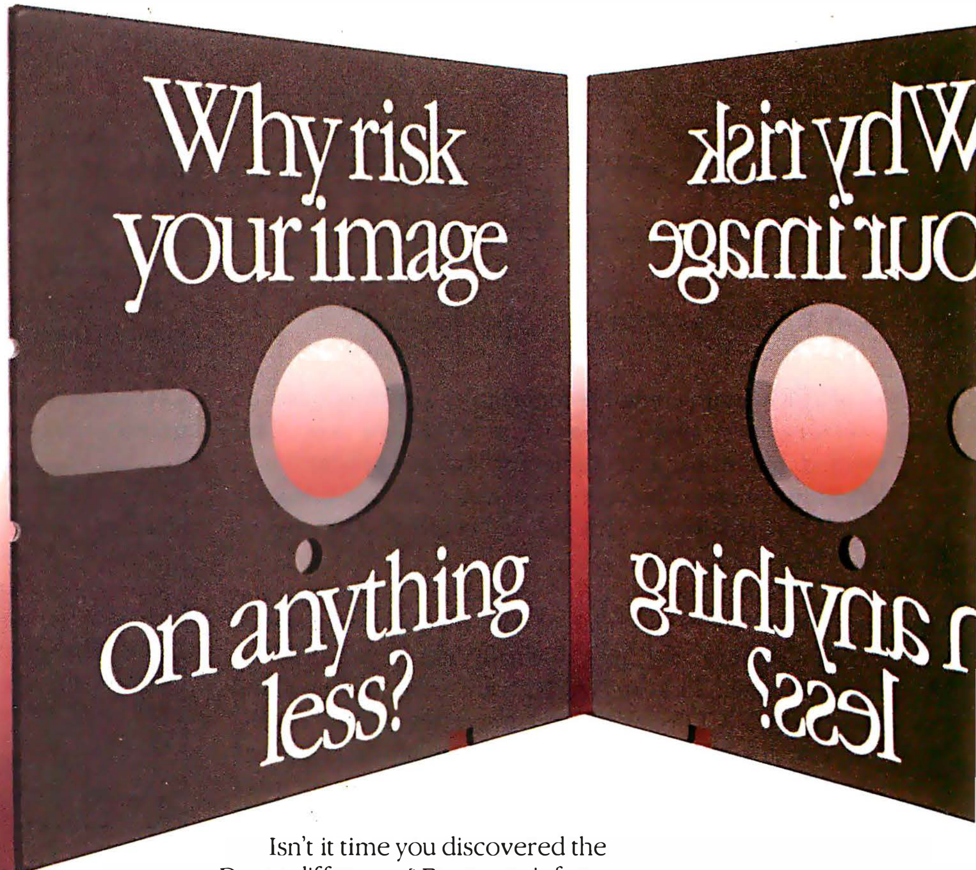
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Listing 3: *An alternate version of the SEND subroutine for the VICEPS program. This enables you to use the program with other printers that use the reverse of the MX-80's representation of dots in a column.*

```
1CEC                   :    CONVERT VIC PATTERN TO PRINTER PATTERN
1CEC  A0 00                 LDY #0
1CEE  B1 FB        BYTLUP LDA (VICPAT),Y   ;GET A VIC PATTERN ROW
1CF0  A2 00                 LDX #0
1CF2  0A           BITLUP ASL A            ;SHIFT EACH BIT INTO A
1CF3  7E 97 1D              ROR PRTPAT,X   ;COLUMN OF THE PRINTER PATTERN
1CF6  E8                    INX
1CF7  E0 08                 CPX #8         ;GOT ALL 8?
1CF9  90 F7                 BCC BITLUP     ;NO, DO ANOTHER
1CFB  C8                    INY            ;YES BUMP Y TO NEXT ROW OF VIC PATTERN
1CFC  C0 08                 CPY #8         ;DONE THEM ALL?
1CFE  90 EE                 BCC BYTLUP     ;NO, CONTINUE
```

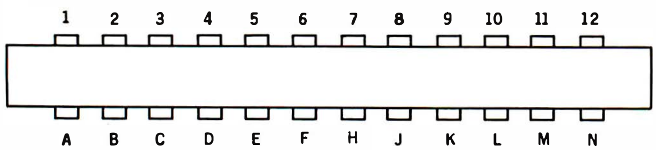


Figure 1: *VIC-20 user port I/O connections.*

would be incomplete but recognizable. The descenders on lowercase and special characters would be lost. This method might be acceptable for many applications. I have implemented both of the above solutions using my Base 2 7-wire printer. This method could also be used on the VIC-1515 printer.

VICEPS as shown in listing 1 resides in VIC memory at location 1C00 hexadecimal. It uses the top two pages of BASIC memory, the area normally used by BASIC for string storage. To keep BASIC from using this area and destroying VICEPS, you must move the end of BASIC memory down by using a POKE command to enter a 28 into locations 52 and 56. On an expanded VIC with more than 8K bytes of memory, 1C00 would not be a very good place to locate VICEPS because it would be right in the middle of BASIC memory. Assembling VICEPS at a higher address would be better.

Conclusion

By interfacing a full-featured printer to the VIC-20, you can make lighter work of developing programs. And by breaking the VIC out of the benevolent grasp of Commodore-manufactured peripherals, you can further unleash the power of this talented computer. ■

The VICEPS program has been incorporated into a full-featured printer driver program for the Epson and other printers. The program supports VIC graphics and all Epson functions via standard BASIC OPEN, CLOSE, and PRINT# statements (no SYS calls). It also has a special mode that formats BASIC program statements for readability. It will communicate to the printer via either the parallel method described above or via an RS-232C interface at up to 9600 bits per second with handshaking. For more information contact United Microware Industries Inc., 3503C Temple Ave., Pomona, CA 91768.

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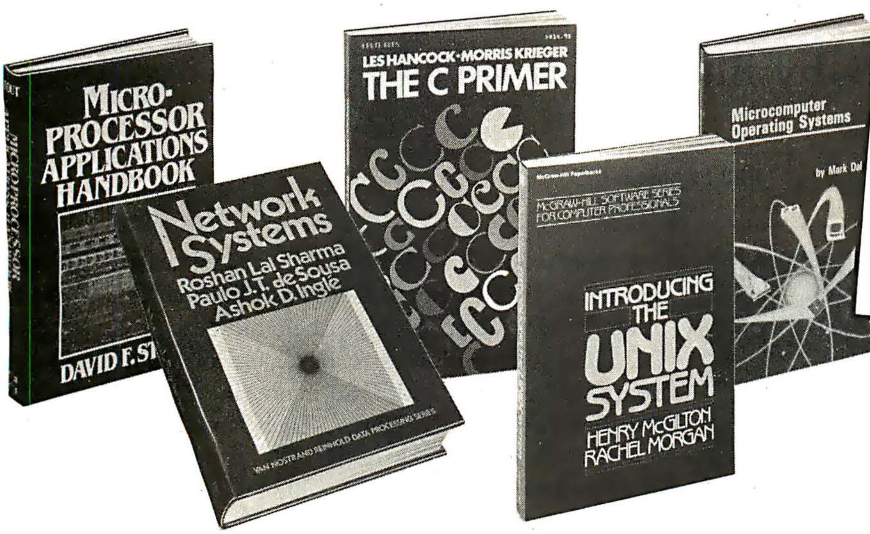
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Two Ways to Use CP/M-80 on the IBM PC

Xedex's Baby Blue and Byad's DS1

Phil Lemmons
West Coast Editor



Photo 1: *The Baby Blue CPU Plus from Xedex converts your CP/M-80 files into PC-DOS format and attaches a header to the file to identify it. You don't have to keep track of two different file formats.*

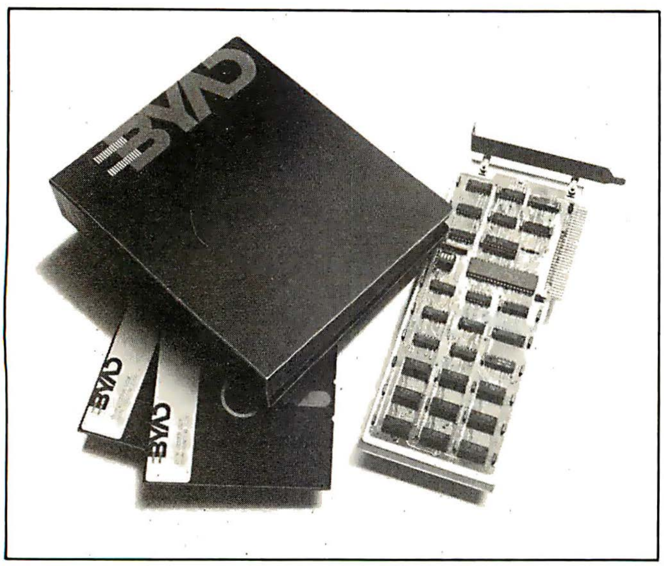


Photo 2: *The DS1 from Byad uses a technically more elegant approach to integrating the Z80B system into the IBM PC. When the Z80B is in control, the 8088 uses its system memory for disk and print buffering.*

People who own a lot of CP/M-80 software but want to buy an IBM Personal Computer have several choices about how to keep running their old software with the PC. One such option is to purchase an 8-bit processor board. Both Xedex and Byad make fine Z80B boards for the IBM Personal Computer. Each has a printed-circuit board with 64K bytes of RAM (random-access read/write memory) as well as the Z80B microprocessor. What distinguishes these boards is the software sold with each and the way they integrate with the IBM PC. Choosing between the boards is largely a matter of determining your software needs.

Xedex and Byad provide utility programs for converting some 5¼-inch CP/M-80 disk file formats to the format used by each of the new boards. Both companies found the problem of conversion much more complex than initially thought. (See the text box, "Reading CP/M-80 Disk Formats with the IBM PC," on page 298.) If you need to convert a lot of disk files (whether data or programs) for use with Xedex's Baby Blue or Byad's DS1, be sure that software is available from Xedex or Byad to handle conversion of your old disk format. If neither company has software to read your old disk format, you may still be able to send your old data to the IBM PC on a serial communications line. Both companies supply the necessary software for receiving data on the IBM PC as part of the standard DS1 package.

Xedex's Baby Blue CPU Plus

Xedex's software for the Baby Blue includes programs called Header, Bind, and Convert. Header must be added to the beginning of each CP/M-80 program in order for the program to run on Baby Blue under PC-DOS, IBM PC's operating system. (You don't actually get CP/M-80 with Baby Blue; it emulates CP/M.) Bind attaches Header to the beginning of CP/M-80 files. Convert takes CP/M-80 programs in any of four different disk formats—NEC PC-8001, IMS 5000, DEC VT-180, Heath/Zenith (48 tracks per inch)—converts them to PC-DOS format, and then attaches Header to the beginning of the

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At a Glance

Name
Baby Blue CPU Plus

Type
Z80B card for running CP/M-80 programs on the IBM Personal Computer

Manufacturer
Xedex Corporation
Box 222, Route 59
Suffern, NY 10901
(914) 368-0353

Price
$600

Hardware
A printed-circuit board with a Z80B microprocessor and 64K bytes of dynamic RAM with parity

Software
Header, a prefix for CP/M-80 programs that enables them to run under PC-DOS in the IBM Personal Computer; Bind, a program that attaches Header to the beginning of CP/M-80 files; Convert, a program that converts four 5¼-inch CP/M-80 disk formats—NEC PC-8001, IMS 5000, DEC VT-18, Heath/Zenith (48 tracks per inch)—and the CP/M-86 format for the IBM Personal Computer into IBM PC-DOS disk format

Documentation
Forty-page typeset manual with index

Audience
Any IBM PC owner who needs to run CP/M-80 software

converted file. In other words, Convert does the same work as Bind but also converts the file to PC-DOS format. After the Header is added, whether by Bind or by Convert, the user can invoke the CP/M-80 program just as if it were a program written for the IBM PC. When PC-DOS finds the Xedex Header on a file, the operating system sends the program to Baby Blue's Z80B for execution. While the Z80B executes the CP/M-80 program, the Header sends CP/M-system calls to the IBM PC's 8088 microprocessor. Then the 8088 manages input/output for the CP/M program. Software with the Baby Blue also includes a program for moving files through the PC's serial port.

Baby Blue is easy to install and use, performs as advertised, and has a superb user's guide. One of Baby Blue's beauties is that after converting your 8-bit programs to PC-DOS format, you no longer have to worry about managing two different file formats on one computer. You don't have to keep track of which disks are CP/M-80 disks and which are PC-DOS disks. Most important of all, any CP/M-80 program or PC-DOS program can access and process any of your data files, because they are all in PC-DOS format. Well, perhaps not any program. The Baby Blue user's guide says (pages 21 and 22), "We have never promised anyone perfect compatibility with CP/M-80. . . . What's of interest to us and to the majority of users is compatibility with plain-vanilla, no-tricks, maximally portable, hardware-independent CP/M-80 programs." The only software that the Baby Blue definitely won't run is CBASIC. The Baby Blue console interface emulates the Televideo 950 terminal to support screen handling (cursor placement, etc.) of CP/M-80 programs.

Baby Blue is easy to install because the procedure is straightforward and the user's guide is written and illustrated well. Photographs orient the user at different stages of installation. The instructions for resetting the IBM and Baby Blue switches to configure both the PC and the Z80B board for different amounts of memory leave nothing to chance. Side-by-side illustrations of the correct positions of all eight switches for the PC and Baby

Blue cover every possibility in 32K-byte increments all the way from 128K bytes (including Baby Blue's own 64K bytes) to 544K bytes. Steve Walton, the author of the Baby Blue user's guide, could do the microcomputer world a great service by teaching courses in how to write clear and pertinent documentation.

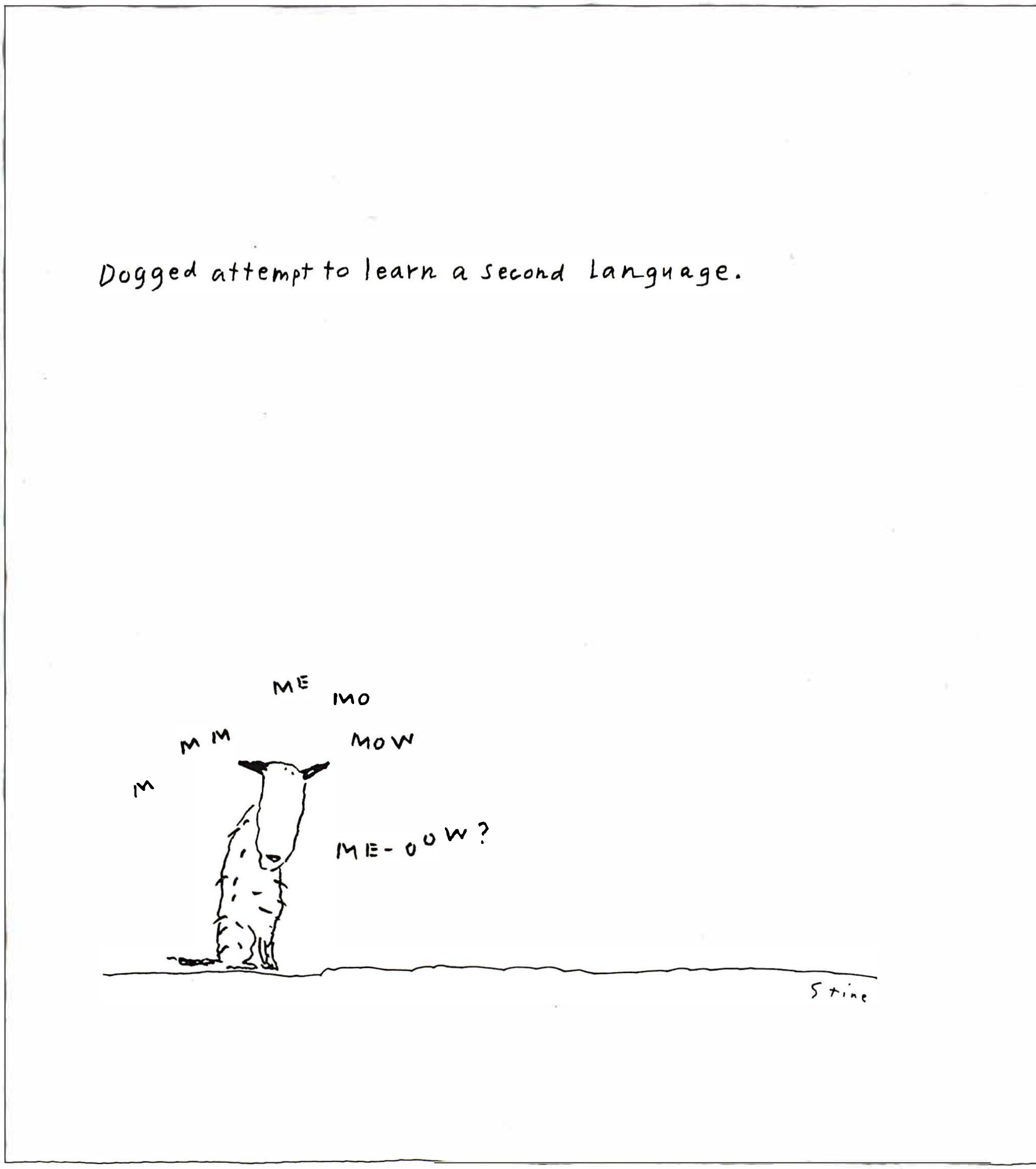
If you already own 8-bit versions of your favorite applications programs, you will probably want to convert them and run them on Baby Blue. It is worth noting, however, that Xedex sells versions of Wordstar and Mailmerge for Baby Blue. In fact, Xedex has done a better job of adapting Wordstar to run on Baby Blue than Micropro has done of converting Wordstar to run on the IBM PC's 8088. Xedex's version of Wordstar makes better use of the IBM PC's function keys by both using more keys and making better choices of which control codes are sent by the keys. Xedex sells Baby Blue, Wordstar, and Mailmerge as a package for a total of $980. In effect, you get the 8-bit versions of both Mailmerge and Wordstar for $380. Xedex also offers Personal Pearl and the Baby Blue for $650.

Note that Baby Blue's software does not include the CP/M-80 operating system and its utilities. You do not receive a license to CP/M-80 when you buy Baby Blue. Header and Bind just enable Baby Blue to execute machine-language command (.COM) files that will execute under CP/M-80. The usual procedure when selling one machine and buying another is to write the publisher of each program and pay a small fee to transfer your license from the old processor to the new one. Presumably you should do that before using Header and Bind to make your old CP/M-80 programs run on Baby Blue.

Byad's DS1

When you buy Byad's DS1, you buy both a Z80B board and a license to CP/M-80, including all its utilities. Obviously this implies complete compatibility with CP/M-80 (although some versions of CP/M-80 may differ in disk formats and hardware-specific features). Byad now sells CP/M-80 version 2.2 with DS1 but will also offer CP/M-Plus, the greatly enhanced new version of the venerable 8-bit operating system. For those IBM PC owners who have chosen CP/M-86 or Concurrent CP/M-86, the Byad DS1 (or its cousin, the DS2, which has its own RS-232C serial port that can also drive RS-422A lines) is the logical choice as a CP/M-80 card. The DS1 and DS2 use the same disk format on the IBM PC as CP/M-86.

The DS1's software includes programs called Transfer, Filex, and Setup as well as the usual CP/M-80 utilities (STAT, PIP, ED, etc.). Transfer enables you to capture data coming through the IBM PC's serial port. Filex lets you read certain 5¼-inch disk formats (including NEC PC-8001, Televideo, Cromemco, Heath/Zenith, Intertec Superbrain, and others) into the DS1 format. Setup is necessary for configuring the system after installing the DS1 board. Among other things, Setup lets you enhance CP/M by setting aside some of the PC's memory to serve as disk buffers, a print buffer, a serial-in buffer, and a



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At a Glance

Name
DS1

Type
Z80B card and CP/M-80 operating system for the IBM Personal Computer

Manufacturer
Byad Inc.
5345 North Kedzie Ave.
Chicago, IL 60625
(312) 539-4922

Price
$660

Hardware
A printed-circuit board with a Z80B microprocessor and 64K bytes of dynamic RAM with parity

Software
CP/M-80 and all its utilities; Setup configures the DS1 for different hardware and terminal emulation; Format formats disks; Filex converts files from certain CP/M-80 5¼-inch disk formats (including NEC PC-8001, Televideo, Cromemco, Heath/Zenith, and Intertec Superbrain) to Byad format; and Transfer enables the DS1 to receive files from another CP/M-80 computer

Documentation
Preliminary at time of review

Audience
Any IBM PC owner who needs to run CP/M-80 software

serial-out buffer. You can also choose to have the DS1 emulate one of three different terminals: the DEC VT-52, the Lear Siegler ADM 31, or the Heath H-19.

Installation of the DS1, following the instructions in the *preliminary* version of the manual, was somewhat awkward. The manual was about average; the only serious lack that I noted was instructions for setting the PC's switches to accommodate different amounts of memory. The blame for the awkwardness of installation, however, goes more to the procedure itself than to the manual. You must remove any other memory expansion boards from the IBM PC while installing the DS1. You must then set the PC system board switches for either 48K or 64K bytes of RAM. After putting in the DS1 board, you close up the system to see whether it will still run PC-DOS. Having done this, you remove the PC-DOS disk and boot the Byad CP/M-80 system and run some CP/M utilities (such as STAT, the disk status command) to confirm that CP/M works. No problem. But then you have to configure the system to use any memory not on the PC's system board or the Byad board.

Configuration takes two steps: first, edit the Byad file called SETUP.CMD; second, run SETUP.CMD. It sounds easy, but you have to use the CP/M editor ED to edit SETUP.CMD. ED is a primitive editor, and most people who use CP/M-80 use another editor. I had to reread the old Digital Research instructions for using ED in order to install the DS1.

Having relearned ED, I was all set to reconfigure the system for my expansion memory, which required entering the correct segment addresses. The DS1 instructions gave only four possibilities, so I was off to the IBM PC manuals. Having decided at last on the segment addresses, I went on editing SETUP.CMD in order to configure some of the DS1's buffers. I wanted to try using 64K bytes of RAM as a print buffer, but because I hadn't yet put back my own 256K-byte memory board or reset the system board switches, Setup informed me there was not enough memory for the desired buffer. I should have realized that. But I still faced a problem: I couldn't configure the system for my hardware until my own memory board was installed and the switches were adjusted, but the instructions told me that I also couldn't use the configuration procedure until after removing my memory board—sort of a "catch-22" installation procedure. The solution was to go through the setup procedure for one set of parameters, reinstall my memory board, and then repeat the configuration procedure. At length, after rereading the Byad preliminary documentation and reexamining the ED documentation, I succeeded in installing the DS1. Of course, although the setup procedure is awkward and time-consuming, installation is usually a one-time event, and the DS1 documentation was preliminary.

To use CP/M-80 with the Byad board, you just boot the IBM PC with the Byad system disk in drive A. After doing so, I had no difficulty in running a variety of CP/M-80 applications programs on the DS1. Performance seemed excellent.

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[**Late notes:** *Scott Bartky of Byad informs me that the installation procedure has been simplified since I used the system. The instructions now require using ED to edit only a single line of text and show exactly what the user must type to edit that one line. In addition, the instructions list the segment address that must be entered for any amount of memory that may be in the machine.*]

At Comdex in November, Byad and Digital Research announced an agreement under which Byad will produce a new Z80B card to be called the CP/M Card. The new card will be equipped with 256K bytes of RAM, a Z80B, and a serial port. Digital Research acquired all rights to the CP/M Card, including the marketing rights. The availability of the CP/M Card with CP/M-86 for the IBM PC will enable CP/M users to run 8- and 16-bit software without worrying about maintaining two different disk file formats. Using the CP/M Card along with Concurrent CP/M-86 will make possible running a CP/M-80 program as one task while the 16-bit operating system is in control. Byad itself will also be bringing out a Z80B board with up to 256K bytes of memory and is making its boards compatible with PC-DOS, no longer requiring the user to keep separate disks for PC-DOS and CP/M-80.

Conclusion

If you just want to run your old 8-bit machine-language programs on your IBM PC, then Xedex's Baby Blue CPU Plus probably suits your needs. If you want to continue doing work with the CP/M-80 utilities or to keep revising your old 8-bit assembly-language programs, then the Byad DS1 is the better choice (though you can use CP/M development tools, languages, linkers, etc., with Baby Blue). Another major factor in deciding on one of these two boards is your choice of 16-bit operating systems for the IBM PC. If you are using PC-DOS (Microsoft's MS-DOS) exclusively, you will want Baby Blue CPU Plus. If you are using Digital Research's CP/M-86 or Concurrent CP/M-86, you will want the DS1.■

Reading CP/M-80 Disk Formats with the IBM PC

W. Scott Bartky
Byad Inc.
5345 North Kedzie Ave.
Chicago, IL 60625

In designing a Z80B board to let users run CP/M-80 on the IBM Personal Computer, we encountered several obstacles that made it difficult to read CP/M-formatted 5¼-inch soft-sectored disks on that machine. Although the disks were supposedly physically compatible with the PC, a combination of three factors determined whether or not a successful read operation could take place.

One factor was a problem in the disk-controller hardware. The IBM PC uses a disk-controller chip manufactured by Nippon Electric Company, the NEC 765 or 765a. Either chip has a built-in reset tied to the detection of the disk's index hole. If you try to read a disk that has been formatted with the first sector too close to the index hole, the chip doesn't have enough time to reset itself and read the disk.

The solution is simple: cover the disk's index hole. Most popular soft-sectored formats identify each sector by the sector's header block. The controller does not need to use the index hole for locating a given sector. Fortunately, the 765 does not require the index hole to either read or write data. In fact, the index hole is important only when formatting the disk.

To use this solution, you should start all disk records at the same point on each track so that track-to-track seeks can take place quickly and efficiently. Once the disk is formatted, the hole can be covered, and the controller will still be able to read and write data. The only possible complication is that the operating system may never wait the maximum time needed to read a disk if your machine uses the index hole for this purpose. The IBM PC uses an independent time-out schema, and the covering of the hole won't produce a change in performance.

With the hardware problem solved, we soon found another obstacle to reading disks formatted on other systems. Some systems format their disks in ways that violate common rules of good engineering practice. For example, Intertec's implementation of ten 512-byte sectors per track exceeds the sensible track-length specification by some 70 bytes. This design reduces the size of the interrecord gap, the space between the first and last sectors on a track.

When we find a format in which this interrecord gap is too small, we use either of two possible solutions. One is to set up a formatting function on the IBM PC to format disks for the nonstandard machine. Then we take the disk formatted by the IBM PC, use it with the other machine and transfer all the files to that disk. A second solution is to slow the speed of the nonstandard machine's drive slightly (about 1 percent) to produce a longer interrecord gap when it formats a disk. Neither solution may work all of the time because multiple writing and reading may cause "creeping" of the records, and the gap will shorten once more.

The third problem affects even well-designed disks such as Cromemco's. IBM uses a phase-locked loop (PLL) in its data separator. Unlike the simpler one-shot multivibrator designs, used in some older systems, that synchronize to the data stream in two pulses, the PLL requires several clock pulses to lock in. (Although it requires the additional pulses, the PLL is a better design than its simpler counterpart because it is less susceptible to noise and rapid fluctuations.) If you attempt to read disks from an older system and are unsuccessful, it is highly probable that your problem is in the data separator design. There is no permanent cure for this incompatibility without altering the IBM card—a complicated operation. All you can do is try again or transfer the data through some other means.

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Building a Hard-Disk Interface for an S-100 Bus System

Part 2: The Hardware

Andrew C. Cruce and Scott A. Alexander
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In last month's article we described Winchester disk-drive technology and generally how drives of this type are integrated into microcomputer systems. This month we will be more specific and describe how a particular set of hardware can be assembled to provide Winchester disk capability for an S-100-bus microcomputer. After reading this article, you should understand the concepts involved in the design, fabrication, and integration of the hardware needed for a 10-megabyte S-100-based Winchester disk system.

The block diagram presented in figure 1 shows the various components of the Winchester disk subsystem. The functions of the host computer adapter (HCA), the disk controller, and the disk drive were described in last month's article. The only remaining component in the diagram is the power supply, which provides the disk drive and controller with power.

About the Authors

Andrew Cruce has a Ph.D. in Aeronautical Engineering and has recently received an S.M. degree in management as a Sloan Fellow at MIT. Scott Alexander has an M.S. in Electrical Engineering. Both have extensive design and implementation experience with small computers and are full partners in the firm of ASC Associates, which markets the hardware described in this series of articles.

This diagram suggests an approach to designing the disk system. The first step is to establish the data path; that is, you must determine how the HCA, the disk controller, and the disk drive are connected. Before you can do this you need to settle on the particular disk and controller to be used in the system as well as the functions that are to be included in the HCA. Once you complete this process, you'll have enough information available to specify power requirements for the system and to identify power supplies that could be used in the system. Finally, when the data interface is complete and you've chosen a power supply, you can consider how to package the system.

We'll now proceed through this design sequence, first discussing the availability of disk drives and controller cards and which ones we ultimately adopted. Next we'll cover the requirements for the HCA and go into the detailed logic design of this component. Finally, we will examine some of the options in choosing a power supply for the system and show the steps required to construct an attractive and reliable package for the system.

Disk Selection

The first decision we made in selecting a disk was on its size and storage capacity. As we stated last month, we chose the 5¼-inch disks because they offered what we consider to be more than sufficient storage capacity for most applications at a reasonable price. When we started this project, a number of manufacturers, including Seagate Technology, Shugart, Memorex, and Miniscribe, offered 5¼-inch Winchester drives. We needed a drive with a disk-to-controller interface equivalent to that of the ST-506 disk drive manufactured by Seagate Technology. This interface has become the de facto standard in the industry and provides the freedom to select from a number of potential controllers that are compatible with this interface.

In considering the storage capacities available on the 5¼-inch-drive systems, we found that 10-megabyte systems were becoming available at prices only marginally higher than the smaller 5-megabyte systems. Based on the attractive cost per bit of storage capacity of the 10-megabyte drives, we opted for the higher-capacity disk systems.

With these criteria in mind, and taking into account the price/performance ratios of the available units, we chose the 10-megabyte disk drive manufactured by the Miniscribe Corporation. Our initial choice could change because we made it at a time

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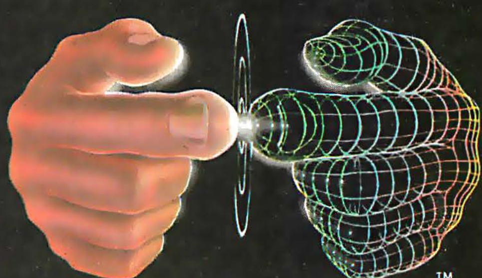
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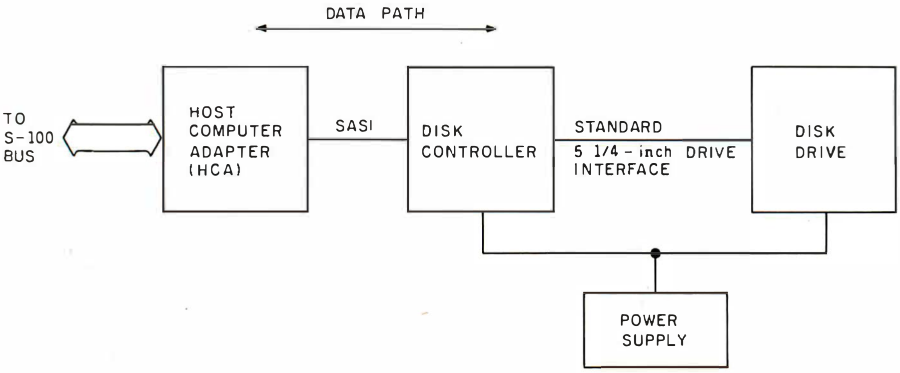


Figure 1: *Winchester disk-drive subsystem block diagram.*

when many disk-drive manufacturers had not yet commenced delivery of 10-megabyte hardware. However, now that the Seagate Technology interface has become the industry standard, virtually any new 5¼-inch drive currently being manufactured could be immediately plugged into whatever controller we selected. This also means that, for the purposes of this article, you could substitute any other 5¼-inch Winchester disk drive as long as it uses the Seagate Technology standard interface.

Controller Selection

Our decision on which controller to use in the system was somewhat more complicated. The first and most important requirement was that the controller be compatible with the Seagate Technology ST-506 interface (so as to be compatible also with any of the disk drives we were considering).

The second requirement was that the controller implement the Shugart Associates Systems Interface (SASI) to the HCA so that we could interface not only to S-100 systems, but also to a variety of other microcomputers such as the Apple, the Osborne, and the TRS-80. This criterion eliminated some of the available controllers, including those made by Morrow, which interfaced directly with the S-100 bus. A few of these devices would also have been eliminated because any system they are used in must conform to the IEEE standard for the S-100 bus. The problem here is that many of the older S-100 systems do not conform completely to this standard (for example, a number of systems do not implement the extended 24-bit addressing of the IEEE S-100-bus specification) and thus would not operate properly with the "S-100-compatible" controllers.

Working within these constraints, we considered the cost, performance, size, and power consumption characteristics of a number of commercially available Winchester disk-drive controller boards. At the time we made the selection, the Xebec S1410 controller appeared to offer the best performance per dollar expended. Again, for purposes of this article, the choice of the particular controller board does not largely influence the rest of the design. If you have a controller board that uses the SASI to connect to the HCA and a Seagate-Technology-compatible interface to connect to the Winchester drive, then the hardware and software designs covered in this series should work with little or no modification.

After we verified that the controller and disk were indeed compatible, all we needed to complete this interface was to fabricate a 34-conductor and a 20-conductor ribbon cable to connect the disk and the controller. The next step was to decide on the requirements for the HCA and to design the hardware accordingly.

HCA Interface Requirements

Several preliminary choices had to be made before we designed the host computer adapter for the Winchester disk system. The first was whether the disk subsystem should have DMA (direct memory access) capability. The alternative was to design the HCA to allow the host computer to perform data transfers between the disk and computer memory. Based on our assessment of most microprocessor system requirements, we considered that the additional speed gained by providing DMA capability in the HCA was not worth the additional complexity and expense that this capability would require. Thus we initially decided that the HCA would not perform DMA data transfers from the disk to memory.

The second decision concerning the design of the HCA was whether or not this device should contain a PROM (programmable read-only memory) chip and a new system-bootstrap program. Assuming that the system to which the Winchester disk is to be connected is operable, it should already have a bootstrap program. However, this program is designed to work with the original disk peripherals. It is possible to interface a Winchester disk with such a system and then use a separate "Winchester Boot" program to bring the Winchester disk BIOS (basic input/output system) routines into the system. However, this means that a hardware bootstrap will always go to the original disk system and that the Winchester Boot program must always be run to bring the Winchester drive into the system. We considered this to be a fairly cumbersome procedure and decided that we should provide the capability for a new bootstrap for the system that would bring up the Winchester disk and all the previously existing peripherals in the system.

Host Computer Adapter Design

Based on these requirements, the design of the HCA can be divided into three essential elements: a connection to the SASI on the disk controller board, a PROM subsystem on the HCA board to store a new bootstrap program, and an interface to the S-100 bus that provides all the signals required to support the first two elements. The combination of these elements results in the initial top-level HCA block diagram presented in figure 2.

The SASI interface on the disk controller is a 2-byte parallel interface.

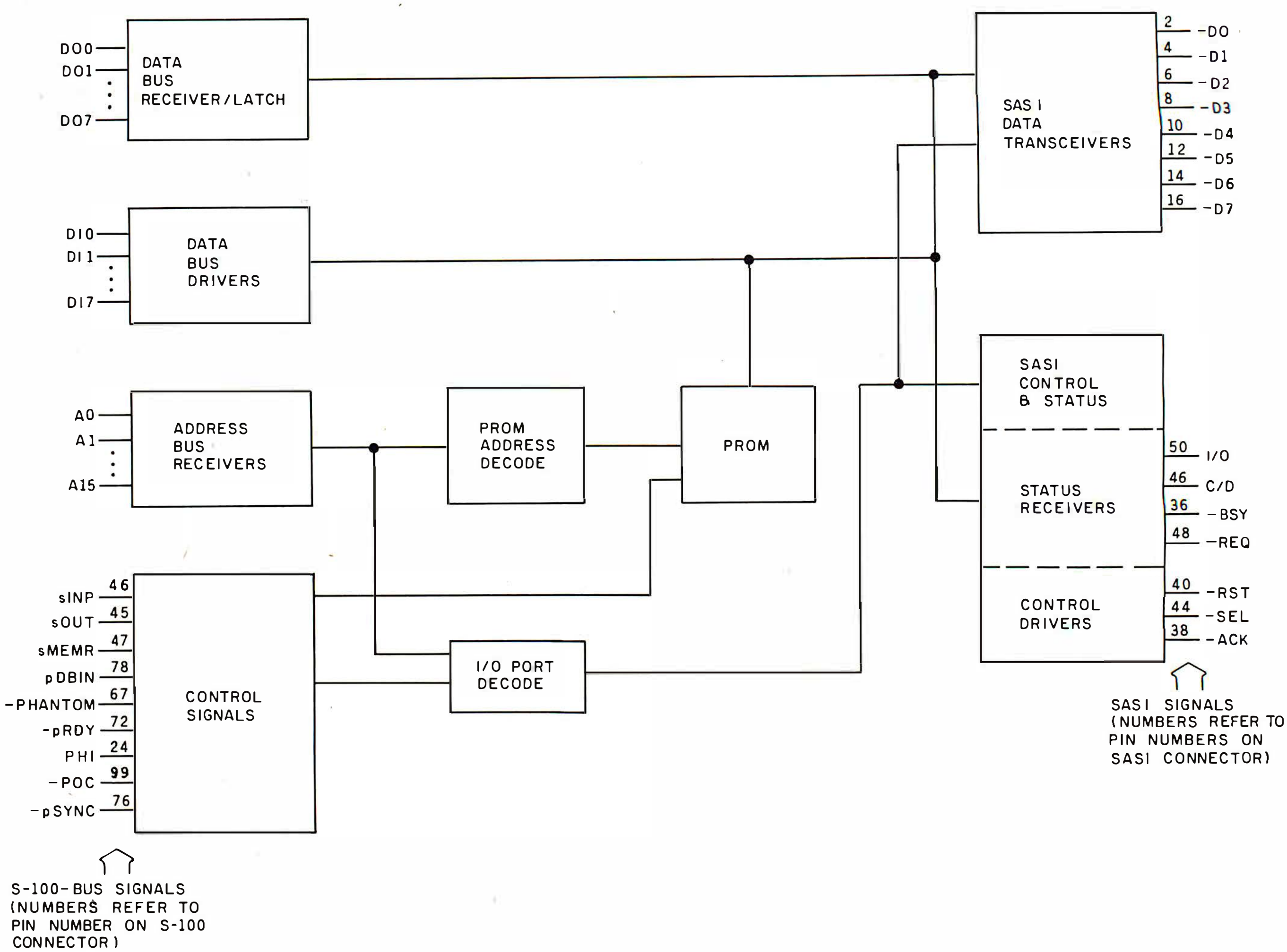


Figure 2: *Block diagram of the host computer adapter (HCA) for the Winchester disk drive.*

The first byte contains 8 bits of data being sent to or received by the controller. The second byte consists of control and status signals that are used by the host processor to determine the status of and provide control to the disk controller board. The controller board receives these signals on a standard 50-conductor ribbon cable. The signal names, descriptions, and pin numbers are presented in table 1. The portion of the HCA that communicates with the disk controller must send these signals to the controller, preferably via a 50-conductor cable.

The PROM portion of the HCA board is relatively simple in concept. Basically, it provides 2K bytes of nonvolatile memory to store a bootstrap loader. However, in considering the actual design, a number of questions arise. The first is whether to provide a wait state for access to the PROM. Depending on the speed of the processor being used, it may be necessary to make the processor wait during memory-access operations to allow the PROM time to access the requested data. Another question is whether to provide compatibility with memory systems that support phantom memory. In these systems the bootstrap PROM can be located in memory locations that overlay normal RAM (random-access read/write memory). During the bootstrap operation, the PROM system must assert a PHANTOM signal, which causes the RAM in the computer not to respond as long as the signal is asserted. Thus the PROM is accessed during the bootstrap, and then after the bootstrap is finished the PROM is disabled and conventional RAM memory replaces the PROM in memory. As we will show, neither of these two options is particularly difficult to implement, so we decided to design both a wait-state enable and phantom-memory support into the HCA. Again, figure 2 shows basically how these two capabilities fit into the system.

With the SASI interface and the PROM memory established, it is now possible to determine what signals from the S-100 bus must be used to communicate with these two elements. Accessing the PROM is like accessing normal memory. All that is required is some address-decode logic and some combinational logic using the S-100 bus signals sMEMR and pDBIN to gate the PROM data onto the S-100 bus. Several other signals are needed to support the memory wait state and the phantom-memory capability. These are the -pRDY signal going back to the processor (which keeps the processor in a wait state), the -PHANTOM signal back

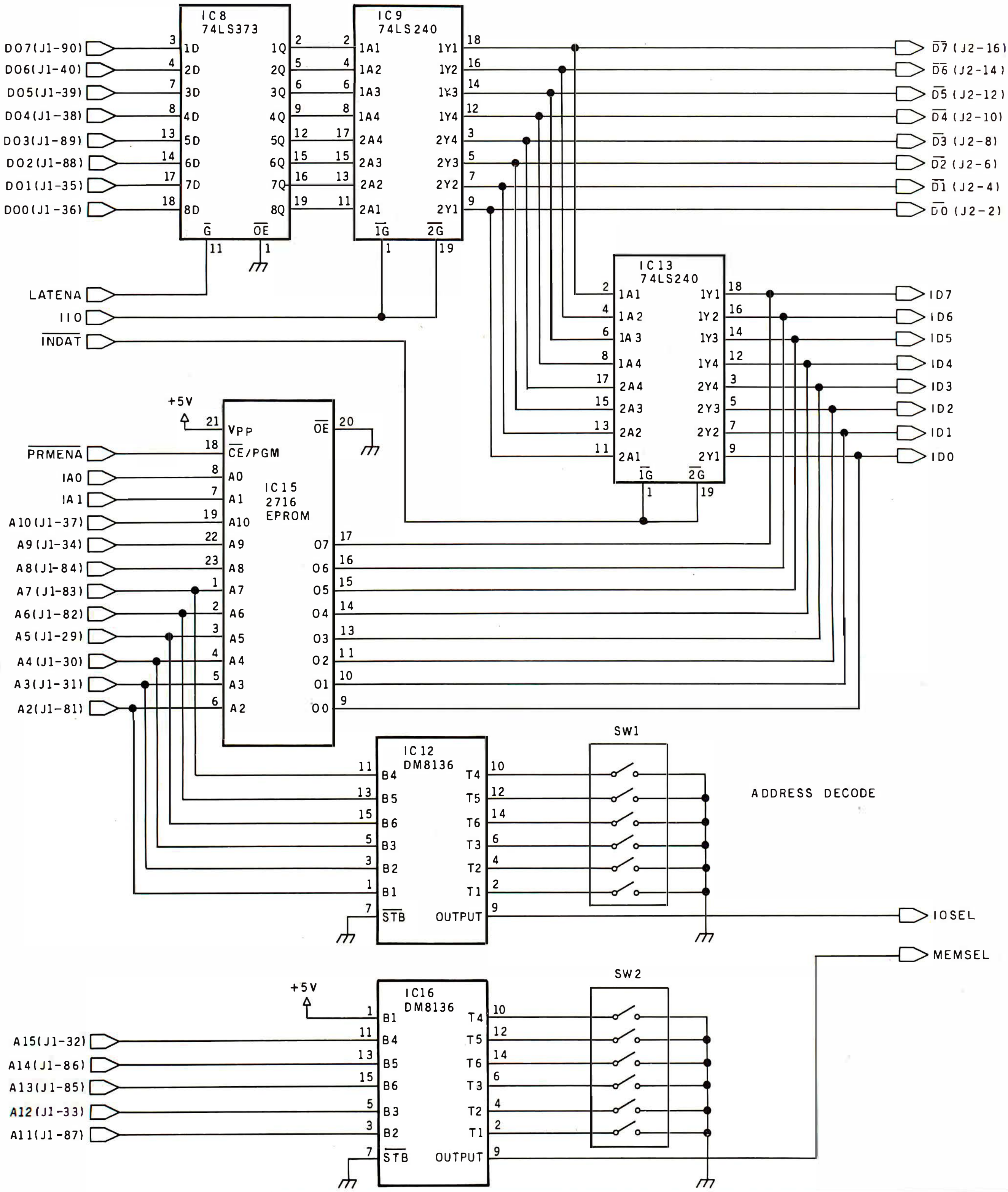
Signal Name	Pin Number	Description
I/O	50	Input/Output: open collector output from controller to HCA. Low level indicates a controller-to-HCA data transfer. This signal is qualified by -REQ.
C/D	46	Command/Data: open collector output from controller to HCA indicating command or data on the data bus. Low level means command bytes. This signal is qualified by -REQ.
-BSY	36	Busy: open collector output from controller to HCA indicating a controller is ready to receive data or command information from the HCA. High level means controller is ready for data.
-MSG	42	Message: open collector output from controller to HCA indicating that the current command is complete. (This signal is not used in our design.)
-REQ	48	Request: open collector output from controller to HCA to initiate controller-host handshaking sequence.
-ACK	38	Acknowledge: host-generated signal that is asserted active low in response to controller -REQ when the host is ready to receive or transmit data. In order to complete the handshake, the host adapter must send -ACK in response to each -REQ from the controller.
-RES	40	Reset: host-generated signal, active low, that resets the controllers. This signal must remain low for at least 100 nanoseconds.
-SEL	44	Select: host-generated signal, active low to initiate a command transaction to a controller.
-DB0	2	Data Bus 0 through 7: tristate input/output bus to send data/command information from the host to the controller or for the host to receive data from the controller.
-DB1	4	
-DB2	6	
-DB3	8	
-DB4	10	
-DB5	12	
-DB6	14	
-DB7	16	

Table 1: *Signals and pin locations for the Shugart Associates Systems Interface (SASI) between the disk controller and the host computer adapter (HCA).*

to RAM (causing it not to respond), one phase of the system clock (PHI), and the Power On Clear signal (-POC or -RESET).

In addition to supporting the PROM, it is also necessary to provide for data communication between the S-100 bus and the SASI ports on the HCA. There are two ways of doing this. One is to make the SASI ports appear as memory to the processor and use memory-mapped I/O to communicate with these ports. However, this uses up memory space, and a better approach is to use the I/O ports that are accessed by the 8080 IN and OUT instructions. This again calls for some address-decode logic to determine which port is selected and some combinational logic on the S-100-bus signals sINP and sOUT. These signals indicate whether data is to be written to or read from the particular port selected; figure 2 shows generally how they are used in the HCA design. They are standard S-100 signals, and a detailed description of their use and required characteristics can be found in any complete description of the S-100 bus.

In the logic design process, the block diagram shown in figure 2 is expanded to include the digital logic necessary to perform the functions in-



Number	Type	+5 V	GND	Number	Type	+5 V	GND
IC1	74LS10	14	7	IC10	74LS74	14	7
IC2	74LS139	16	8	IC11	74LS74	14	7
IC3	74LS244	20	10	IC12	DM8136	16	8
IC4	74LS00	14	7	IC13	74LS240	20	10
IC5	74LS04	14	7	IC14	74LS04	14	7
IC6	7438	14	7	IC15	2716	24	12
IC7	74LS240	20	10	IC16	DM8136	16	8
IC8	74LS373	20	10	IC17	74LS244	20	10
IC9	74LS240	20	10	IC18	74LS00	14	7

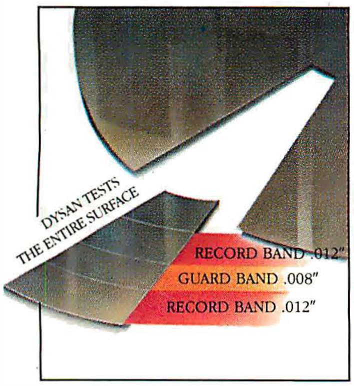
Power table applies to figures 4 and 5, as well.

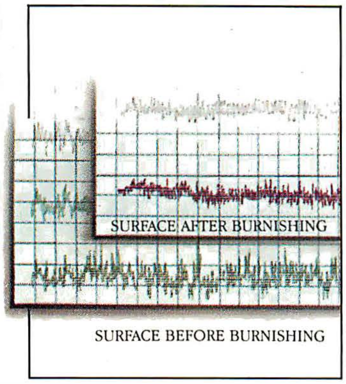
Figure 3: *Diagram of the address-decode logic of the HCA.*

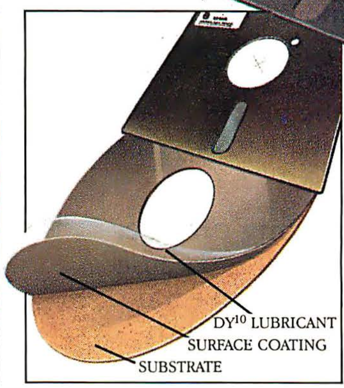
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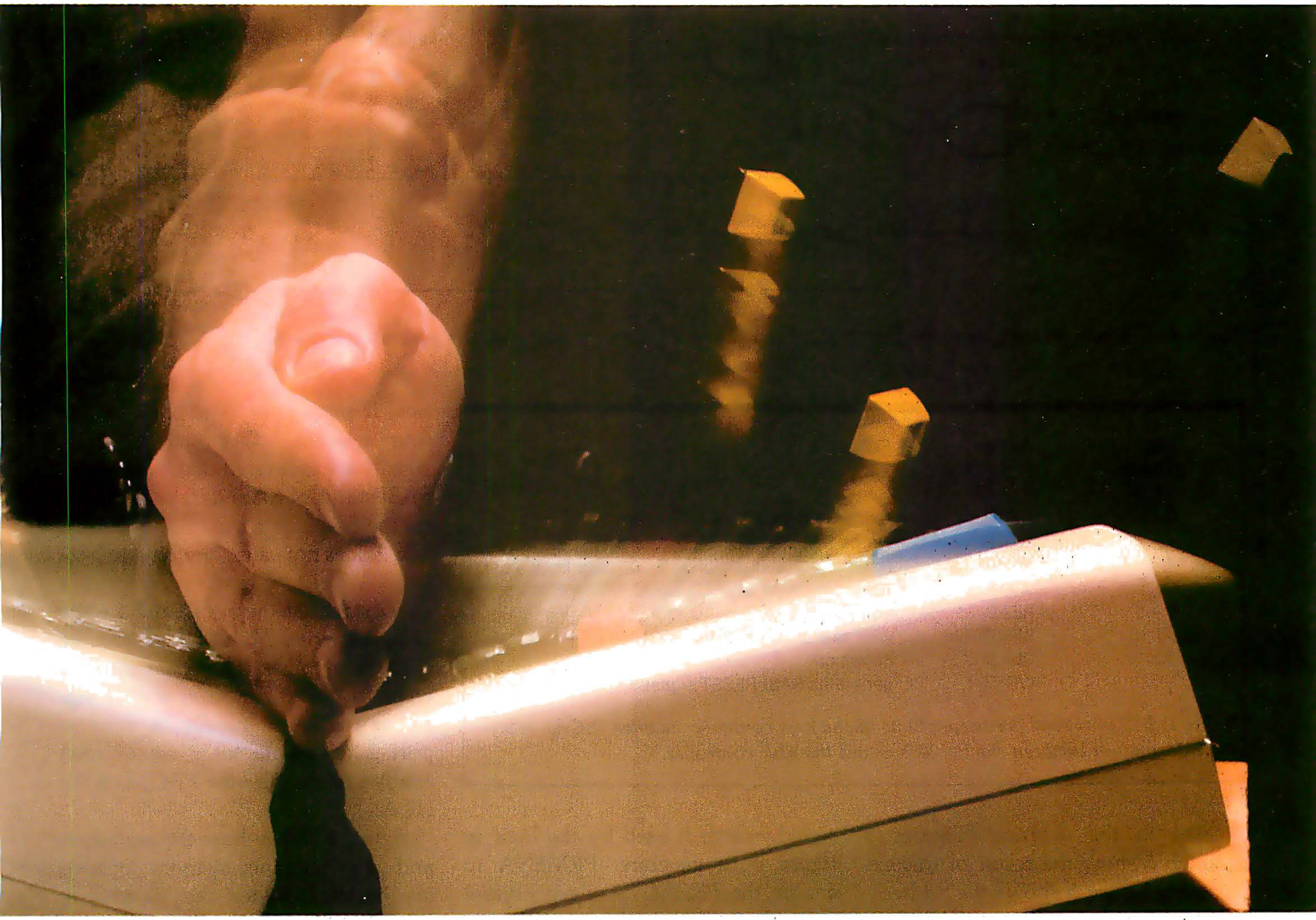
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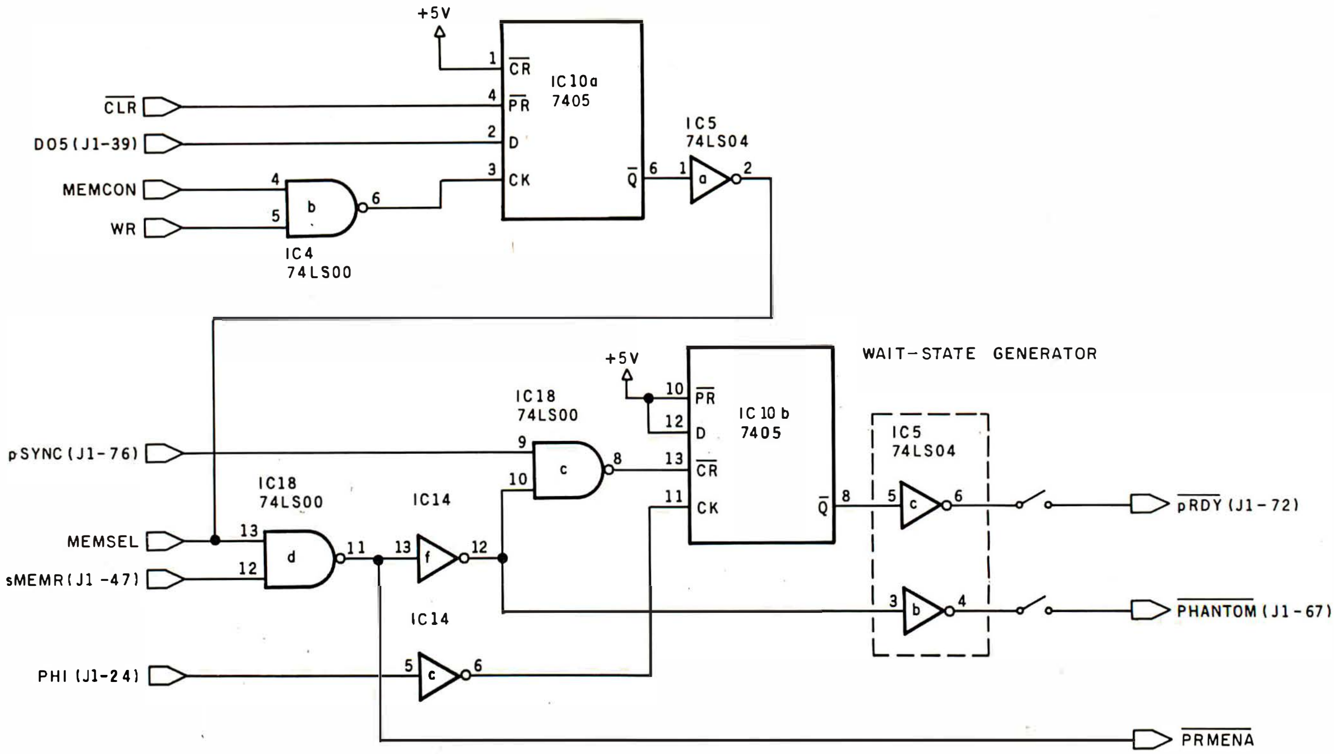


Figure 4: *Diagram showing how the PHANTOM signal and the memory wait state are generated in the HCA.*

Port Number	Action	Function
0	READ	reads SASI data onto S-100 data lines
	WRITE	writes S-100 data to SASI data port
1	READ	returns four status bits on S-100 data lines
	WRITE	generates SASI SELECT signal
2	READ	no action
	WRITE	with data bit 5 set turns PROM on
3	READ	no action
	WRITE	generates SASI RESET signal

Table 2: *I/O port read/write functions of the host computer adapter (HCA), relaying information between the S-100 bus and the disk controller.*

dicated in the diagram. Figures 3 through 5 show the result of this expansion. Figure 3 shows the address-decode logic and the S-100/SASI data bus buffering. Figure 4 shows how the PHANTOM signal and the memory wait state are generated, and figure 5 shows the port-decode logic and the remainder of the system.

The memory and port-address logic are set up so that the address of the PROM and the I/O ports are selectable using a set of switches on the HCA board. For the PROM, the upper five address bits are compared with a switch setting on the board and used to generate the MEMSEL signal, which is used by the logic in figure 4 to generate -PRMENA to enable the PROM. Similarly, bits 2 through 7 of the address are compared with switch settings on the HCA to determine if an I/O port on the HCA has been selected. If a match is found, IOSEL is asserted and bits 0 and 1 are used to determine which of four possible I/O ports has actually been selected. At this point there are eight possible operations because each possible I/O port may be either read or written depending on the status of the sINP and sOUT signals on the S-100 bus. Table 2 shows the results of each of these eight possibilities. If ports 0 or 1 (of the block of four selected I/O ports) are read, signals are generated that cause either SASI status or SASI data to be placed on the S-100 data bus. Reading ports 2 or 3 does not cause anything to happen. A write to port 1 generates a select signal at the SASI, and a write to port 0 writes 8 bits of data from the S-100 bus to the SASI data port. A write to port 3 generates a -RST signal at the SASI. Finally, a write to port 2 with data bit 5 set or reset enables or disables the PROM on the HCA.

Figure 4 shows how the wait-state and the phantom-memory options are handled. When the memory is selected, the output of the flip-flop U10 is set low and remains low until the next transition of the PHI clock signal raises it. This sequence generates the -pRDY signal, which is qualified by a switch setting. If the switch setting allows this signal to get to the S-100 bus, the result is a single wait state each time the PROM is selected. This allows use of PROM memory that would be too slow to respond to the high-speed Z80 processor boards on some S-100 systems. The upper portion of the figure also

shows the combinational logic used to generate the PHANTOM signal.

The PHANTOM signal is generated whenever the PROM is selected, depending on the state of flip-flop (U10). This flip-flop enables generation of the PHANTOM signal on receipt of the Power On Clear (-POC) signal and disables generation of PHANTOM when the host writes to port 2 of the four selected output ports with data bit 5 set. This whole operation is qualified by the switch on the board that either allows or disables PROM operation. For systems that support phantom memory, the intended mode of operation is to have the Power On Clear signal (which is the hardware boot signal) enable the PROM and the generation of the PHANTOM signal. The bootstrap in the PROM would then run and load a loader program into RAM. The loader program would then load the CP/M operating system, and (as a final instruction before transferring control to the operating system) the loader program would write data to port 2 with data bit 5 reset to disable the PROM from memory.

Figure 5 shows how this all comes together to perform the required HCA functions. For a PROM access, the upper five bits of the address, qualified as shown in figure 4, form the -PRMENA signal that enables the PROM. The lower eleven bits of the address are sent directly to the PROM to select the byte of data from the PROM that is to be read. This data is then placed on the S-100 data bus using the tristate bus driver (U17).

The way data and control information are transferred to and from the SASI depends on the particular portion of the SASI being addressed. The -RST and -SEL signals are generated by writing to ports 3 and 0, respectively. The -ACK signal is automatically generated if -REQ is asserted any time data is read from or written to the SASI. The control information from the disk controller to the host computer is read by sending an IN instruction to port 1. This places four bits of control information on the S-100 data bus. The data portion of the SASI is addressed by reads and writes to port 0. A data write to port 0 latches the data off the S-100 bus (U8) and passes this data through the data bus driver (U9) to the SASI if it is enabled by the SASI I/O control line. Data is received from the SASI data bus by U13. When the HCA is driving the data bus, the latched data from the S-100 bus will be turned around through U9 and U13 and will be available if a read is directed to port 0. This state exists whenever a controller is not active on the SASI bus and is useful for verifying the HCA data paths.

The next step in the design process is to take the logic diagrams shown in figures 3 through 5 and reduce them to a printed-circuit card that can be inserted in a standard S-100 bus 100-pin socket. Because the S-100 bus is fixed, the only choice in this operation is to decide how the HCA card will be physically connected to the disk controller card. For our controller card, this is done using a

Text continued on page 319

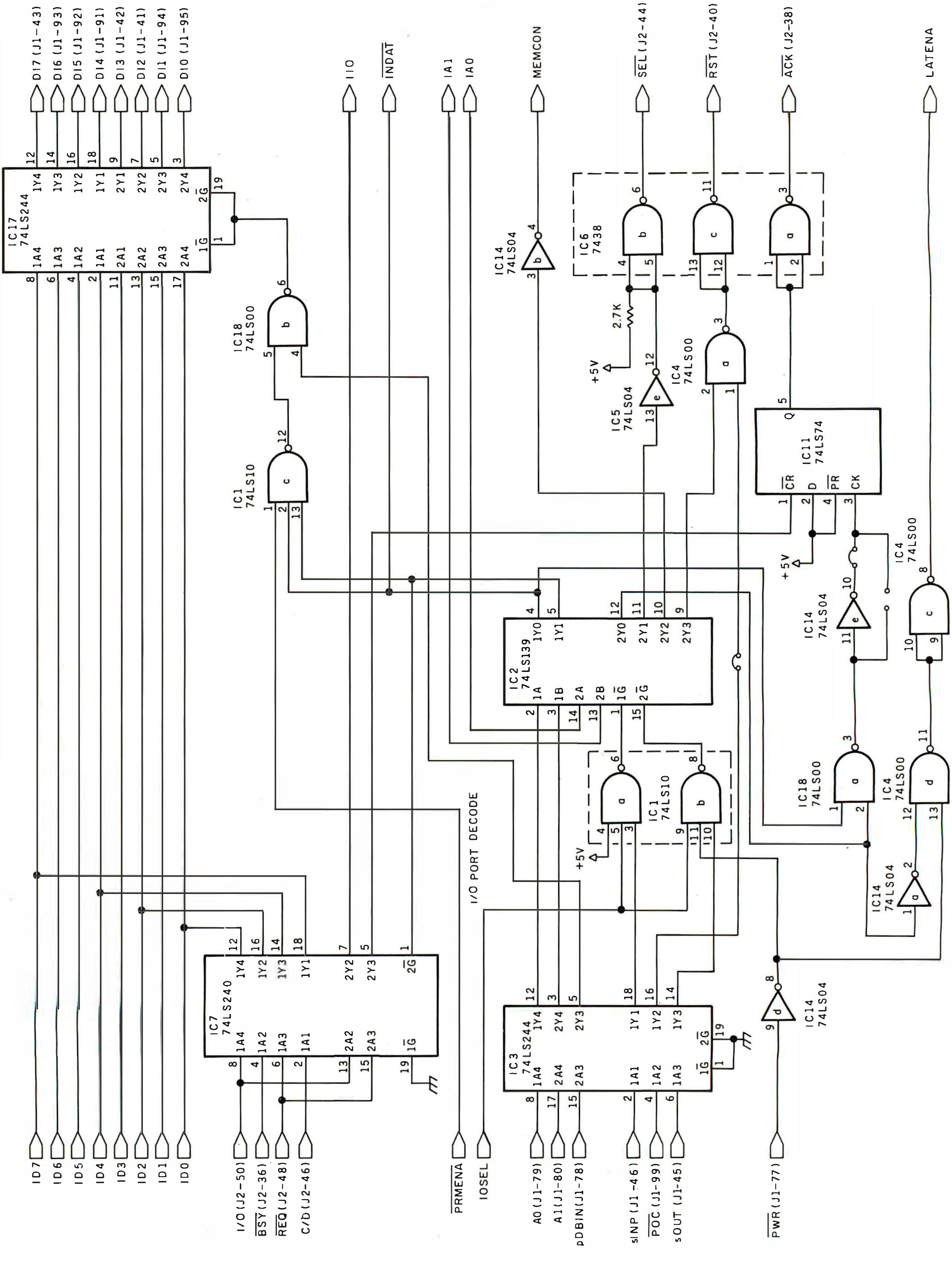


Figure 5: *Diagram of the port-decode and HCA-interface logic.*

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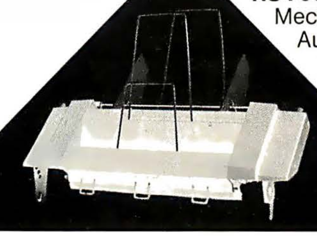
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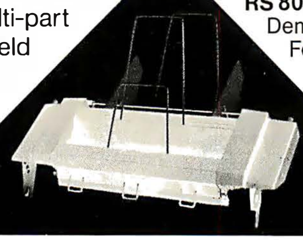
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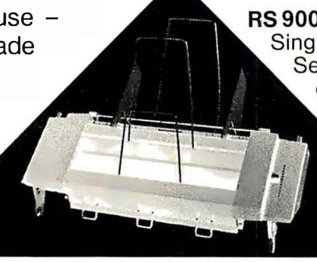
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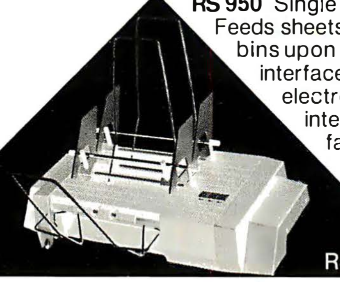
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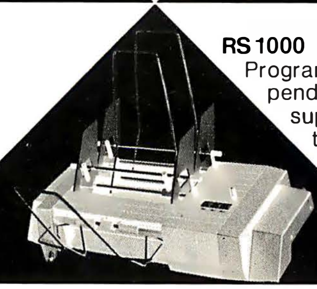
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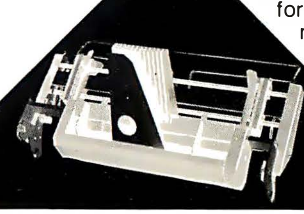
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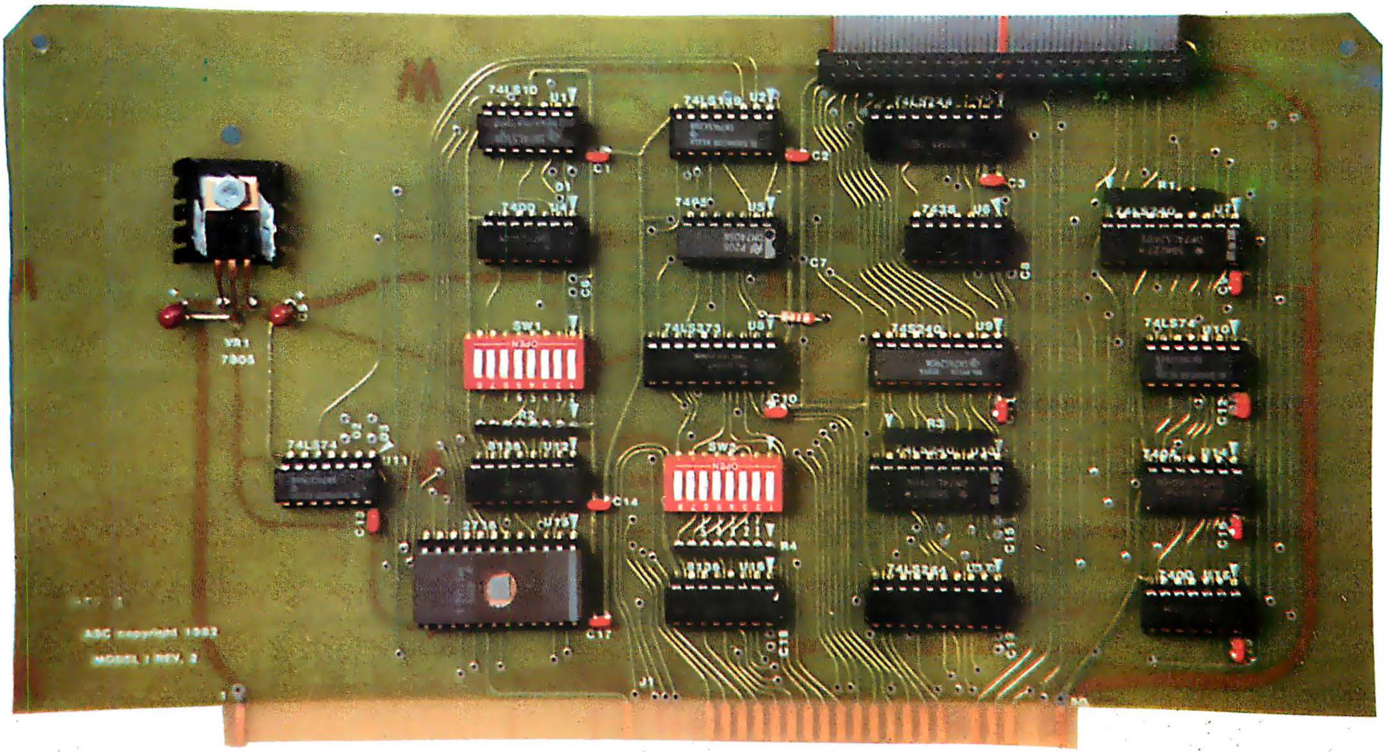


Photo 1: *The host computer adapter (HCA) printed-circuit card.*

50-conductor ribbon cable, which is the SASI standard. Photo 1 shows the printed-circuit card that results. For anyone interested in building only one of these devices, the HCA could also be implemented on a wire-wrap card instead of a printed-circuit card.

Power-Supply Characteristics

The HCA board obtains its power from the S-100 bus so the only elements of the Winchester disk subsystem that require external power are the disk drive and the controller card. Both these devices require +5 and +12 volts (V) DC. Adding up the power requirements for both devices at both voltages results in total power requirements of about 1.5 amps at +12 V and about 3.0 amps at +5 V.

Several options were available for providing this power. These included designing and constructing a power supply, buying a commercially available linear supply, or finding a commercially available switching supply. Fortunately we were able to find a commercially available switching supply that provided 2.0 amps at +12 V and 3.0 amps at +5 V. This exactly fit our power requirements. Because it was a switching supply it was small enough physically that we could include it in a small enclosure with the disk drive and controller card, and the supply was relatively efficient so that power dissipation and cooling problems in the disk enclosure would be minimized.

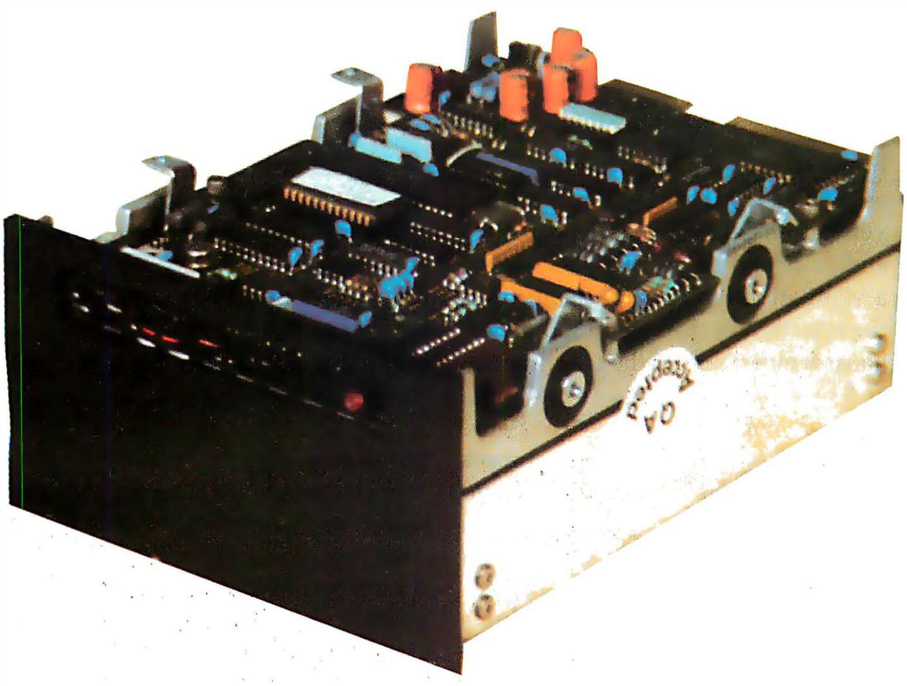


Photo 2: *The Miniscribe 5¼-inch Winchester disk assembly.*

System Packaging

Choosing the power supply completed the overall design of the Winchester disk subsystem. The only remaining step was to devise a way to package the system. This was particularly important due to the characteristics of the Winchester disk drive. Photo 2 shows the Miniscribe disk as it is delivered from the manufacturer. From this view it is apparent that the disk drive, as is true of all Winchester disk drives, is intended to be mounted

in some type of enclosure. In fact it is even more important to install this disk in an enclosure than the photo would indicate. The disk is meant to be installed using the isolation points shown in the photo to isolate the disk mechanically from the rest of the system. These isolation points absorb high-frequency shocks occurring during handling that could result in damage to the very sensitive read/write head of the drive. Thus it is imperative to install the disk in an enclosure as soon as possible and to exercise extreme care in handling the disk prior to its installation.

The controller card and the power supply we chose had dimensions that made it feasible to mount both these elements in the same enclosure as the disk drive. Photo 3 shows all these elements before assembly. We chose to mount this equipment in a box 7 inches wide, 12 inches deep, and 7¼ inches tall. In our opinion, a box this size approached the median between having a small, compact system and still providing enough free space in the enclosure for adequate ventilation.

The enclosure selected had a removable top, and photo 4 shows how these various components were mounted in the box. The disk drive was bolted to channels attached to the box. The controller card was attached to the bottom of the box using angle brackets, and the power supply was bolted directly to the bottom of the box. We constructed a cable harness to route electrical power from the power switch to the power supply and on to the disk drive and controller. Also we fabricated three ribbon cables. One of these was used to connect the HCA to the controller board and the other two were used to connect the controller board to the disk drive. Photo 4 shows the installation with all the cables in place. As the photo shows, the installation is still rather compact but has sufficient room for ventilation.

One of the last but, from a reliability standpoint, one of the most important design considerations was to allow sufficient ventilation of the assembled product to prevent excessive heat buildup. Photo 5 shows both the front and back of the assembled enclosure. We punched ventilation holes on the front of the enclosure and on the rear we included a ventilation fan to force air through the system. We then measured the exhaust temperature of the air at the fan and measured the temperature inside the box during operation to assure ourselves that there were no hot spots in the box. The fact that we found no hot spots was not surprising because all the equipment in the enclosure is designed to be convectively cooled, and the fan we chose had a volume flow rate that replaced the air in the enclosure about 40 times every minute. The end result of the entire design operation was the set of hardware shown in photo 6, a forced-air enclosure containing the disk drive, controller, and power supply; an HCA card that plugs into an S-100 backplane; and a 50-conductor ribbon cable to connect these two elements.

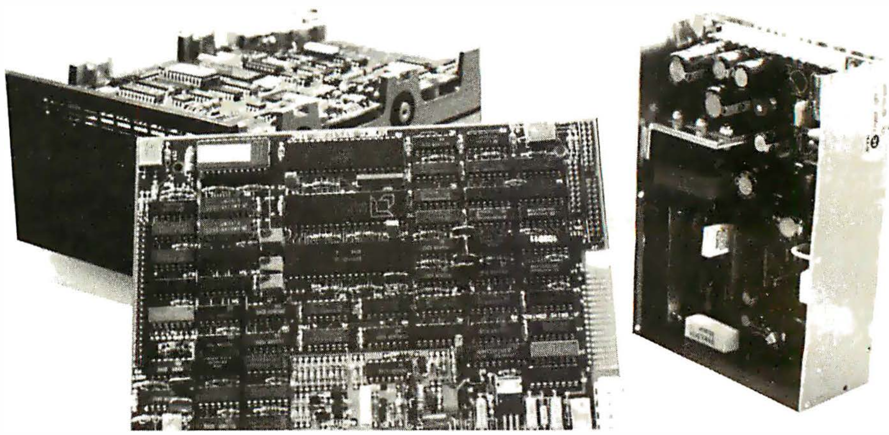


Photo 3: *The Winchester disk-drive subsystem components before assembly.*

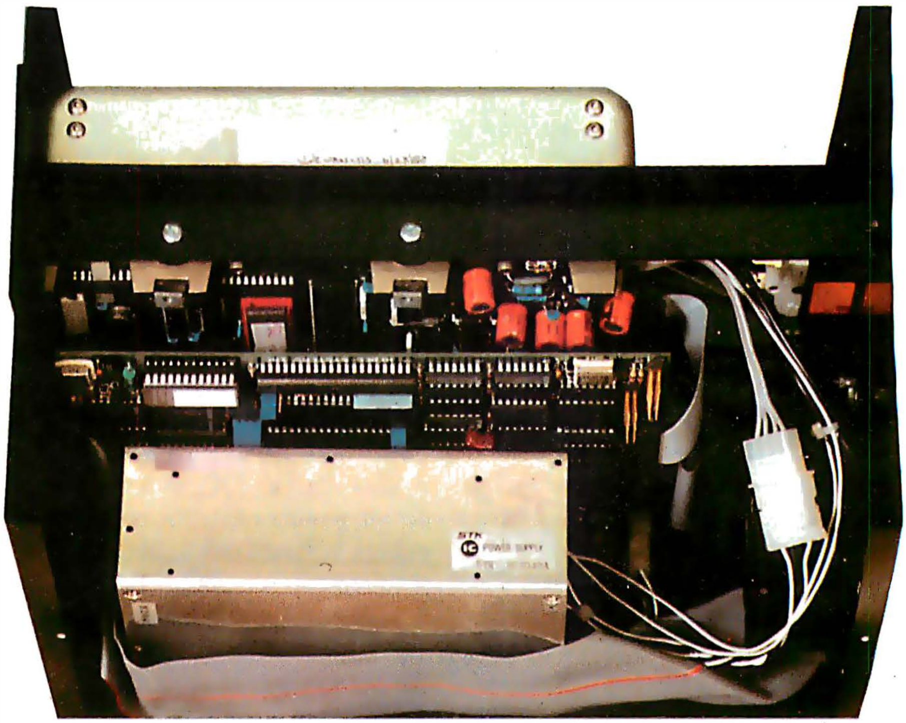


Photo 4: *The completed disk-drive assembly.*

Summary

In this article we have described the design and construction of the hardware necessary to interface a Winchester technology disk drive with an S-100 computer system. You should now have a detailed understanding of what is required to perform this type of integration, and with sufficient

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perseverance you should be able to design and construct one of these systems. Next month we will finish this series by describing the various software components that must be developed to interface the hardware with the system. Specifically, we will cover how to write a BIOS that combines the BIOS for the existing peripherals on the system with a set of BIOS routines to handle the hard disk. We will also discuss how to write a relocatable bootstrap loader for the HCA PROM and discuss some of the methodology involved in testing and debugging the various hardware interfaces in the system. ■

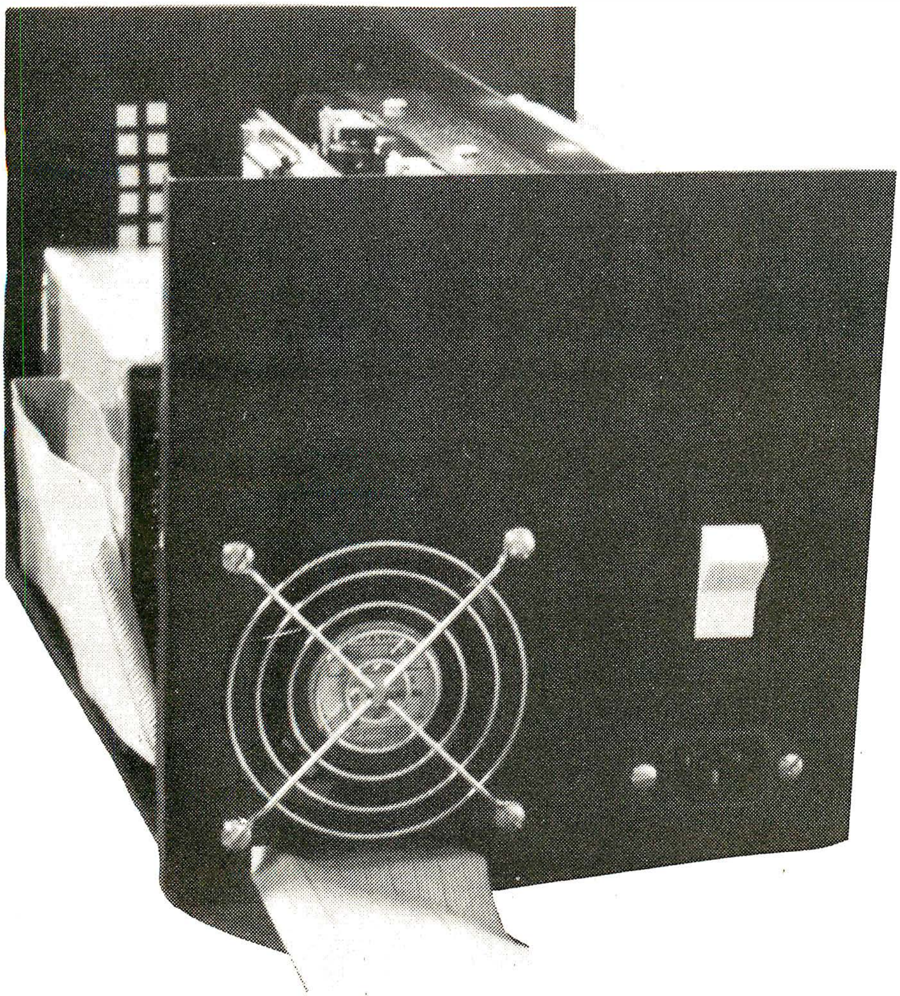
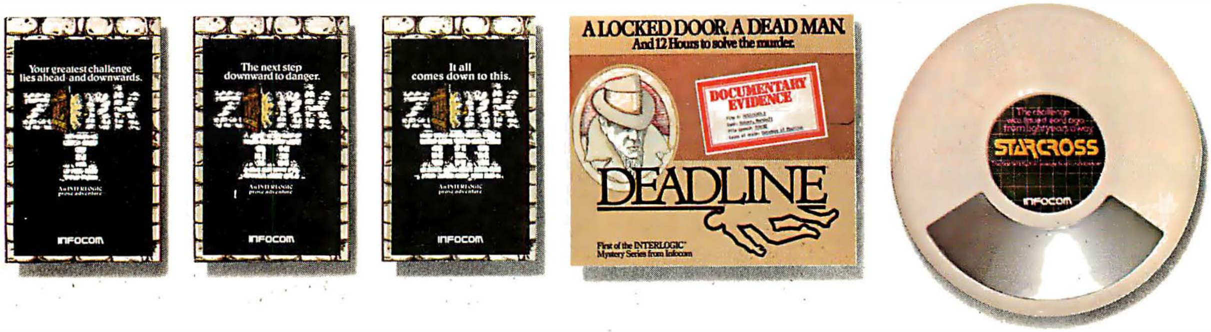


Photo 5: *Ventilation details of the disk-drive assembly.*

The Winchester disk-drive subsystem described in this series of articles is available as a completely assembled unit from ASC Associates of Lexington Park, Maryland. In addition to the S-100 version discussed, versions are also available for TRS-80 and Apple computers. The disk-drive systems for these computers use the same drive and controller hardware as the S-100 version but use a different host computer adapter and interface software. Until a nationwide dealer distribution network is established, these systems will be available by mail order for $1995. To order or obtain further information, write to ASC Associates Inc., POB 615, Lexington Park, MD 20653, or phone (301) 863-6784.



Photo 6: *The completed disk subsystem showing the drive assembly and the HCA printed-circuit card.*



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Terminal concerns for Wordstar users, BASIC comments, and a bunch of useful utilities are reviewed at Chaos Manor.

Jerry Pournelle
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My Televideo (TVI) 950 terminal holds an ambiguous position here at Chaos Manor. I rather like it in some ways. However, I haven't got around to writing a program that will make use of all its reprogrammable keys, and it has all these extra (and nonreprogrammable) "feature" keys that seemed so useful when I bought it, but which turn out to be worse than useless now that I have it. For example, not one text-editor program I know of can make use of the arrow keys. Worse, there's Back Tab.

I find I'm not alone in my distaste for the Back Tab key on the Televideo 950 terminal. It does nothing useful at all. I and many others keep hitting it instead of the Control key. For those not familiar with TVI terminals, Back Tab is just below Control and outboard of Shift, optimally placed for being hit when it shouldn't be. It produces the sequence Escape I, which, depending on what you're doing at the time, can range from annoying to disastrous.

Thus, sometimes I think I'll keep the 950, and other times I'm tempted to sell it.

My friend and sometime associate Tony Pietsch has found a way for his WRITE text editor to distinguish between an Escape sequence done by a human operator and one sent by a programmable key. I'm not sure how he does it. One way would be to use a timing test: Escape followed by some character is interpreted one way if the character comes almost immediately, as it will if it's part of a sequence sent by the terminal, and another way if there's an appreciable lag between the Escape and the following character.

However Tony does it, his installation of WRITE on the TVI converts the Back Tab key to something harmless. That's certainly one possible solution, and somewhat less drastic than what I was tempted to do, which involved removing the key entirely. Of course, it works only when using the text editor, although I suppose I could use the same sort of trick in my CBIOS (customized basic input/output system) to intercept Back Tab's Escape I and turn it into, say, a null . . .

Good News for Wordstar/TVI Addicts

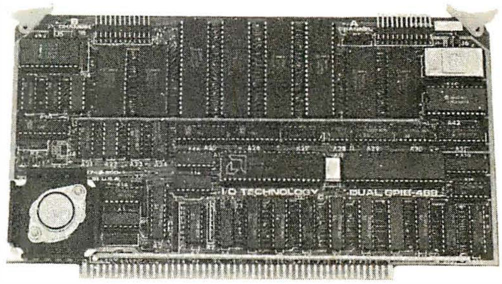
Wordstar users now have available a very elegant way to get around Back Tab, while making use of all those lovely extra feature keys that made the TVI 950 so attractive when I thought of buying it, and which turned out to be so useless once I brought it home. Wordtech Systems TV2000 Conversion will turn the TVI 950 into an excellent Wordstar terminal.

The Wordtech system consists of a new PROM (programmable read-only memory) that replaces the one that comes with the 950, a new set of key tops, and a label strip. It's easy enough to install, although getting the old PROM out and putting the new one in does involve opening up the terminal, and you'll want to be

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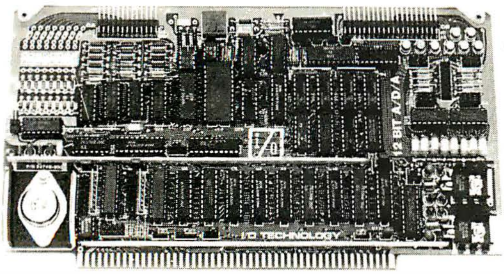
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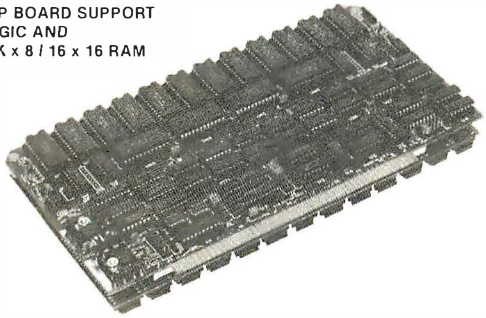


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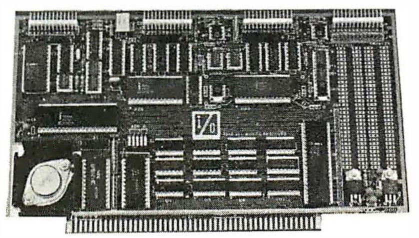


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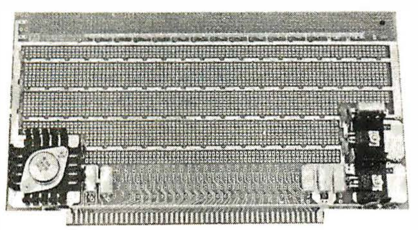
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careful in handling the chips. Once that's done, you pull off the old key tops and put in the new according to a chart provided by Wordtech.

The Wordtech changes will be invisible, and your TVI terminal won't seem to be changed until you enable it through an Escape sequence. Once that's done, all the new key tops will apply. Back Tab, for example, becomes Block Menu or Control-K. All the other keys become useful also. The Wordtech rearrangement of the keyboard is not the one I would have designed, but then I'm not a Wordstar user, and thus might easily be mistaken. One thing's for sure, the Wordtech arrangement is about a zillion times more convenient than the way the TVI keyboard comes.

You can go back to regular TVI mode any time with a different Escape sequence. The key tops have the old function names as well as the new.

The Wordtech scheme is an excellent one, and I recommend it for all Wordstar users who have the TVI 950 terminal.

I've been talking to the people at Wordtech, and they claim they can make me a new PROM for the TVI that will optimize it for WRITE and Wordmaster, which are the editors I use. I think I'll love that.

Status Line Removal

Several letters inform me that there's a simple way to get rid of the TVI 950's status line: just go Escape g Escape f Space Space Space Carriage Return. (The case is important: that is, use lowercase g and f.)

This certainly works, although I wasn't able to figure it out from the manual. I thank those who told me about it.

Manual Trades, Part One

There's good news and bad news on the document front. The good news comes from Paul Brest of Pro/Tem Software who says, "In a review of Cardfile several months ago, you quite justly criticized the documentation. The review persuaded me to rewrite the manual from scratch." He enclosed a copy of the new manual.

Cardfile is marketed by Digital Marketing, an organization whose distinctive logo shows up in a lot of places. In its own words, "Cardfile automatically stores, retrieves, and displays the sort of information typically kept in index card files—summaries of books and articles, notes, recipes, menus, catalogs of phonograph records, etc." It does this in a complex way that's made reasonably transparent to the user. In my previous review I said I was favorably impressed by the program, but quite unhappy with the manual.

That's fixed now. The new manual is very good. It tells what the program does and how to make it do that. There are plenty of examples, and it's clearly written. My only complaint is relatively trivial: unlike the previous manual, this one is not punched for storage in a 3-ring binder, and it's a little too thick for my punch, while too thin to have its name on the spine so it can be shelved by itself.

Manual Trades, Part Two

I really do like Digital Research and much of what it publishes, honest I do. That doesn't stop me from trying

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to change its documentation habits, which aren't very good.

Example. The other day I decided to put random-access files into my Minimum Data Base (MDB), which is written in CBASIC and CB-80. CBASIC pseudocompiles to an intermediate code that is then interpreted a line at a time; CB-80 compiles to true 8080 machine code. They aren't the same language, but they don't differ by much. If you're careful, programs will compile in both. CBASIC will run under CP/M 1.4; CB-80 needs 2.2 or later. MDB is a little do-all program that I use for Christmas cards, menus, and all kinds of odd jobs.

I haven't done much CB-80 file-management programming for a while, so I thought I'd read the manual as a refresher. After all, the CBASIC manual had taught me enough about random-access files to allow me to write the accounting program I use, and what I had in mind for the MDB wasn't anywhere near that complicated. Because I was going to work primarily in CB-80, I took out that manual and turned to the index.

No entry for "random access." None for "sequential" either.

I began to splutter. "Now wait a minute!" I yelled, causing my assistant, two of the boys, and the dog to come running in to see what was wrong. There *had* to be random-access files in CB-80. I *know* there are, because the POST program that takes my journals and posts them into ledgers, although written originally in CBASIC, compiles and runs fine under CB-80; and each of those ledger pages is a random-access file.

Nothing for it but to scan the table of contents, which I did. Nothing on file types at all. Best to read the whole chapter, then. In the opening paragraphs on "File Description" there is a brief discussion of "fixed" and "stream" files. It is terse to the point of uselessness.

The remaining 13 pages on files are much the same: if you can understand what's said there, you already know at least that much about the subject. If you don't know what's going on, you won't learn it from that stupid manual. Perhaps that's an overstatement, but not by much.

The old CBASIC manual, published before Digital Research bought out Gordon Eubanks and his Compiler Systems company, had more than 20 pages on files, including an excellent section called "Programming with Files" that explicitly discussed the differences between "sequential" and "random-access" files, and explained precisely how "random access" worked. Example:

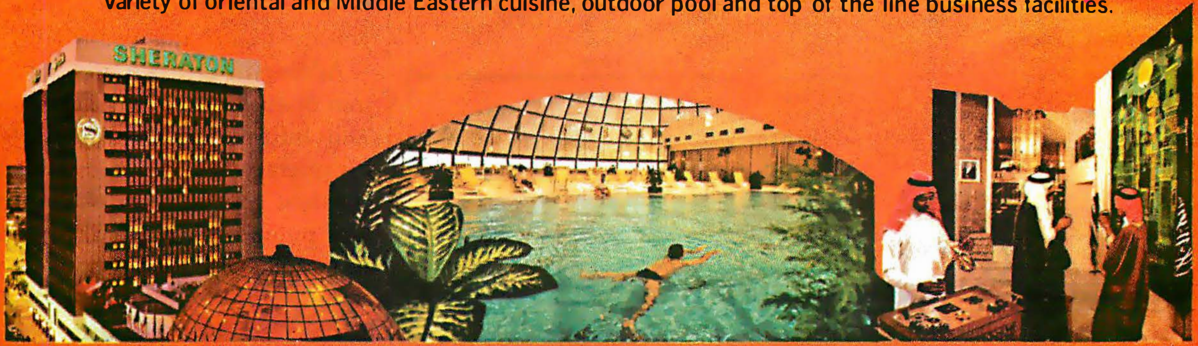
> *Randomly accessed records must use the fixed [record length] organization. CBASIC locates each record on a randomly accessed file by taking the relative record number specified in the program, subtracting one from the number, and multiplying it by the length of a record. The result is the byte displacement of the record measured from the beginning of the file. If the records were of varying length, the displacement could not be calculated in this manner.*

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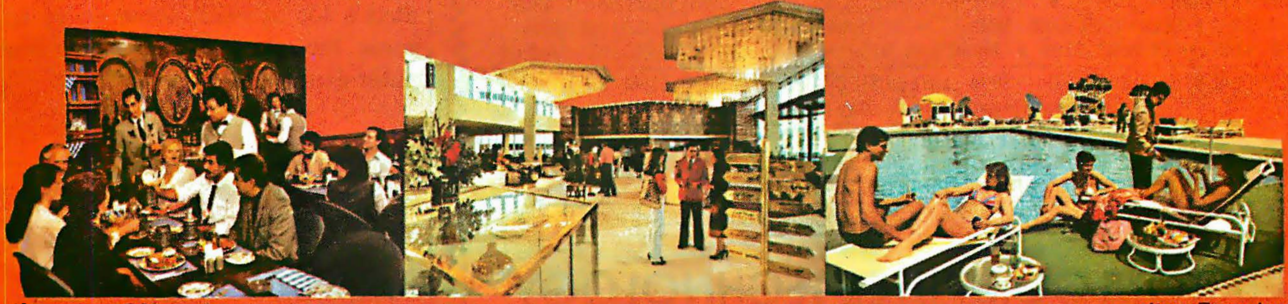
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And so forth. That's informative. The result was that way back when I began playing with small computers, I was able to create a pretty sophisticated accounting program, because the CBASIC manual told me something about the language, and said it in comprehensible terms.

None of that is in the CB-80 manual. Now true: the CB-80 manual calls itself a "Reference Manual," meaning, I suppose, that it's the user's responsibility to get his or her own primer. This is not, in my judgment, a sane marketing strategy. Whatever the relative merits of CB-80 and Pascal—and I am prepared to defend CB-80 as a real candidate for the beginner's microcomputer language of the future—there's no contest if you can't *learn* one of the languages.

Adding insult to it all, at the bottom of *every* page is the silly phrase, "All Information Presented Here is Proprietary to Digital Research." The constant repetition of this meaningless pomposity would be irritating enough if the information were more comprehensible, but given what you actually get it's doubly so.

I'd strongly advise Digital Research to generate a good beginner's manual for CB-80. The language, with features like true local variables, parameter passing, functions that can serve as true "procedures" and can be called by name, etc., is far too good to be restricted to experts. Flash: there have been reforms at Digital. More next month.

Free BASIC and PBASIC

My October 1982 column generated a lot of mail, some angry and some thoughtful, by quoting computer expert Edsger Dijkstra:

> *It is practically impossible to teach good programming to students that have had a prior exposure to BASIC; as potential programmers they are mentally mutilated beyond hope of regeneration.*

Now I don't believe that; not only can people whose first computer experience was BASIC programming

learn to write good code in other languages, but some good programs are written in BASIC itself. By a "good" program, I mean one that does something useful, is easily used, and can be updated and maintained; and I contend that Minimum Data Base and my Accounting Package both meet those criteria. (I don't say there aren't *better* programs; only that for me these are *good enough*.)

However, Dijkstra, whose paper "GOTO Seen Harmful" was one of the primary works that began the structured-code movement, has a valid point. BASIC, especially its early versions, encouraged "spaghetti" code, and many older BASIC programs expire in an impenetrable fog of GOTO statements. No one, including the original programmer, has any idea of what's going on, or why, and it's very easy to write that sort of horror in BASIC.

Several possible solutions to this problem are available. One is to give up BASIC; an idea that has many advocates among my readers. Unfortunately, there's no agreement on what to put in its place. Pascal, Logo, various assemblers, FORTRAN and RATFOR, C, PL/I, FORTH, and LISP all have their (very vocal) advocates. Moreover, a lot of people out there have BASIC and don't want it to go to waste.

Another possibility is to change BASICs. CBASIC was a start. Its compiled successor CB-80 is a more obvious candidate; indeed, CB-80 has nearly all the structured features of Pascal. However, CB-80 is expensive, and, as I noted above, the introductory manuals leave something to be desired; while CBASIC is slow. For files programming these versions have another disadvantage: not only are they slower than Microsoft's MBASIC, but their files take up considerably more disk space. That used to be more important than it is now in these days of megabyte floppies, but it can still be significant if you have a machine with limited disk capacity such as an Osborne.

Furthermore, there are a lot of advantages to using an *interpreted* language like Microsoft MBASIC. Interpreted languages make programming

simpler; you can check out your code a little at a time and trace the program operation. It's especially nice if you can then compile it to increase program operation speed, as you can with Microsoft's BASCOM. A lot of people have MBASIC; perhaps there's a way to structure programs while still using it?

Which brings us to the third possibility, given in Richard Mateosian's excellent book *Inside Basic Games*. Far from just a book on games (although it is that, and quite good, too), this book is a darned good lesson in programming technique.

Early in the book, Mateosian introduces what he calls "Free BASIC." This isn't really a language; it is what my mad friend used to call a *metalanguage description* of a program. Free BASIC uses an exact syntax and includes most of the constructs required for structured programming: IF. . .THEN. . .ELSE, DO. . .WHILE, DO. . .UNTIL, and CASE. The programs Mateosian uses as illustrations are all "top-down" structured, and in his discussions of how to program he emphasizes the techniques of top-down programming, introducing concepts such as "stubs" (dummy subroutines for checking program logic). If all BASIC programs were first written in Free BASIC before translation to regular BASIC, there would be a great deal less criticism of the BASIC language.

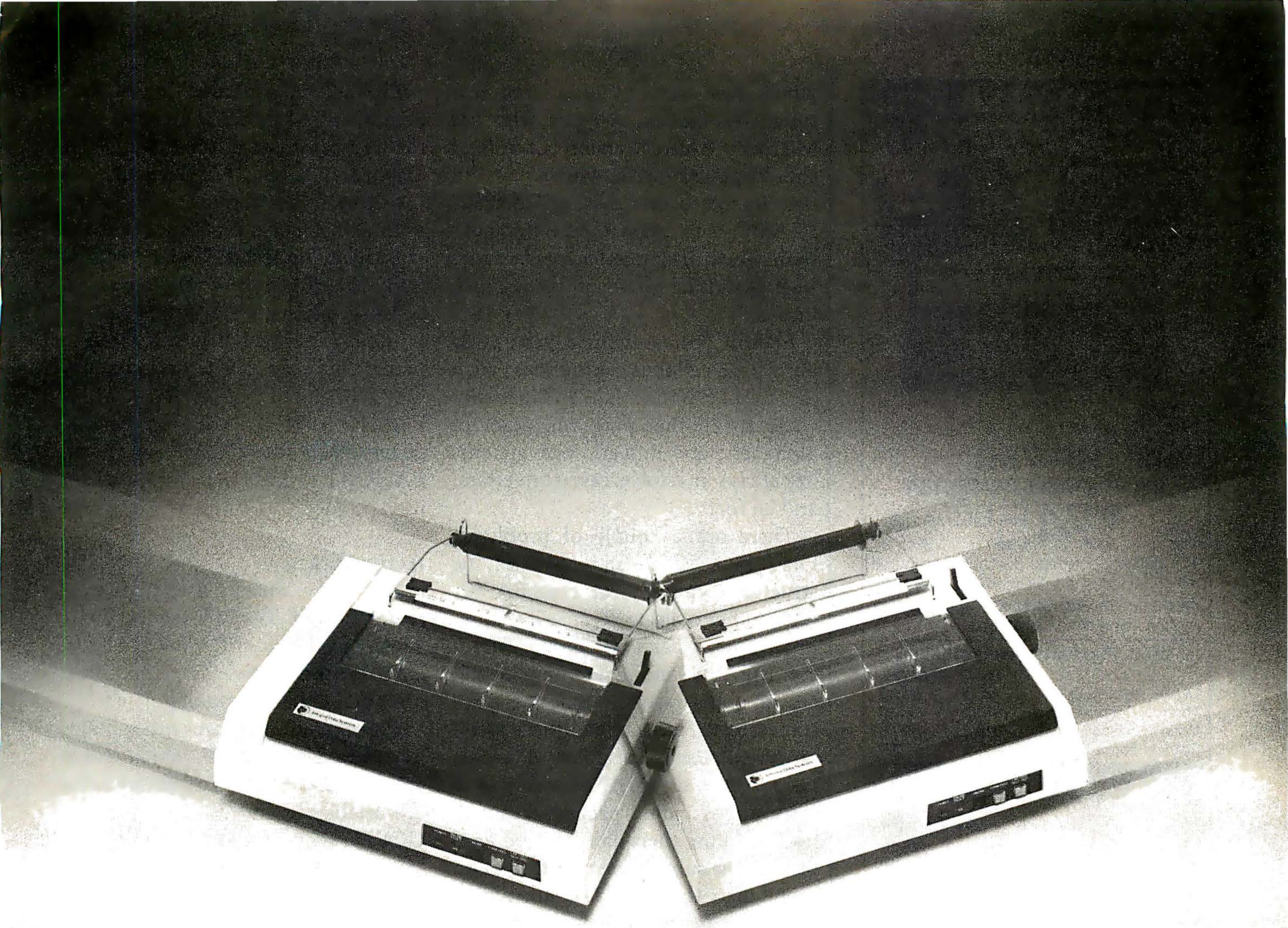
Alas, though, there is no such thing as Free BASIC; that is, unlike RATFOR, for which there is an actual preprocessor that translates top-down structured code into standard FORTRAN, there is no Free BASIC program; the "language" exists only in concept, and once you've written your program in Free BASIC you must hand-translate it into actual code. I agree with Mateosian that using Free BASIC is an excellent idea and to be recommended; but I am also certain that, like many good ideas, it's not likely to be adopted. That shouldn't stop beginning programmers from reading his book, though.

Another possibility is PBASIC. This is an actual preprocessor that takes structured code and turns it into Microsoft MBASIC.

PBASIC allows unlimited comments, "pretty printing" with indentation to increase readability, alphabetic labels for subroutines, code without line numbers, local variables and parameter passing, and the like. It also makes "chaining" programs easier: that is, programs can call other programs as subroutines. Finally, PBASIC has simplified methods for creating and maintaining a library of subroutines and including them in new programs as needed.

Bruce Tonkin, PBASIC's creator, is convinced that PBASIC is much better than both CBASIC and CB-80. He may well be right about CBASIC. PBASIC is a compiler rather than an interpreter, of course, and thus has some inherent problems; but it compiles into interpretive MBASIC, which is usually easier to debug.

I don't think I agree about CB-80,



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which has excellent structured features. No matter. Anyone who has Microsoft BASIC Version 5.2 or later should get PBASIC, whether or not they intend to get CB-80 or CBASIC. PBASIC isn't perfect, but it's more than worth its price to anyone who intends writing Microsoft BASIC programs.

PBASIC comes with a very good library of callable subroutines, such as "CALLPROG" that will actually chain to another program, a set of alphabetic and numeric conversions, uppercase and lowercase converters, and so forth.

There are a couple of problems. First, PBASIC doesn't have all the structured concepts of Free BASIC. It's another dialect. Because it's a preprocessor, it can't get inside Microsoft MBASIC and make fundamental changes; the result is that there are some costs. For example, there aren't any *real* local variables; PBASIC keeps track of variables internal to subroutines and procedures and doesn't allow their names to be used outside the subroutine, but it can't do more than that. They're still global variables, and you can have problems with nested subroutines if you're not careful.

Finally, the documentation isn't all that clear. You'd want to be pretty familiar with BASIC before tackling the PBASIC manual. It does have a good index, and there are examples; it's not *that* formidable.

PBASIC is mostly compatible with BASCOM, the Microsoft BASIC compiler. You can write PBASIC programs with any text editor that uses Carriage Return-Linefeed pairs as newline characters and doesn't set the eighth bit. (Wordstar in nondocument mode is fine; so is Wordmaster. WRITE and Electric Pencil will require a simple conversion program; a suitable converter is available along with a lot of other useful stuff on CP/M Utility Disk One from Workman and Associates.)

If you do much programming in Microsoft BASIC, I recommend that you get PBASIC. If you're just learning, I recommend that you get Mateosian's *Inside Basic Games* and read about Free BASIC, then get PBASIC.

PBASIC is available in standard 8-inch CP/M format directly from the author; it can also be obtained in Osborne, Otrona, KayComp II, and (possibly) other formats from Workman and Associates. Osborne users, with their limited disk space, should find PBASIC especially valuable, because Microsoft MBASIC packs random-access disk files into about 60 percent of the space required by CBASIC. Do understand that PBASIC is not a stand-alone language; you must have Microsoft BASIC 5.2 or later to make any use of it.

Active Trace

Another extremely useful program for Microsoft BASIC users is Active Trace, by an outfit known as The Data Works. Active Trace is distributed by Digital Marketing.

Three major programs are included in Active Trace: VREF, which makes an alphabetized cross-reference table of variables in an MBASIC program; GOREF, which makes a map of every line called by GOTO or GOSUB; and SCOPE, which runs with the program much like TRON (the built-in trace utility within MBASIC), but which outputs not only line numbers but variable values as the program runs.

These programs were written in Microsoft BASIC, but the source code is not provided. They have been compiled with Microsoft's BASCOM, and both the linked (.COM) versions and the BRUN versions (which require that you have Microsoft's BRUN run-time package, not provided with Active Trace) are included on the disk.

The documentation is good, if a bit disorganized. It contains examples, a tutorial, and a rambling essay on structured programming and program philosophy. I had no problems understanding it, but some of the students here required help. They didn't need *much* help, but the documents would be improved by testing with high school or undergraduate beginning programmers. I've got a class of Boy Scouts working on the Computer Merit Badge meeting here in a couple of weeks, and I'll try to note down

Text continued on page 338

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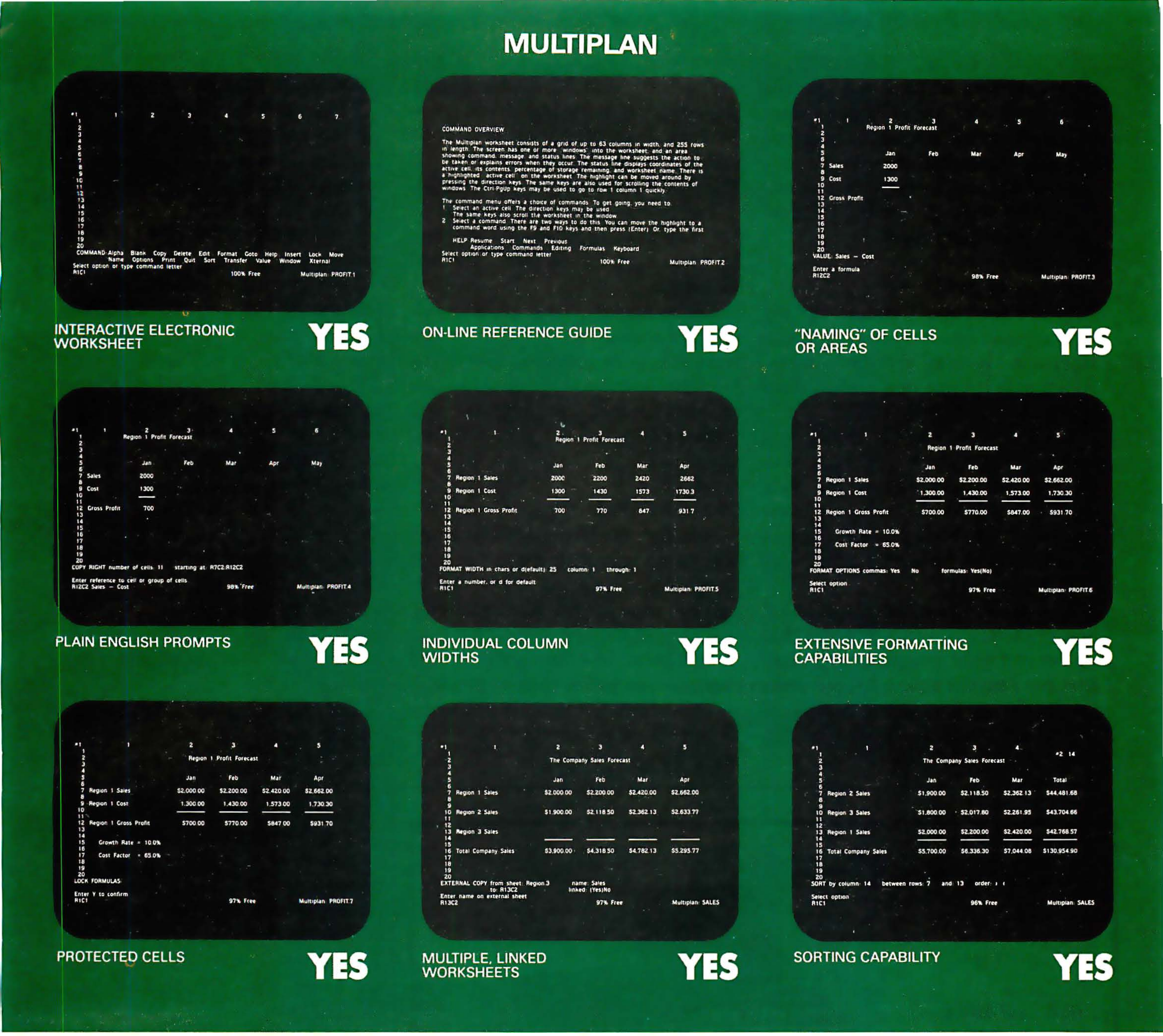
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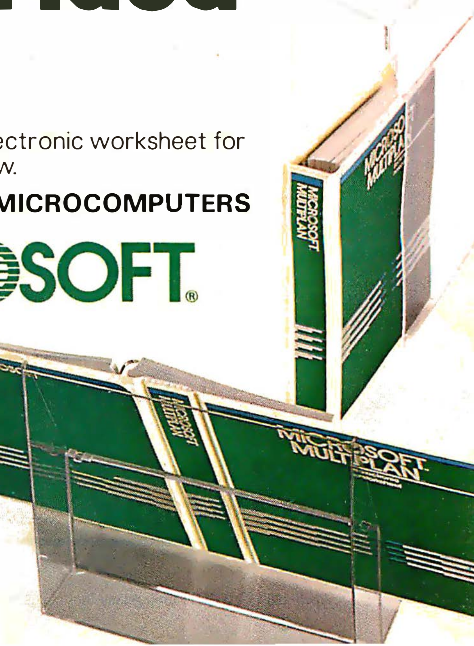
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their questions to feed back to The Data Works. However, I don't want to overstress the document problem; this was better than most I see.

Anyone doing much programming in Microsoft BASIC should appreciate Active Trace a *lot*.

Osborne Expands

Two weeks ago I packed up my Osborne and sent it off to Osborne in Hayward. It was returned today. Along with it came new system disks in double density.

What should I say? It works, and instead of 92K bytes on each disk there's now 184K bytes for data storage; not quite as much as my first computer's single-density 8-inch disks with their 242K bytes, but enough for most purposes.

A manual update explains what double density is, and it tells you that you've not only bought double density, but also the ability to read disks created by a variety of machines: Osborne 1 single density, Xerox 820 single density, Cromemco single density, and the IBM PC double density providing that it used CP/M-86 (all in 5¼-inch disks, of course). They don't mention it, but the new Osborne will also read disks created by Compupro.

There's no universal standard in 5¼-inch disks, but Osborne is doing his best to get around that. I applaud his efforts.

The manual is quite good; although comprehensible at the elementary level, it is quite complete. Everything works beautifully, and I can't imagine anyone who has an Osborne will want to be without the double-density conversion.

The New Math

Actually, not new math, but a new way to do math: the 8087. The 8087 "math chip" can do 16-bit mathematical operations like lightning; matrix-operation programs that took 10 to 20 minutes to run with the 8088 can now run in less than a minute.

There aren't many implementations of the 8087, and not much software for it; but I expect both those situations to change.

I have two boards that can make use of the 8087. One comes from Compupro and is an 8086/87 board for the S-100 bus. I don't have that running yet because I'd have to disable the 8085, and I need that dual processor.

The other 8087 comes from Jim Hudson of Hudson and Associates. Hudson sells a small "piggyback" board that plugs into my Compupro CPU-816 dual processor CPU (central processing unit) board, fitting in where the 8088 chip normally goes; the 8088 is then put into Hudson's board. (One wants to take due care not to allow static charges while messing with chips; like all complex chips, the 8087 is sensitive to static. Ground yourself and don't work on a carpet; having high humidity in the room helps, too. In my case we keep tropical fish, which humidifies things nicely . . .)

The 8087, alas, runs only at 5 MHz, meaning that if you're going to use it you have to slow the processor down somewhat; but if you have many math operations to do, the result is *well* worthwhile: on my benchmark matrix-multiplication program, using Pascal/MT+86 with the 8087 "reals" linked in, the 20 by 20 case ran at 7.8 seconds. For a 50 by 50, it ran in 1:41.2; both these times are faster than the Sage II using UCSD Pascal.

As I write this, I have seen only two software sources that support the 8087: Pascal/MT+86 from Digital Research and the C86 C compiler from Computer Innovations. I know nothing of the C compiler, but I use Pascal/MT+ routinely now. We're just getting CPM-86 running; when I do, I'll use MT+86 with the Speed Programming Package even more. Its only rival is the Sage II (which continues to operate beautifully).

I've only started using the Hudson 8087 board, and as I write this I hear from Bill Godbout that Compupro is going to be marketing Hudson's board (with a few Compupro modifications); but since Hudson's system works nicely now, and Godbout's people have a prodigious reputation for improving anything they get their

hands on, I have no difficulty in predicting that the Compupro edition will work very well.

If you have a need for fast number-crunching—and that includes financial stuff as well as scientific—the 8087 may be what you need. I don't want to be too dogmatic about that: the Sage II is also awfully fast. I'll try to get some benchmark comparisons for another column.

Note that the development of the 8087 is another instance of my motto, "Iron is expensive, but silicon is cheap"; meaning that if you have a good versatile system with capability for expansion, people will develop upgrades for you. The great thing is to be able to use all this new stuff.

Mathemagic

One thing computers are supposed to do is compute, but in my experience most microcomputers end up processing more words—and playing more games—than they do number-crunching; and indeed, most microcomputer owners also own one or more sophisticated calculators, which they use in preference to their computers when they want to do math.

Comes now Mathemagic to change all that.

Mathemagic advertises that it "transforms your microcomputer into the ultimate calculator," and while it might not go so far as *that*, still it's no bad thing. Mathemagic is a menu-driven way to put your head back in shape if you had nauseating math teaching. It's not as versatile as spreadsheet programs like Sorcim's Supercalc, but it will handle longer and more complex formulas, and it's fairly easy to use. I can think of applications in which Mathemagic would be much more useful than Supercalc (although I'd rather have Supercalc myself).

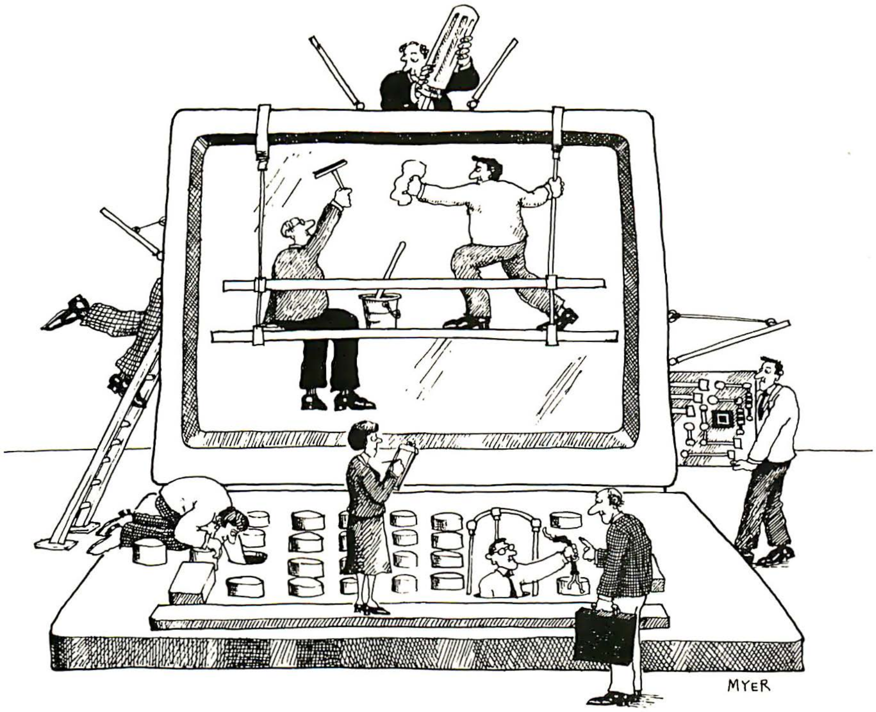
Whatever you do, though, *don't* buy Mathemagic from the publisher; go to a reputable dealer, one you trust, and get a demonstration of the program in comparison to its competition. Make up your mind *before* you put out any money. If this sounds like harsh advice, it's merited: International Software Marketing, which publishes Mathemagic, has reached new levels in "user-threatening" licensing agreements.

Not only does this company explicitly say it's going to prosecute you for any violation of its terms, but it doesn't assume *any* responsibilities whatsoever.

It says, "You assume responsibility for the selection of the program to achieve your intended results, and for the installation, use, and results obtained from the program." This means the company promises to provide *zero* support in getting it to run, and if it turns out you thought it would do something it won't do, tough luck, baby.

There's more.

The "Limited Warranty" isn't limited, it's nonexistent. It says, "The entire risk as to the quality and performance of the program is with you. Should the program prove defective, you (and not ISM or an authorized



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dealer) assume the entire cost of all necessary servicing, repair, or correction." Later it says, "ISM does not warrant that the functions contained in the program will meet your requirements or that the operation of the program will be uninterrupted or error free."

Translation: if it don't work, tough luck, baby. We may fix it, but you get to pay.

So. As I said, get a demonstration from a dealer you trust.

Footnote

I don't use Wordstar to *create* text, but it's awfully handy to have around. It's not so much Wordstar itself as the tons of support programs like Footnote that make it useful. I have no doubt that when WRITE becomes more generally available, comparable programs will be developed for that, too, but meanwhile most of the really nifty word-mashing utilities need Wordstar.

Footnote comes from Pro/Tem and is marketed by the ubiquitous Digital Marketing. Like all Digital Marketing products, it's way above average, with very complete documentation and well-tested programs. The marketing agreement is rational, too.

As you'd suspect, Footnote handles footnotes in Wordstar text files. It does what everyone wants it to, putting the notes at the bottom of the page or, alternatively, into a separate file that can be appended to the end of a document. The format is standard thesis style, suitable for term papers, dissertations, or submissions to academic journals.

Footnote is easy to use. You don't need to remember the numbers; all notes get the symbol @ when created, ↑R indicates the beginning of a block of notes, @ delimits each note within the block, and .pa ends the block. Notes can be put in anywhere you please, near the place referenced or before or after it; it makes no difference, as long as ↑R precedes the block and .pa ends it.

The program then goes through and numbers the notes, both in the text and within blocks of notes; after that it extracts the notes, reformats the text, and moves everything around so that it will print out properly. (Naturally you must give the program your text-printout format: margins, line width, line spacing and lines per page, etc.)

It does it all painlessly and simply.

Some programs are so well done that there's not much to say about them. Footnote is one of those; it's hard to think of improvements.

My copy of Footnote came bundled with a program called "Pair," which matches the underline and boldface characters for Wordstar so that you don't end up with page after page of unwanted underlined material. WRITE doesn't require that kind of checkup, but Wordstar users ought to appreciate it.

If you do scholarly writing and you use Wordstar, you'll want Footnote.

Wedged . . .

Everywhere you look there's a new spreadsheet program for sale. Spreadsheets are programs that let you enter a matrix of numbers and formulas, and recalculate the whole matrix if you change the value of any one entry. The first of these was called Visicalc, which was a really great idea, and one of the most useful programs ever developed for microcomputers.

Visicalc is one of the great success stories of the computer world, and I truly wish I'd thought of it. (I did, actually, as a sort of "I wish I had a program that would . . .", but I didn't do anything about the wish, so that counts as not thinking of it.)

Visicalc was designed for the Apple, and I'm told it was responsible for a lot of Apple sales. Naturally there was a rush to get versions running for the CP/M 8080/Z80 family of machines. One of the earliest, and best, Visicalc "workalikes" was Sorcim's Supercalc, which I've mentioned here often enough, and which I recommend.

Predictably, there's a rash of others. It's very hard to compare them feature by feature, and in general they all do the same thing anyway, so how do you tell them apart (other than by price)? One possible marketing strategy is to make distinctive product packages.

Text continued on page 346

BASIC VERSUS

A NO-HOLDS-BARRED

1 EASE-OF-USE

While Basic is easily learned, for just a little extra effort invested, Pascal pays much bigger dividends. Many universities use only Pascal to teach programming; *it's the more modern language, incorporating advanced programming techniques.* Example: by dividing programs into modules, JRT Pascal makes very complex programs—of nearly any size—a breeze to manage.

Pascal code is *self-documenting;* program sections are identified by meaningful names, not line numbers. And error messages are verbal, not number codes. JRT offers more (and more powerful) *data types: 12*—to Basic's 2 or 3. Use regular or hex numbers; JRT gives you the choice.

Total it all up, and the result is a language that's very easy to use.

Here's the real shocker!

Features	Basic	JRT Pascal
Structured programs	No	Yes
Separate compiled modules	"Chaining"	Structured procedures with auto-loading & purging
Arithmetic precision	Usually 6 or 7 digits	14 digits
Indexed files	No	Yes
Maximum string size	255 characters	64,000 characters
Loop statements	1	3
Data types	Usually 2 or 3	12
CASE statement	No	Yes
Introduced	1965	1980
Price	???	$29.95!

2 POWER

For power—the ability to write better, clearer programs, faster—Pascal is the run-away winner. The CASE statement is just one good example:

Basic

```
IF X = 5 OR X = 10 THEN\
    X = 73\
    GOTO 99
IF X = Z - 4 THEN\
    PRINT X\
    GOTO 99
PRINT "X NOT VALID"
99 REM
```

JRT Pascal

```
CASE X OF
5,10  : X : = 73;
Z- 4  : WRITE (X);
ELSE  : WRITE ('X NOT VALID');
END   ;
```

JRT simplifies programming by accomplishing complicated operations (for Basic) with one command:

Basic

```
IF A$ = "V" OR
  A$ = "W" OR
  A$ = "X" OR
  A$ = "Y" OR
  A$ = "Z" THEN...
```

JRT Pascal

```
IF A IN ['V'..'Z'] THEN...
```

Convinced?

3 FLEXIBILITY

JRT Pascal's wide variety of data types reduces programming restrictions; *the language works for you, not against you.* And Pascal data types are not all fixed in size. Add *JRT's 3 looping statements* (Basic has one), and you get programming better tailored to your specific needs. That's flexibility.

You gain flexibility, too, because programs aren't limited to one diskette. With JRT Pascal, even very large programs can be created and run, because program modules can be spread over many disks. Common modules can be used for several programs, avoiding time-consuming, expensive duplication.

Basic generally limits text strings to 255 bytes; *JRT strings go up to 64K.* You process entire documents, not just single lines.

Flexibility—it could be JRT's middle name.

4 EFFICIENCY

Whereas Basic relies on a static, inefficient memory map to allocate storage, JRT's *dynamic storage* fills every available main storage area; there's no waste.

With Basic, sub-routine modules *must* be linked together; with JRT, they can be linked—but don't have to be. Another storage efficiency.

JRT programming hours are more productive, because our more powerful commands run faster. Typically, you'll *write Pascal programs 3 to 10 times faster* than in Basic. And the programs are more reliable, easier to read, easier to use.

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- Graphing procedures
- Statistic procedures
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- 14 digit BCD FLOATING POINT arithmetic
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- More than 200 verbal error messages
- Separate compilation of auto-loading external procedures
- No limits on procedure size, nesting or recursion

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*CP/M is a Digital Research TM. A 56K CP/M system is required.

The Wedge, by Access Software Inc. of Palo Alto and marketed by Systems Plus Inc., does just that. It comes in a handsome cardboard 8-inch disk box rather than in a looseleaf binder or something similar as most do. All the documents have slick, glossy covers. I find the name unfortunate, but the package is attractive enough.

I haven't had time to do a lot with The Wedge, but it seems to work all right, and it was easy enough to install. There's a set of 8-inch flash cards, that is, slick paper sheets, each of which has a tutorial lesson on getting the spreadsheet running, setting up spreadsheets, saving them, printing them, etc. As far as the program itself goes, I didn't notice any special features not present on other spreadsheets, and the documents don't seem to claim any. It will handle numbers up to 999,999,999.99 (just shy of a billion), and as small as 0.001, and that's a greater range than many such programs have, although not outstandingly so.

The Wedge's competitive edge, then, must be the documents; and if Access Software had stayed with the style of its typeset tutorials, there'd have been a real contest, and I'd have had a lot more work to do. Alas, it was not to be. I *suspect* the manuals, 20 pages in the Installation Guide and 80 pages with index in the Applications Manual, are well written and fairly complete; but I could confirm my suspicions only at the risk of my already failing eyesight, and I'm just not willing to do that.

The outside pages, including the Table of Contents, are typeset and readable; but the body of both documents is two-column printout, probably from a Diablo. It is not right justified. It was printed with either a bad ribbon or a misaligned print head (or most likely both), then photoreduced. In a strong light I can read them, though not easily, and as I said, I think they're well written. However, I'm never going to find out, and everyone else here declines to do so, so I guess we just won't have a test of The Wedge against Supercalc.

I can't imagine why, having spent what Access Software did on the rest of the package, it didn't get a good dark typescript to work from; after all, amateur science-fiction magazines ("fanzines") manage it. This company didn't, though, and thus wedged itself out of my being able to give it a fair evaluation. Those with much patience and stronger eyesight than mine might find this product interesting.

Superfile

I swear it: something has *got* to be done about silly licensing agreements before we all become a complete nation of scofflaw computer users.

Let's look at the good part first.

Authors have problems: we have to keep track of characters. For short stories that's not so difficult, but with epic-sized books like *Lucifer's Hammer* or our new *Footfall* things can get messy. We may think we're done with a character in chapter one—say the aged uncle of the waitress in the restaurant where the main characters meet—and then later discover he's just ideal for a walk-on in chapter nine; except that we don't remember precisely where he appeared, or what we named him, and we sure don't want to stop and look it up.

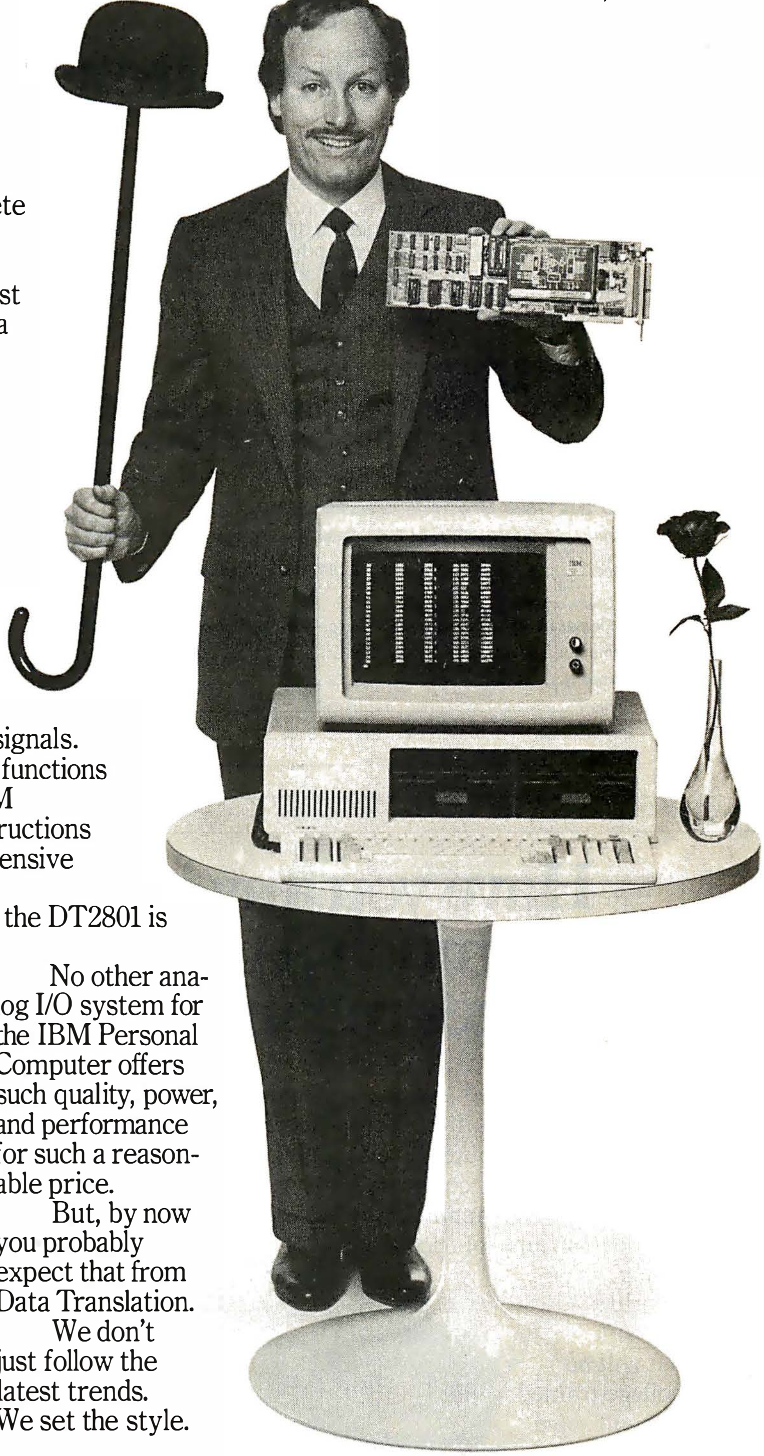
Consequently, for some time I've had in my "Do It" book a note to make up a table of characters for *Footfall*, our novel in progress. I haven't got around to it, though, mostly due to sloth. I expected to do it in my own Minimum Data Base that allows search by keywords and is easy to set up; easy or not, however, it involves work. I'd have to have a paper copy of the book to read while entering the names and data, or else have two machines going side by side, one displaying text, the other taking data entries.

Then, suddenly, there was Superfile, which appeared out of the blue courtesy of UPS. (Turns out Alex had spoken with the company while I was in Italy.)

Superfile has some very nice features. It requires no fixed length for fields, you can mix entry lengths, and you use your own text editor to create

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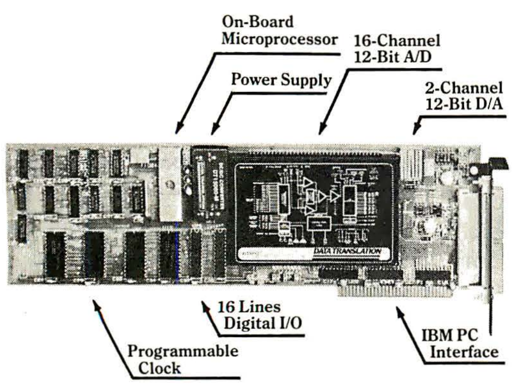
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index files. When it's all done, it makes a "dictionary" of keywords used, and you can search using up to 64 keywords combined with AND, OR, and NOT.

The search algorithm used has some problems: although it uppercases both keyword and search entry (there is an override if you really want to differentiate between uppercase and lowercase), it doesn't use an "include" comparison; the result is that BYTES won't be found if you search for BYTE. I think this is unfortunate, but you can live with it.

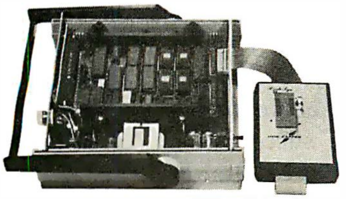
There are problems with the Sort feature, too. Superfile thinks all numbers are strings; at least that's my guess as to what's going on. What's certain is that "numbers used for sorting must all be the same length and format. If you use numbers 1 through 999, for example, all one- and two-digit numbers must have leading zero's (0) as 'pads,' like this: 001, 002 . . ."

Problems always exist with any "free-form" data-retrieval system; because the data is not in any fixed format, it's hard for a Sort routine to find the "field" on which you want to sort. The advantage, of course, is that you don't have to enter data in fixed format and in response to prompts.

My intention with Superfile is to go through and, using my normal text editor, "mark up" a copy of *Footfall*. Superfile thinks that *C begins a data entry, *K begins the keyword field for that entry, / separates keywords, and *E ends the entry. Thus, I should be able to create a characters database right from the marked copy of the text. This isn't an *indexing* program, so it won't know what page it found the entry on, but that isn't fatal; the great thing is that it ought to pull all that stuff out. If I make the character name the first entry after the *C, according to the documents Superfile will be able to sort the newly created database, giving me an alphabetic list of my characters along with whatever comments I decide to include between the character name and the *K; plus a bunch of keywords, such as the names of people they're associated with, so that I can find them again.

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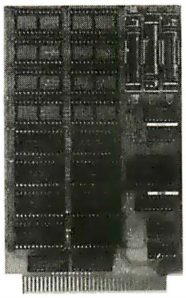
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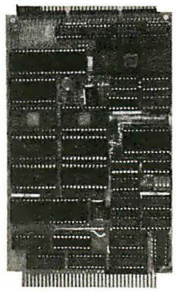
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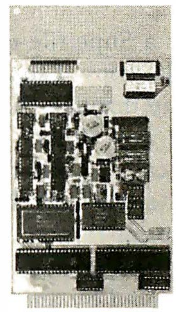
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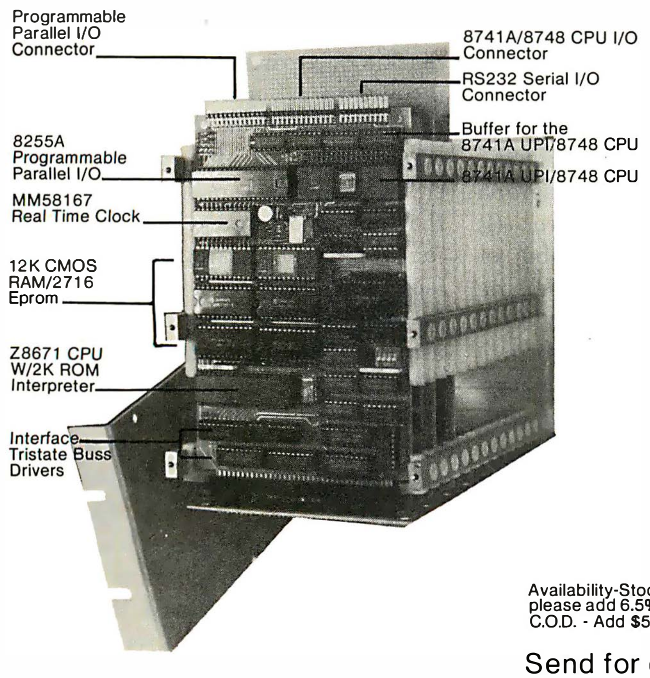
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Superfile runs only on a Z80 (I tried it with the 8085/8088 Compupro dual-processor system, and it won't run on that), but I have Zeke II running fine, so that's no difficulty.

There is a problem. The program documents give no examples at all. They write instructions in what's very nearly baby talk, but they don't show what's going on. Let me give an example.

There's a Superfile utility that will open a file, copy it to a new file, and on the way through change any characters to any others. This kind of utility is called a filter, and it's very useful for doing such things as changing the print-format commands so that text files created by one editor can be printed by another.

Superfile is all menu driven. To run this utility, you specify the "change characters" option in the utilities program. I now give you Superfile's instructions exactly as they appear in the book:

> Enter the present characters first, then the replacement characters
> present >
>
> change to >
>
> At this point you simply list the characters that you want changed, and then what you want them changed to.

That's it. No more instructions. One problem: how does it know when you're finished listing characters you want changed, and ready to accept the ones you want them changed to? On trying it, I find that you simply list what you want it to look for, end the list with a Carriage Return, and begin a new list; the program lines them up for you, old above new, so it's relatively easy to do; but it sure would have been a lot simpler to figure out if they'd given an example.

Please. Any of you out there writing programs and contemplating sales: Do not assume that your deathless prose is so sparklingly clear that you can dispense with examples. Paper isn't that expensive.

Incidentally, the Superfile utility will let you enter characters by ASCII (American National Standard Code for Information Interchange) number, so that you can change all the Control-Qs to Control-As or any such. Alas, there doesn't seem to be a way to create or remove eighth-bit-set characters (which appear as reverse video on my system) as created by Wordstar. For reasons I don't understand, Superfile will accept numbers greater than 128 (the ASCII representation of a character with the eighth bit set), but what it does with them is simply not predictable.

Still in all, let's try it. I'll go do that now.

* * *

The asterisks indicate passage of time. They also indicate mild gnashing of teeth. Superfile has its good

Superfile has its good points, but there are some infuriating aspects to it as well.

points, but there are some infuriating aspects to it as well.

First, like many programs nowadays, Superfile wants your text editor to mark the ends of lines with not only Carriage Return, but Linefeed. This is annoying. To save space on files, WRITE (like Electric Pencil before it) marks paragraph ends with a Carriage Return. (It doesn't mark line ends at all, but of course when you're using something like Superfile you'll make each line a separate paragraph; no problem.) Thus, I have to run my stuff through a filter before Superfile will deal with it—and Superfile's "change characters" utility will *not* deal with that problem, because it won't substitute two characters for one. Grrr.

Second, Superfile doesn't extract stuff from your old document; what it does is make a mess of pointers to where in your document each entry can be found. Then it renames it. Thus, I started with a chapter called DISCOVERY.TXT and went through marking it up: whenever I found a character, I put a *C at the beginning of a line, then the character name, then notes that were often just pulled from the text itself; then *K and a bunch of keywords, then *E to show that entry was done. It wasn't onerous. I didn't bother to eliminate the text between entries.

To be safe, I saved that as DISCHAR.TXT, put it into the B drive, and invoked Superfile. After some frustration with the instructions—they *will* not give examples and just assume that all is very clear—we succeeded in "creating a database" called FOOTCHARS (meaning characters in *Footfall*, the title of the novel).

Examining the disk shows there are new files: FOOTCHARS.NDX and FOOTCHARS.DIC, as well as a file called DISCHAR.D00, which is nothing more than DISCHAR.TXT with a new extension name. Four entries were crammed in among one whole lot of useless text. No extraction had been done at all. I'd obviously had the wrong idea about what Superfile does—yet I'd spent some time reading the documents.

Close rereading discloses that if I want to add anything to my "database," it will append the new files onto the old one; it still won't extract.

This means that my scheme of marking up existing stuff and extracting it into a Superfile isn't going to work; I'll have to eliminate the extraneous matter. It will be simple enough to write a small filter program that does that, and while it's at that job it can put Carriage Return-Linefeed pairs wherever it sees a Carriage Return; whether that's easier than using my Minimum Data Base (which *will* find included strings and thus would find BYTES if you searched for BYTE) is another matter.

Thus, after a couple of hours' work I was able to figure out what Superfile is and does. Understand, it's not all that hard to *use* the program, because it's all menu driven and the documents are pretty good at walking you through a lot of it; but I, at least, had my problems figuring out what it was going to do until it did it.

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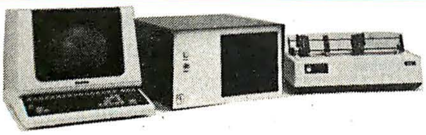
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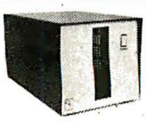
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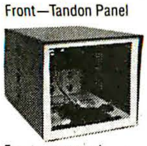
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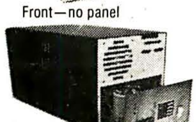
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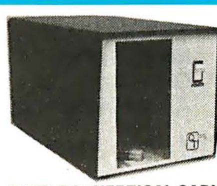
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like. You begin each entry with a *C. If you want to make mailing labels, you can make the first entry a name, last name first for sorting. This still isn't clear to me because there's no entry for "mailing labels" in the index, and the various references to making labels didn't tell me much; I presume that if I read the whole document I'd find out.

You can put anything you like, in any format you like, in the entry. This free format severely limits the ways Superfile can sort your data; the simplest is by the first words after the *C. There appear to be ways to do "numeric" sorting as an alternative, but that isn't clear, and the sort algorithm insists that the numbers be padded with leading 0s.

Lines in the entries must be separated by Carriage Return-Linefeed pairs; anything else will prohibit you from displaying any filed data, making the whole exercise futile. Superfile will *not* add Linefeeds, although it does have some limited filter capabilities.

At the end of the data part of the entry you put a *K, followed by keywords. Keywords must be separated by the "/" character; since there can be spaces in keywords (i.e., Superfile can use keyword *phrases*), this is reasonable, but of course that means that spaces are significant characters; BYTE NOW and BYTE NOW are different. Furthermore, Superfile looks for the *exact* keyword, and there is no provision for searching for *inclusions*.

Superfile takes the whole text file you've just created, renames it, and makes up an index; it also makes a sorted dictionary of keywords. This is done automatically and painlessly and is one of the best features of the program. The text file you've created becomes your "database." You can mark up existing files and add them to the database; however, extraneous matter not part of any entry will remain in the database, taking up space and presumably adding to the access-time requirements. I don't know what happens if you try to sort a database containing extraneous matter.

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confident that you'll like it that it will let you have it for a 30-day trial; if at the end of the time you don't want it, you can return all the materials plus a certificate swearing that you've kept no copies, and FYI will refund your money.

Superfile seems to work, and I expect it's easy enough to learn. The cascade menu system is nearly foolproof—I deliberately tried to crash the system by typing Control-C at various places and I couldn't do it—and the various prompts and error messages make sense, or at least do so with increasing experience. There are some annoying aspects, but on the whole this is a pretty good program. It's a lot faster than dBASE II, but of course it's also a lot less versatile.

I'd recommend it, especially with that money-back guarantee and trial period—except that FYI has devised another user-threatening agreement. This thing is in tiny print; I need a strong light and the glass from my transistorized *Oxford English Dictionary* to read it, and even then I have trouble.

The agreement is in legalese. It begins with the word *Whereas*, goes on to *witnesseth*, and ends with a signature block so damned small that I couldn't get my real name in there if I were foolish enough to sign the silly thing. If you're planning to sign as J. Doe you can just about do it, and maybe that's no bad plan unless your name really is J. Doe.

I don't know what FYI warrants; the print's too small to read. I see in the last line it disclaims any responsibility for letting you assume this product was useful or merchantable or fit for any particular purpose.

In another place there's a provision to be sure the lawyers are paid no matter what else happens. I wonder why that doesn't surprise me?

In theory you can't get Superfile without signing this thing, which is actually in the form of an application; the last line says "Upon receipt of two (2) properly completed and signed copies of this Agreement, along with the appropriate Order Form(s) and Fee payment, FYI or its authorized Dealer will return one copy of this Agreement to End User [I think that means customer] along with the appropriate FYI product materials."

Now that I look at it, I've apparently locked myself out of ever being able to be an authorized user: that is, I sure haven't signed this stupid agreement; but one of its provisions is that any use of FYI products without having signed this is unlawful and subjects me to all kinds of horrible penalties, liability for which I acknowledge by signing the agreement . . .

If you can put up with a company that lets its lawyers run wild like that, and you're willing to sign a licensing agreement that you can't read and hasn't room for a signature anyway, you might like Superfile, although I suggest you examine Cardfile first to see if it would do; Superfile has a number of features Cardfile lacks, but it costs a lot more, too.

I may yet use it, if I get around to writing the filter programs it would need before it could solve my problems. ■

Jerry Pournelle welcomes readers' comments and opinions. Send a self-addressed stamped envelope to Jerry Pournelle, c/o BYTE Publications Inc., POB 372, Hancock, NH 03449. Please put your address on the letter as well as on the envelope. Due to the high volume of letters, Jerry cannot guarantee a personal reply.

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Text box continued on page 356

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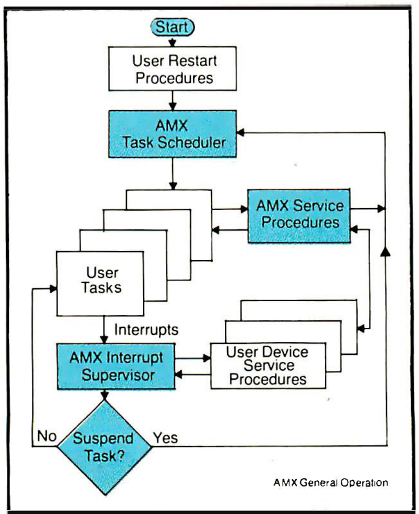
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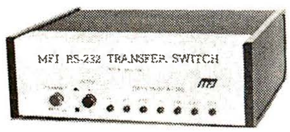
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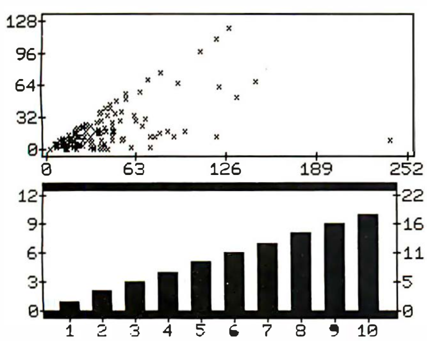
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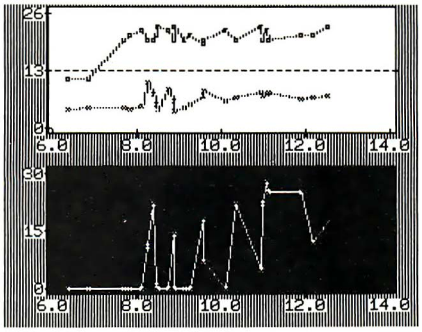
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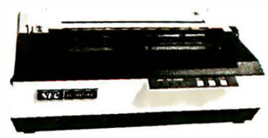
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Build this Memory, Part 2

Constructing the Memory Card

Cameron Spitzer
175 Calvert Dr., R105
Cupertino, CA 95014

This month I will continue development of the 64K-byte memory board (see part 1 in the March 1983 BYTE, page 310) by describing the construction procedure I followed (skipping the errors I made). You should follow the "test-as-you-go" procedure to reduce the bug hunt to a small portion of the board at a time.

You can build this memory board if you can solder cleanly and wire-wrap consistently. As I mentioned last month, careful construction of the circuit will result in a dependable, versatile memory that you can fill with software and enjoy for years. If you rush the job or buy untested parts, you could have a stimulating puzzle to tinker with or worse. Wiring problems (errors, poor wrapping, loose metal floating around, cold solder joints) have been known to blow the lids off ceramic integrated-circuit (IC) packages. Building this memory card should not be attempted as a first project.

All caption numbers are continued in sequence from part 1, March 1983 BYTE, page 310.

The parts are all widely available, except for the crystal. The circuit seems to work with any clock from 4 to 15 MHz, but wait states are necessary below 14 MHz when using a 4-MHz Z80 microprocessor. The crystal is not critical, but I advise you to stay between 13 and 14.5 MHz, especially if you can't measure the frequency it runs at. Crystals love to run at impossible harmonics. The prototype board seemed to have trouble holding data until I forced its 10.17-MHz crystal to stop oscillating at 20.34 MHz.

For a happy ending, don't rush the job and don't buy untested parts.

Incidentally, if you can't get a 74S65, use a 7422 and a 7403 with all their outputs tied together. You may substitute regular TTL (transistor-transistor logic) for the S-type Schottky TTL (labeled 74SXX), but you may get a wait state in some op-code fetches. If you buy a spare set of ICs, a wiring disaster can't cost too much time (table 4 is a parts list). The heat sinks I used were made from ¾-inch aluminum angle stock: a 1-inch length for the −5-volt (V) regulator, and a 3-inch length for both positive regulators. (The −5-V regulator barely gets warm; the others get hot, but not dangerously so.)

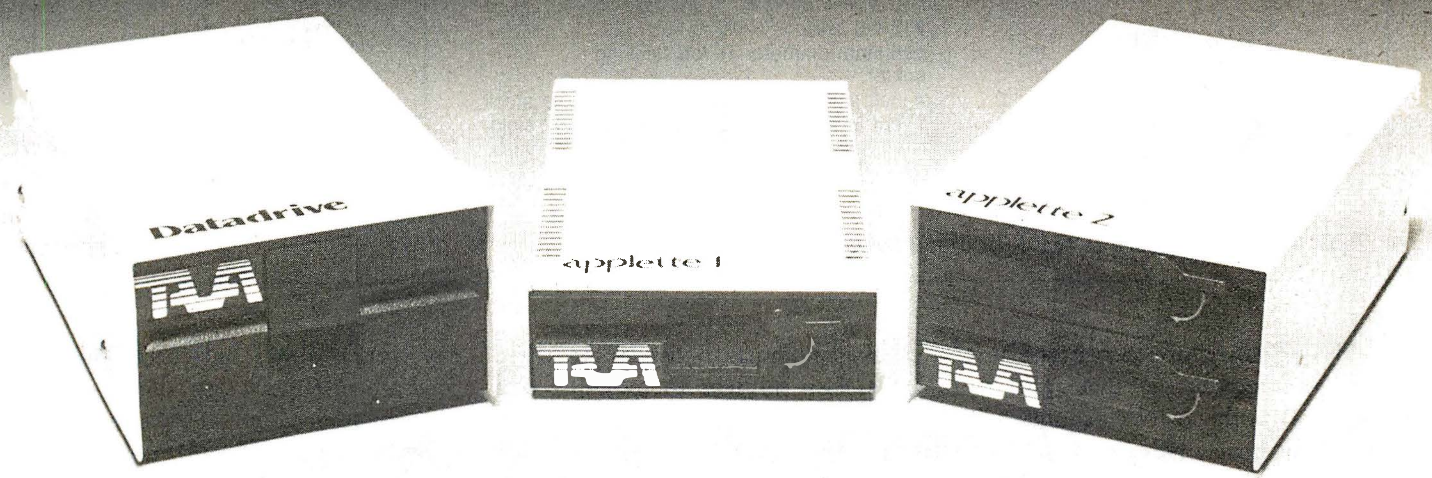
Mark locations and edge-pin numbers before installing anything. Use the layout in figure 6 to minimize bus-line length. Leave one row of holes between the memory ICs and two or three holes between rows of TTL: this leaves space for later additions.

Build the power supply first. Wire the regulators so that you can change them for debugging or for future 5-V-only memory devices. The supply fits in a 1- by 5-inch strip at the end of the board, out of the way. Test the supplies with a pair of number 47 pilot lights and a voltmeter. Two bulbs in series, across +12 V and ground, glow white, and in parallel each 5-V regulator can light both

About the Author
Cameron Spitzer designs I/O channels for Four-Phase Systems, a Motorola subsidiary.

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Circle 341 on inquiry card.

Item	Designation	Quantity	Description	You May Substitute
1	Board	1	Vector 8801-1 bare S-100 plugboard	10- by 5-inch perforated board
2	RAMS	32	MK 4116-3 16K-bit dynamic RAM	(See table 1, March BYTE, page 311)
3	XTAL	1	14.5-MHz quartz crystal	4 to 14.5 MHz (see text)
4	7805	1	5-V, 1-A positive voltage regulator (TO-220)	LM340T–5.0
5	7905	1	5-V, 1-A negative voltage regulator	LM320T–5.0, 79M05, 79L05
6	7812	1	12-V, 1-A positive voltage regulator	LM340T–12
7		2	22-μF, 25-V electrolytic capacitor	4.7 μF tantalum
8		1	47-μF, 25-V electrolytic capacitor	22 μF tantalum
9	Caps	40	0.1-μF, 15-V ceramic capacitor	
10		1	150-pF ceramic capacitor	
11		2	33-pF ceramic capacitor	
12	Diodes	5	1N4001 50-V, 1-A silicon diode	1N4002, etc. Do not use 1N914
13	U9,U12	2	74S00 quad NAND gate	74LS00
14	U2	1	74LS00	7400
15	U15	1	74S04 hex inverter	*
16	U1	1	74S10 triple NAND gate	*
17	U36	1	74LS30 NAND gate	Any 74LSxx (see text)
18	U21	1	74S65 AND-OR-INVERT	7465, 7403, and 7422 (see text)
19	U3,U10	2	74S74 dual D-type flip-flop	74LS74
20	U13,U27	2	74LS74 dual D-type flip-flop	7474A
21	U20	1	74LS139 dual 1-to-4 decoder	*
22	U33	1	74LS151 1 of 8 multiplexers	74151
23	U4	1	74S175 4-bit D-type flip-flop with clear	*
24	U26	1	74LS240 octal line receiver	*
25	U19,U24	2	74LS373 octal D-type latch	25LS373 (74LS240, U19 only)
26	U17,U18,U25	3	74LS374 octal edge-triggered flip-flop	25LS374
27	U6,U11	2	74LS393 dual 4-bit counter	4x 74LS293, etc. Binary only
28	RP1	1	1 kΩ × 13 14-pin resistor DIP	
29	RP2	1	4.7 kΩ × 13 14-pin resistor DIP	
30		1	2 kΩ } ¼-watt 5-percent resistors	
31		3	470Ω } ¼-watt 5-percent resistors	
32		14	33Ω } ¼-watt 5-percent resistors	
33		1	1 kΩ } ¼-watt 5-percent resistors	
34		6	20-pin } wire-wrap sockets	
35		37	16-pin } wire-wrap sockets	
36		17	14-pin } wire-wrap sockets	
37		75	loose wire-wrap pins	
38			#30 wire-wrap wire	
39			#18 bell wire	
40			#18 inner-diameter Teflon sleeving	
41			solder	
42		2	4-inch length of ¾-inch aluminum angle stock cut into 1- and 3-inch pieces (for heat sink)	

Cost Breakdown

32	RAMs	$55
60	sockets	30
	board	20
	ICs	20
	spare ICs	20
	crystal	5
	odds and ends	5
		$155

* Indicates "do *not* substitute"

Table 4: *Parts necessary to build the 4116-type memory.*

bulbs yellow. Do not proceed until the power supplies are just right. You may bolt both positive regulators to the same heat sink, but be sure to isolate the case of the 7905, because it is at −5 V.

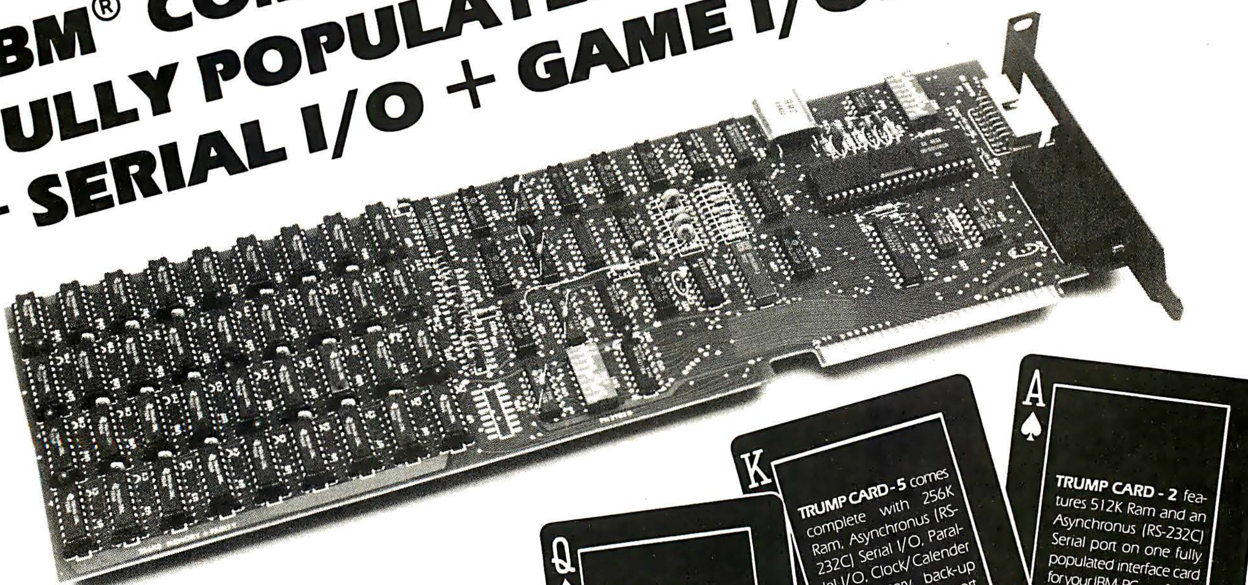
Next, mount the memory sockets, as shown in figure 6, by soldering AWG18 wire to all pins 16 (ground) in a grid. I formed the wire into a zigzag and slid bits of Teflon tubing down it. Then I could solder in a whole row at one time. Each pin 16 is connected to the next, horizontally and vertically, to form a low-impedance ground plane. Repeat the grid process on pins 1 and 8 separately. Use a buzzer or ohmmeter to check for shorts between the three grids. Use sunlight to look for bad (rough, dull) solder joints. Remove bad solder, don't just reheat it.

The TTL-supply wiring is less critical. I supplied power to the TTL sockets by wiring a few wrap posts up with AWG18 copper wire, then connecting these to the sockets with AWG30 wire-wrap wire. The +5-V supply is wired as an address line, using a grid pattern. Again, check for shorts.

Copy the schematic diagram twice. Wire the address and data lines among the memory devices as shown in figure 4 (see part 1 in March 1983 BYTE, page 320). Notice how the array works: almost all corresponding pins are just tied in parallel (i.e., all the pins 15 are hooked together). The exceptions are $\overline{RAS0}$ through $\overline{RAS3}$, and the data pins 2, 4, and 14. Each $\overline{RAS}$ line runs across a bank of eight devices. Each data line (16 of them, in all) ties four pins together vertically. Do not tie together any pins with different numbers. On the first schematic copy, color each line you complete. Wire the TTL and resistors point to point, minimizing each line length (neat bundles of wire-wrap wire will just cause noise trouble). Do not connect the circuit to its regulators yet.

The clock is wired by soldering the

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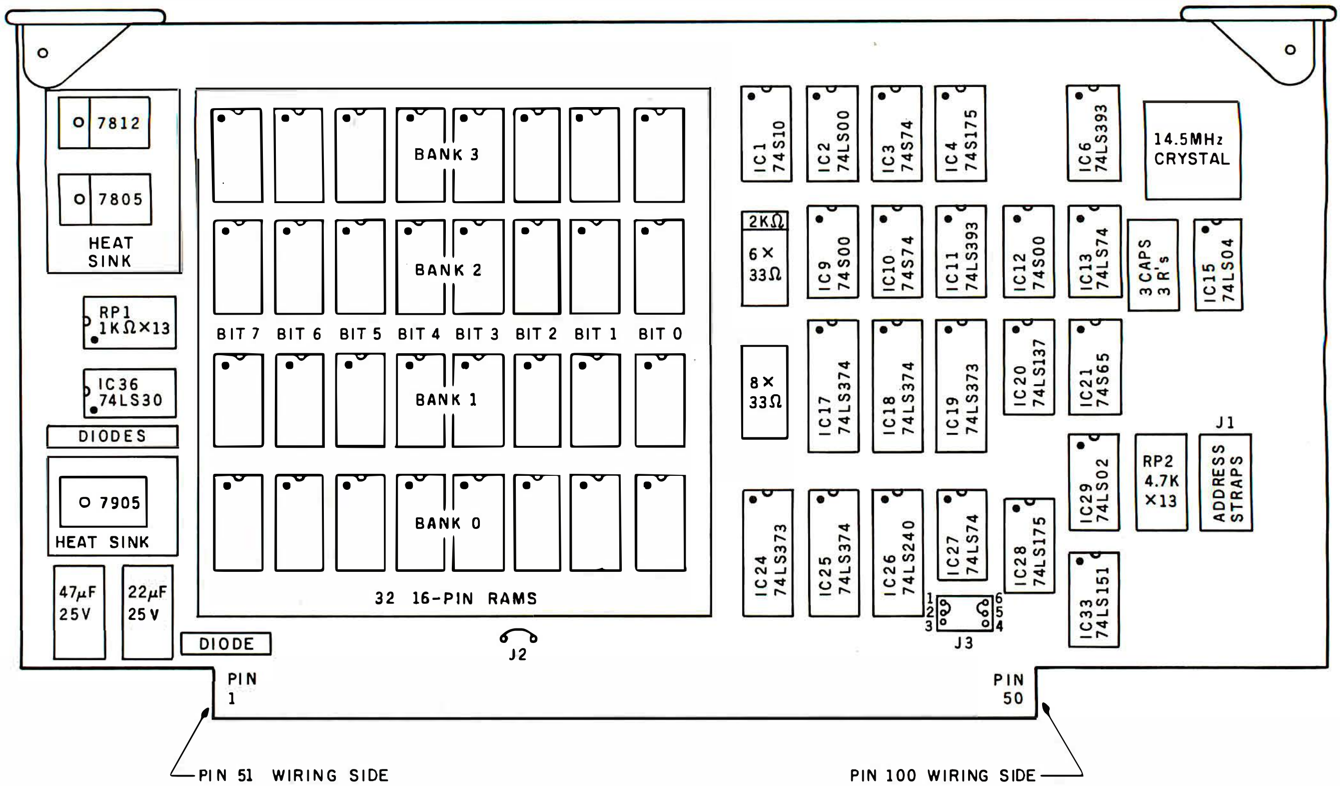


Figure 6: *Layout of ICs on wire-wrap circuit card. Note that, in some places, resistors and capacitors are shown in IC-like blocks.*

resistors and capacitors directly to the pins of the 74S04 socket, keeping leads short and using insulating sleeving. All the other resistors and all ICs but the regulators are in wire-wrap sockets. I made the jumper pads (J2 and J3) by splitting a gold socket with a razor saw.

Once you think you've wired the whole memory, inspect the colored copy carefully for missing color. Then, use an ohmmeter and the second copy to verify that all the connections are there. Inspect that copy, too, for missing color and then compare the two copies. Spot check the longer lines for shorts to other lines. All this checking pays off if you find one wiring error! Finally, inspect the whole job very carefully, in sunlight.

Now, connect the regulators to the circuit and use a meter to verify the supply voltages *at each socket*. You should check each bank of memories for *extra* voltages. After that, mount the 32 decoupling capacitors (0.1-microfarad [µf] ceramic) by soldering them to the pins of the memory sockets. Use a checkerboard arrangement, with a capacitor at every other memory socket between pins 8 and 16. Then mount the second half of the capacitors on the sockets you skipped before, between pins 1 and 16. Then test the supplies *again*.

All the checking pays off if you find one wiring error.

Distribute the remaining 6 or 8 capacitors around the TTL power lines. Remember the TTL power pin assignment: highest numbered pin is +5 V, the pin with half that number is ground.

Debugging

Plug in all the TTL parts and resistors. Apply power to the board and watch it carefully, feeling all the parts for excessive heat. No LS (low-power Schottky) TTL parts should get noticeably warm, and nothing is supposed to get burning hot. If a regulator gets hot enough to burn you, you have a short or a part installed backwards. You can find a bad TTL part by applying power to the board several times, adding one part each time, until you find the one drawing too much current. (TTL is reliable, but when one part dies, it usually shorts.) When all the regulators and the TTL seem right, turn off the board for a while and plug in a row of memory devices. Pick an address bank that is free in your machine's memory space. Don't install a jumper at J1 (8K block enables) yet. Apply power again and quickly measure the voltage at each pin of one memory device. They should run cool to the touch. When all seems well, your new memory has passed its "smoke test."

Install a jumper at J1 to enable half the addresses in the bank of memory. Using your computer's front panel, or machine-language monitor, try to read from and write to the new memory. There are three possibilities now: it looks good, it looks bad because the memory is not working, or it looks bad because the bus is incompatible. If it looks good, load your system software and run your toughest memory test program (see



Listing 2: *These loops exercise parts of the board for observation by oscilloscope. (See also photo 4a.) Remember to disable the chain not being tested.*

```
0000  21 06 00        LD HL,!         ; Reading test.
0003  11 80 7F        LD DE,RAM       ; Row=0s, col=1s
0006  1A            ! LD A,(DE)       ; Observe
0007  E9              JP (HL)

0006  12              LD (DE),A       ; Write test (same loop)
                      END


7F7D  21 80 7F        LD HL,7F80
7F80  E9              JP (HL)         ; Observe an op-code fetch
                      END             ; Used for photo 4a
```

listing 1, on page 372). Run the test overnight. When you see no errors, celebrate and continue with the next section.

Alas, a swarm of potential bugs could plague your new card. Using the divide-and-conquer method, you can sort them into *bus* and *on-card* categories and chase them all down.

First, eliminate the most obvious bus problems. Dig out the schematics of your other cards to see if any of them are using pin 67 for anything but $\overline{\text{PHANTOM}}$. If one is, remove the jumper at J2. Check the processor-board schematic to find out how it derives the status signals. The most common processor board will be a Z80 driving a few gates (probably 74LS02). For this board, connect by jumper pins 1 and 2 on J3, as well as pins 5 and 6. If your system is an 8080A, using an 8228 to derive sMEMR, place the read-status jumper on pins 2 and 3 of J3. If your system is an 8080 with no 8228 or a Z80 inside a spiderweb of gates and one-shots (monostable multivibrators), try moving the other jumper also.

In the worst case, you may have to figure out what the status lines from your particular processor really do and use them to set the three request flags via some special circuit. (I will be glad to help readers who send all the details of their problems, along with a self-addressed, stamped envelope.) Most non-8080 processors have a lot of trouble generating pSYNC, so you might look there first. Some processors generate the S-100 clocks with one-shots, also suspects.

If you have the Z80 version and the card doesn't work, the bug is probably on the card. I debugged the prototype with only a computer, a 5-MHz oscilloscope, and a logic probe. Starting with a valid schematic means you can probably find your manufacturing problem with just a probe.

As you can see in figure 3 (March BYTE, page 318), all activity on the card propagates down two chains: *refresh* and *memory*. The chains share the cycle generator, its clock, power, and the memory devices themselves. Because the refresh chain runs (when all is well) by itself, it's easiest to check first. If your probe can't detect a 25-nanosecond (ns) pulse, hook up a Schottky one-shot on a breadboard for these tests. Check the refresh chain with no other cards plugged into the S-100 bus.

Check to see if the clock is running. If it's not, try a 74LS04 in the socket. The clock ripples through the timer and sets the refresh-request flag (IC13, pin 5). Check whether the flag is stuck and whether the pulse gets to IC4, pin 4 (ANY REQ). IC4 should cycle, clearing the flag again. This logic is self-clearing for any initial state, so any stuck flag reveals a defect. IC4 will cycle every 10 microseconds (μs). Refresh cycles make pulses on IC3, pins 2 through 6, that reach IC20 (address selector) and IC19. IC11 counts, producing long square waves (down to 1 kHz). If any of this isn't happening, the break in the chain pinpoints the trouble.

Because the TTL is static logic, you can run it very slowly. (I first ran the board at 1 Hz to check the gross logic design.) CK5 will still be 20 ns to 40 ns long, however. You can therefore root out a total failure using LEDs (light-emitting diodes). Some devices (the "untested" or "hobby-grade" ones), though, fail only their AC timing tests, and they'll seem to work at low speeds.

The memory-cycle chain is more complex, but its shared parts have been tested already. The easiest part to check is the read-buffer latch (IC24) and its interface. Unplug the memories. Stick a 470-ohm resistor in each of eight memory sockets between pin 14 and either pin 16 (logic 0) or pin 9 (logic 1), and try to read the test pattern formed by using your monitor. If you can't read the proper pattern, lift pin 11 of IC12 and try again. This test checks the path through J1, MADDR, $\overline{\text{TALK}}$, and the output latch. If lifting pin 11 of IC12 makes it work, you have trouble around the $\overline{\text{CAS}}$ gate.

To check the write logic, probe memory pin 3 as you write with your monitor. There should be one pulse per write. (Be sure J1 is properly connected by jumper for this test.) The chain from MWRT to pin 3 is simple. The write-request flag must be free to change state.

If you have an oscilloscope, it's easy to follow pulses through both chains. You can check the signal at various points by lifting one of the request-flag pins and exercising the board with a tight software loop as you observe the other chain (see listing 2). Remember that extra activity is as bad as no activity. $\overline{\text{CAS}}$ should stay high during refresh cycles. $\overline{\text{WR}}$ (write) should stay high during reads. $\overline{\text{CK5}}$ should never be low for more than 50 ns; it may be hard to see, but it can trigger a 74LS74 clock.

Before giving up, have a friend double-check the board for you. Some people can check the same error a dozen times and never see it. Perhaps the information in listing 1 and photos 4a and 4b on page 370 can be used to some advantage.

Think Big

In part 1 of this article, I mentioned

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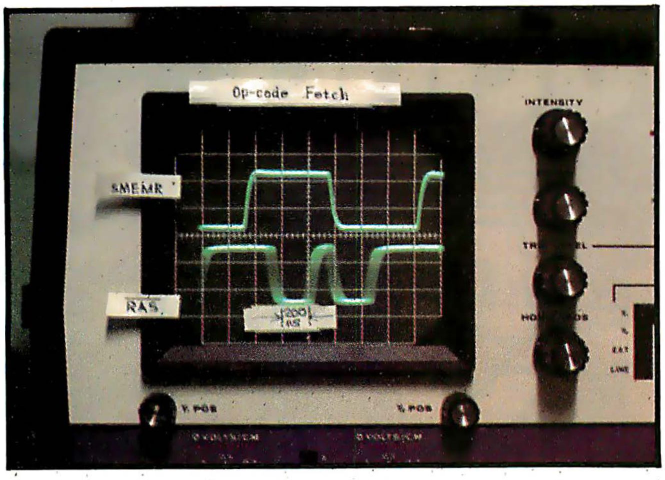


Photo 4a: *The Z80 clock runs at 3.58 MHz, and the memory clock at 14.5 MHz. An op-code fetch (a short Read with M1 high) sets two request flags. The first $\overline{RAS}$ pulse is the actual op code being fetched, and the one on its heels is a "hidden refresh." The time elapsed for each vertical line on the scope face is 200 ns. The horizontal smear on $\overline{RAS}$ is the 69-ns latency time of the cycle generator.*

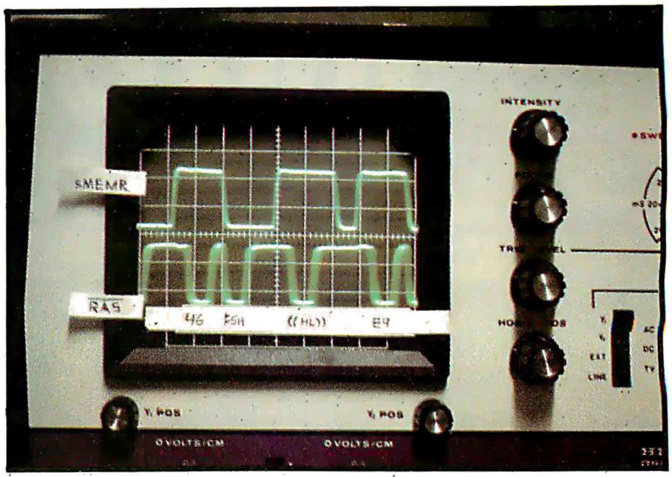


Photo 4b: *This is a "scope loop," like those in listing 2. The first sMEMR (high-going pulse) fetches an indirect-read instruction (B←(HL)). The next sMEMR carries out the instruction. Because HL points to the instructions location, we have two kinds of read from the same location. The single $\overline{RAS}$ in the middle is the data read. Finally, an E9 hexadecimal (jump to (HL)) is fetched, restarting the loop.*

that this card may be expanded to cover a larger address space and to support write protection and overlaid-page selection (sometimes called *paging* or *multiuser*). I have described in detail a 64K-byte memory, but for simplicity's sake the schematic (see figure 4 in part 1 in the March 1983 BYTE, page 320) doesn't show any upgrade options. The fancy addressing additions will fit on the card if you pack the circuit as tightly as I did, but each user's requirements will be different.

On the other hand, the upgrade to denser memory devices is easy. The 4164 is a 64K- by 1-bit dynamic memory device whose pins are almost the same as the 4116's. There is one more address pin (9), and there's only a +5-V supply. Here's how to use the 4164s:

1. Get the board working with 4116s first!
2. Remove the 4116s, the 7812, and the 7905 and its diodes. Replace the 7812 with another 7805. Mount a 1k-ohm resistor between pin 8 and pin 1 of any memory device.
3. Remove any capacitors from pin 9 of the memory grid that used to be the +5-V supply. Connect the pin-9 grid to the two dangling resistors marked by a star on figure 4). Make sure the +5 voltage is no longer present on any pin 9.
4. Move the two wires now on S-100-bus pins 32 and 86 to pins 16 and 17, respectively. Each 8K-byte jumper now represents one 32K-byte block (for a total of 256K bytes).
5. Install the 4164s. Run your toughest memory test. The early version of the 4164 sometimes suffered a high error rate due to internal radioactivity, but this problem has been solved.

As for the other upgrades, you can easily change the 2-bit bank-select latch (IC2) into an output port and control it via software. Be sure to install only two jumpers on J1, or the same 16K-byte block will appear all over your address space.

To build a PC board that will provide write protection for 8K-byte blocks, change the input of the write-request flag (IC13, pin 12) from MADDR to the output of another multiplexer, controlled by a port instead of jumper straps. The port will then control the write enable to each 8K-byte block. It should be cleared by a power-up reset.

Large-Scale Integration

The 4116 contains more than 20,000 transistors. Why, then, can't we find an equally complex IC to replace all that TTL? The manufacturers offer some dynamic RAM (random-access read/write memory) controllers and other support parts now (error-correction devices, line drivers, etc.), but most are still unavailable on the hobby market. The older ones, Motorola 3242 and Intel 8202, provide only a 7-bit address path with no latches in it. These parts do not support the 4164, which is now the preferred device for new designs. Some new parts, now in volume production, are National's DP8409, TI's TMS4500A, Intel's 8203 and 8207, and AMD's Am2964B. These devices support the 4164.

During the time this article was in production, my associates at Video Concepts of Maryland (4401 East-West Highway, Suite 408, Chevy Chase, MD 20014) have developed my hobby project into a commercial-quality printed-circuit board. They have added addressing accessories that support most of the de facto standard operating systems used in S-100 machines. The card easily accommodates 4116s, 4164s, or the newly available 41256s (you guessed it: 256K bits in one 16-pin package!), and it uses the Am2964B to save about half the small TTL devices shown in this article.■

Circle 265 on inquiry card.

Listing 1: *Use this program to convince yourself the card is really working. The program writes a test pattern, waits 5 seconds (to test refresh), checks the pattern, and inverts the pattern. After two passes, the main loop has tested each cell with a 0 and a 1. The program calls monitor routines for I/O, as described in the equates at the top. You will have to fill in the addresses for your monitor. It prompts for the limits of memory in order to test and for a character in order to flag continuous or once-through operations.*

A counter is maintained for each 4116. The low byte counts errors, and the high byte records the error pattern. The counter dump forms a map of the board (front view), so that you can see a bad device easily. A dump of all 0s says all is well.

The column buffer register isn't exercised by the test. To check it, use your monitor to write at 1000 hexadecimal. Check that the byte you wrote doesn't appear at addresses 1080, 1100, 1200, . . . , 3000 hexadecimal. An open or stuck bit would cause the same byte to appear at two locations.

```
                              ;              CONFIDENCE          by Cam Spitzer
                              ;                                  and Phil Perucci
                              ;
                              ;        This program will count errors in an expanse of RAM.
                              ; It requires external I/O routines for 16 bit numbers, and for ASCII.
                              ; A single pass will count ALL errors, and once there are no hard
                              ; errors, the continuous mode will accumulate soft errors.
                              ;
                              ;        Stuck RAM address lines will appear as large chunks of errors.
                              ; The column address buffer register, and address lines A7-A15 are not
                              ; tested.
                              ;
                              ;
                              ;        Fill in the locations of your monitor routines:
                              ;
F2E4                          SP16IN   EQU     0F2E4H  Type a space, then get a number into HL.
F317                          OUT16    EQU     0F317H  Type out value in HL.
F355                          ASCOUT   EQU     0F355H  Type A out as ASCII.
F361                          ASCI     EQU     0F361H  Get an ASCII character into A.
F015                          CRLF     EQU     0F015H  Type carriage return, line feed.
F081                          YERMON   EQU     0F081H  Graceful monitor re-entry point.
                              ;
0093                          TIX      EQU     93H     Data retention time constant (about 5 sec.)
                              ;
                              ;
                              ;        The test resides in 1K of known good RAM, beginning at SAFE.
                              ;
0000                          SAFE     EQU     0000
                              ;
0000                                   ORG     SAFE
                              ;
0000  00                      TIMES    DB      0               Single or running test.
0001                          ERRS     DS      64              Bit error count. (32 words)
                              ;                                 Low byte counts errors.  High byte records
                              ;                                 error bit pattern.  (ERRS) refers to Bank 0,
                              ;                                 bit 0.  (ERRS+63) refers to Bank 3, bit 7.
0041  00  00                  WASTE    DW      0
0043  00  00                  STRMUD   DW      0               Start of MUD.  (Memory Under Debug.)
0045  00  00                  ENDMUD   DW      0
                              ;
03FD                          STAK     EQU     SAFE+3FDH
                              ;
0047  31  FD  03              BEGIN    LD      SP,STAK
004A  3E  40                           LD      A,'a'
004C  CD  6E  00                       CALL    ASCO           Prompt for lower test limit.
004F  CD  E4  F2                       CALL    SP16IN
0052  22  43  00                       LD      (STRMUD),HL    Save lower limit.
0055  3E  3B                           LD      A,';'
0057  CD  6E  00                       CALL    ASCO           Prompt for end of supposed RAM.
005A  CD  E4  F2                       CALL    SP16IN
005D  22  45  00                       LD      (ENDMUD),HL    Upper limit.
0060  3E  58                           LD      A,'X'
0062  CD  6E  00                       CALL    ASCO
0065  CD  61  F3                       CALL    ASCI
0068  32  00  00                       LD      (TIMES),A      Continuous test?
                              ;
006B  C3  78  00                       JP      GENTP
                              ;
006E  C3  55  F3              ASCO     JP      ASCOUT         Eases relocation for you.


0078                                   ORG     78H
                              ;
                              ;        Loop to write a test pattern:
                              ;
0078  ED  5B  43  00          GENTP    LD      DE,(STRMUD)
007C  0E  00                           LD      C,00H           Positive mask.  (Neg. = FFH)
007E  7B                      ONETP    LD      A,E
007F  A9                               XOR     C
0080  12                               LD      (DE),A          The positive test pattern is simply
                              ;                                 the low byte of the address.
0081  CD  CD  00                       CALL    CPDEHL
0084  28  03                           JR      Z,TPISIN
```

Listing 1 continued on page 376

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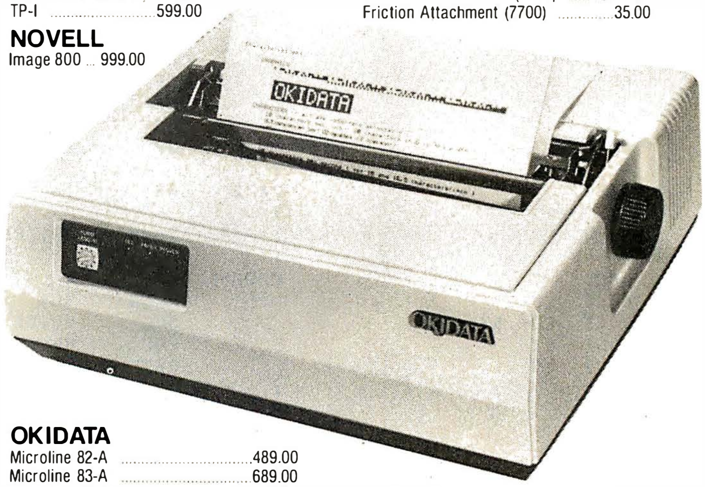
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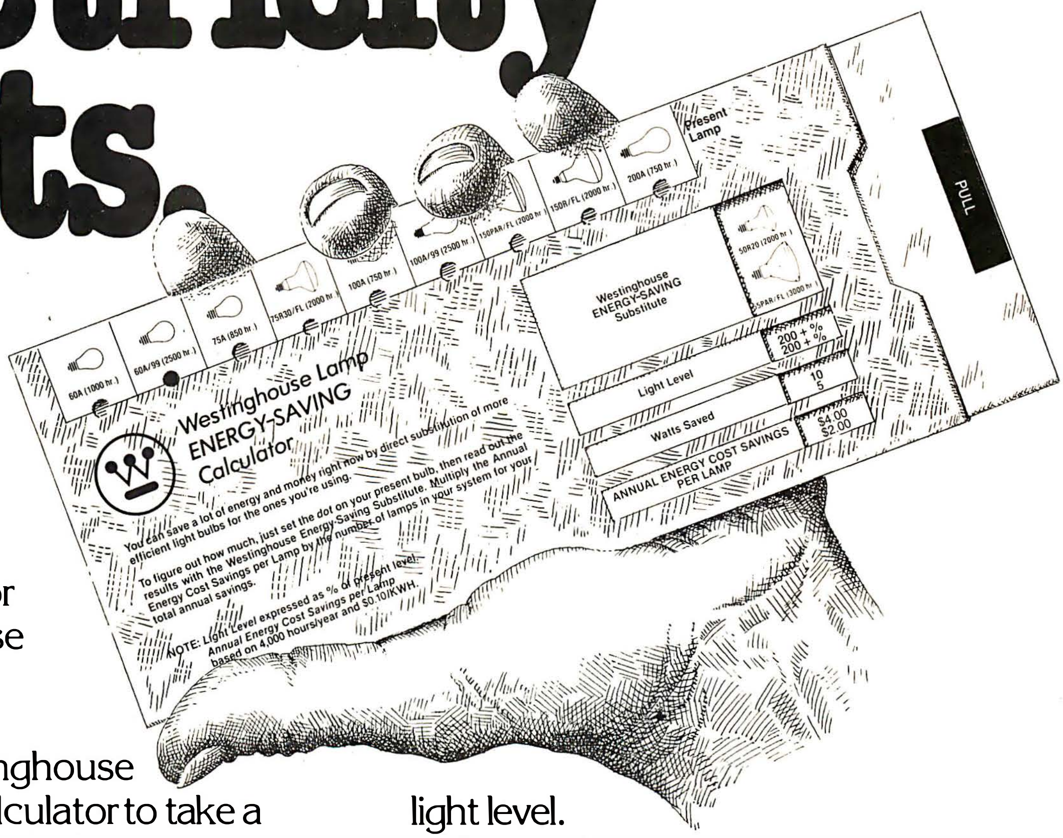
Circle 326 on inquiry card.

Listing 1 continued:

```
0086  13                    INC     DE
0087  18  F5                JR      ONETP
                     ;
                     ;      Setup the test.
                     ;
0089  AF             TPISIN XOR     A               Zero.
008A  06  40                LD      B,64
008C  11  01  00            LD      DE,ERRS
008F  12             CLRERR  LD      (DE),A         Initialize error counters.
0090  13                     INC     DE
0091  10  FC                 DJNZ    CLRERR
0093  06  02                LD      B,2             Loop count for single test,
                     ;
0095  00  00  00  00  00  PAD1  DW    0,0,0,0,0,0,0,0
                     ;
                     ;      Main loop.
                     ;
00A5  CD  6A  01     TEST   CALL    LAPSE
00A8  CD  DB  00            CALL    BYTES  Check pattern
00AB  CD  04  01            CALL    COMPL  Flip it
00AE  CD  28  01            CALL    DUMP   Dump error count.
00B1  3A  00  00            LD      A,(TIMES)
00B4  FE  31                CP      '1'    Once?
00B6  20  ED                JR      NZ,TEST
00B8  10  EB                DJNZ    TEST
00BA  C3  81  F0            JP      YERMON  Done.
                     ;
00BD                 PAD2   DS      16
                     ;
                     ;      Compare DE, HL
                     ;
00CD  A7             CPDEHL OR      A      Clr carry.
00CE  E5                    PUSH    HL
00CF  ED  52                SBC     HL,DE
00D1  E1                    POP     HL
00D2  C9                    RET            Zero if =, Minus if DE>HL
                     ;
00D3                 PAD3   DS      8
                     ;
                     ;      Verify expected pattern
                     ;
00DB  ED  5B  43  00  BYTES  LD     DE,(STRMUD)
00DF  2A  45  00            LD      HL,(ENDMUD)
00E2  1A             ONETST LD      A,(DE)
00E3  AB                    XOR     E
00E4  A9                    XOR     C
00E5  28  06                JR      Z,OKBYTE
00E7  CD  91  01            CALL    BYFAIL          Count the erroneous RAMs.
00EA  7B                    LD      A,E
00EB  A9                    XOR     C               Recompute the expected pattern.
00EC  12                    LD      (DE),A          Remind the flaky RAM.
                     ;                              This way, soft errs count just once.
00ED  CD  CD  00     OKBYTE CALL    CPDEHL
00F0  C8                    RET     Z
00F1  13                    INC     DE
00F2  18  EE                JR      ONETST
                     ;
00F4                 PAD4   DS      16
                     ;
                     ;      Complement mask and test pattern
                     ;              After two passes, main loop has tried 0's and 1's
                     ;              in each bit of MUD.
                     ;
0104  79             COMPL  LD      A,C
0105  2F                    CPL                     Mask
0106  4F                    LD      C,A
0107  ED  5B  43  00        LD      DE,(STRMUD)
010B  2A  45  00            LD      HL,(ENDMUD)
010E  1A             ONEFLP  LD      A,(DE)
010F  2F                     CPL                    RAM contents
0110  12                     LD      (DE),A
0111  CD  CD  00             CALL    CPDEHL
0114  C8                     RET     Z
0115  13                     INC     DE
0116  18  F6                 JR      ONEFLP
                     ;
0118                 PAD5   DS      16
                     ;
                     ;      Dump out the 32 error counters
                     ;
0128  C5             DUMP   PUSH    BC
0129  E5                    PUSH    HL
012A  DD  21  3F  00        LD      IX,ERRS+62          Dump in descending order.
012E  06  04                LD      B,4                 4 Banks.
0130  CD  15  F0     DBANK   CALL    CRLF
0133  C5                     PUSH    BC
0134  06  08                 LD      B,8                 8 Bits.
```

Listing 1 continued on page 378

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Circle 442 on inquiry card.

Listing 1 continued:

```
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0138  CD  6E  00              CALL    ASCO
013B  DD  66  01              LD      H,(IX+1)
013E  DD  6E  00              LD      L,(IX+0)
0141  CD  17  F3              CALL    OUT16
0144  DD  2B                  DEC     IX
0146  DD  2B                  DEC     IX
0148  10  EC                  DJNZ    DBIT
014A  C1                     POP     BC
014B  10  E3                 DJNZ    DBANK
014D  E1                    POP     HL
014E  C1                    POP     BC
014F  C3  15  F0            JP      CRLF            Blank line upon completion.
                      ;
0152                  PAD6  DS      24
                      ;
                      ;       Delay (to test data retention while no MCYRQ's)
                      ;
016A  C5              LAPSE PUSH    BC
016B  06  93                LD      B,TIX   Time is roughly proportional to TIX cubed.
016D  C5              L1     PUSH    BC
016E  C5              L2      PUSH    BC     (For TIX=FFH, at 4MHz Z-80 clock,
016F  10  FE          L3       DJNZ    L3    LAPSE takes about 20 seconds.)
0171  C1                      POP     BC
0172  10  FA                  DJNZ    L2
0174  C1                     POP     BC
0175  10  F6                 DJNZ    L1
0177  C1                    POP     BC
0178  C9                    RET
                      ;
0179                  PAD7  DS      24
                      ;
                      ;       Bad data was read, so count each 4116 in error.
                      ; Entry:        (DE) => bad byte
                      ;               (A)  => set bits flag error positions.
                      ;
                      ; Exit:         All appropriate error counters have been bumped.
                      ;               No regs A-L altered
                      ;               (IX) => counter of highest bad bit.
                      ;
0191  E5              BYFAIL PUSH   HL
```

Listing 1 continued on page 380

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Listing 1 continued:

```
0192  D5                     PUSH    DE
0193  C5                     PUSH    BC
0194  F5                     PUSH    AF
0195  DD  21  01  00         LD      IX,ERRS        Point to base of error counters.
0199  7A                     LD      A,D
019A  CB  0F                 RRC     A
019C  CB  0F                 RRC     A
019E  E6  30                 AND     00110000B
01A0  5F                     LD      E,A            E => which bank has failure in it. (Bits 5,4)
01A1  16  00                 LD      D,0
01A3  DD  19                 ADD     IX,DE          Point to 8 counters.
01A5  F1                     POP     AF             Restore bad bits to A.
01A6  F5                     PUSH    AF
01A7  06  08                 LD      B,8            Loop 8 times.
01A9  CB  0F         BITCHK   RRC     A
01AB  4F                      LD      C,A
01AC  E6  80                  AND     10000000B
01AE  79                      LD      A,C
01AF  28  03                  JR      Z,OKBIT
                     ;                              Here he is!
01B1  DD  34  00              INC     (IX+0)        Count the little jerk.

01B4  DD  23         OKBIT    INC     IX
01B6  DD  71  00              LD      (IX+0),C      Store the error pattern.
01B9  DD  23                  INC     IX            Ready next counter.
01BB  10  EC                  DJNZ    BITCHK
01BD  F1                     POP     AF
01BE  C1                     POP     BC
01BF  D1                     POP     DE
01C0  E1                     POP     HL
01C1  C9                     RET
                     ;
                     ;        Special thanks to Litton Amecom's Electronic Warfare Product
                     ; Development Department, for the after-hours use of their Zenith Z-89
                     ; microcomputer, on which this program was assembled.   Also the Real-
                     ; Time Software Department for the use of their line printer, and
                     ; Mike Cunningham (EW Product Dev.) for software and systems support.
                     ; I am proud to have been associated with this organization.
                     ;
                             END     BEGIN
```

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In 1969, no appropriate programming language existed to clearly display the problem-solving techniques known as *structured programming*. Niklaus Wirth wanted to teach the principles of structured programming unencumbered by the irregularities and deficiencies of existing languages. To accomplish his task, he designed a new and elegant language: Pascal. Then, after nine years of researching Pascal's problems, Wirth created a language to replace it; that language is Modula-2.

Despite its lack of support from either the government or the computer industry, Pascal's remarkable ability to clearly express algorithms and data structures soon vaulted it out of academia and into the commercial world. In 1977, Welsh, Sneeringer, and Hoare (see reference 3) stated that "Pascal is at the present time the best language in the public domain for purposes of system programming and software implementation." Pascal's popularity soared phenomenally through the 1970s, and today it is one of the most popular microcomputer languages.

And yet, Brian Kernighan, a proponent of the C language, describes Pascal in its pure form as "suitable only for small, self-contained programs that have only trivial interactions with their environment and that make no use of any software written by anyone else" (see reference 1). In his blunt but accurate analysis of Pascal, Kernighan identifies eight major areas where Pascal lacks capabilities necessary for serious programming. He concludes that "Pascal is a toy language, suitable for teaching but not for real programming."

How can Pascal be the best system-programming language available while being completely unsuitable for anything but teaching?

Extended Pascal

In his famous Turing Award lecture (see *Communications of the ACM*, February 1981; reprinted in September 1981 BYTE, page 414), Tony Hoare offered advice on language design that helps to resolve these two points of view: "You include only those features which you know to be needed for every single application of the language and which you know to be appropriate for every single hardware configuration on which the language is implemented. . . . That is the great strength of Pascal, that there are so few unnecessary features and almost no need for subsets. That is why the language is strong enough to support specialized extensions. . . ."

Editor's Note: *Portions of this article were presented at the Mini-Micro '82 Computer Conference and Exhibition, September 14-16, Anaheim, California.*

About the Authors

Joel McCormack is a software and hardware engineer at Volition Systems. As a UCSD graduate student, he coauthored the UCSD Pascal Z80 interpreter. McCormack is coauthor of Volition's Modula-2 compiler.

Richard Gleaves is a software engineer and technical writer at Volition Systems. Formerly a member of the UCSD Pascal project, Gleaves is coauthor of the original Apple Pascal interpreter and Softech Microsystem UCSD Pascal compiler.

Computer manufacturers, software houses, and universities have repeatedly shied away from computer languages nominally designed for "real programming." Recognizing the truth in both Kernighan's and Hoare's comments, they have instead chosen (or created) extended versions of Pascal. These computer users have no desire to sacrifice Pascal's unique abilities to:

- clearly describe data structures and algorithms
- detect programming errors as syntax errors (rather than quietly rearrange the meaning of the program)
- protect against improper mixing of different types
- prohibit assigning illegal values to variables

While C and FORTH proponents often dismiss these advantages as trivial, the worldwide proliferation of Pascal dialects testifies to the number of programmers who disagree.

Oregon Software and Digital Equipment Corporation have extended Pascal for real-time work; the University of California, San Diego, and Microsoft included features oriented to programming operating systems; Texas Instruments, Hewlett-Packard, Burroughs, National Semiconductor, and IBM have all added capabilities beyond the basic language. Even Tony Addyman, the driving force behind the ISO (International Organization for Standardization) Pascal Standard, admits to using a "kludged version of Pascal" in his hardware laboratory. How much do these various Pascals have in common? How well designed are their extensions?

The answers, sadly enough, are "not much" and "not very."

For example, UCSD Pascal (and derivative systems such as Apple Pascal and Pascal/M) includes predefined procedures for manipulating character arrays. Called Scan, MoveLeft, MoveRight and FillChar, these procedures blithely accept arguments of incorrect types, perform no checking of array bounds, and, unless used with the utmost care, can "wear out their welcome with random precision." Microsoft Pascal has a similar but different set of procedures called ScanEq, ScanNe, MoveL, MoveR, and FillC.

Critical analysis of existing extensions drives home two points: (1) most programmers (though they may be very good programmers) are poor language designers; and (2) any given deficiency of Pascal has been "solved" in at least a dozen different ways.

Standard Extended Pascal

The alarming growth in extended Pascal dialects naturally led to the idea of defining a standard set of Pascal extensions. The first such effort was organized (with Wirth's approval) in January 1978 by Dr. Jorgen Steensgard-Madsen. Nine major implementers of Pascal (all but one from universities) attempted to reach agreement on a small number of extensions. This effort resulted only in the OTHERWISE clause for the CASE statement and some suggestions on the ISO Pascal standardization effort regarding conformant array parameters (see reference 2).

A second group—this time mostly commercial implementers—was assembled by Ken Bowles in July 1978, but this effort fared no better than the first. Though many language extenders were in attendance, few were experienced language designers. Group members tended to be loyal to extensions already implemented in their own compilers, so in the limited amount of time allotted for the conference only a small number of extensions—all trivial—was approved. A large number of items was passed on to the Steensgard-Madsen group, which at the time still appeared to be a viable committee. The remaining hodgepodge of conflicting proposals was tossed together under the label "experimental." (This meeting is documented in "Proceedings of the UCSD Workshop on Systems Programming Extensions to the Pascal Language," Institute for Information Systems, UCSD, 1979.)

Today, a third attempt is being made to standardize Pascal language extensions, this time under the auspices of the American National Standards Institute (ANSI). Considering the outcome of the first two groups (in which one of the authors participated) and the slow and tortuous path taken just to define an ISO Pascal standard, we have doubts that the ANSI effort will prove any more effective than its predecessors. The time for agreement on Pascal extensions quietly passed years ago; even if ANSI could issue a standard tomorrow, the prospects are bleak for conformance by major Pascal vendors. Popular systems such as Apple Pascal and UCSD Pascal fail to conform to even the base language standard. With their large (and growing) user base, such vendors may find it difficult to offer a new set of standardized extensions while maintaining compatibility with their plethora of existing proprietary extensions.

Meanwhile, Modula

Niklaus Wirth's direct involvement in the Pascal extension efforts was conspicuously small. Indeed, years of debate might have been avoided had he stepped in with his own extension proposals. However, Wirth's comments reflect a motivation by ideals rather than by politics: "If a language proves to be only marginally suitable for some application that was obviously not envisaged by its originator, we should muster the courage to build a new, truly adequate tool, instead of just grafting a fix onto the existing one" (see page 83 of reference 4).

After designing Pascal, Wirth chose to investigate the programming problems posed by multiprocessing and I/O devices. He designed the special-purpose language Modula to gain firsthand experience with programming small real-time control systems:

> The primary benefit of the use of a suitable high-level language lies in the possibility of defining abstract machines in a precise manner that is reasonably independent of characteristics of particular hardware. Assembly code is still used virtually exclusively in those applications whose predominant purpose is not to design a new system based on abstract specifica-

tions, but to operate an existing machine with all its particular devices. . . . A major aim of the research on Modula is to conquer that stronghold of assembly coding, or at least to attack it vigorously [reference 4, page 3].

Modula consisted of a minimal subset of Pascal, to which was added the module structure, an improved syntax, and facilities for multiprocessing and low-level machine access. Unlike Pascal, Modula was not intended as a general-purpose language: among other things, it lacked Pascal's files, sets, and pointers. Modula's most significant feature was the module structure. While programming was awkward without Pascal's data-structuring facilities, modules proved an invaluable asset—as far a step beyond Pascal's block structure as the block structure had been beyond the FORTRAN subroutine call.

Though Modula is still in use today at some universities, Wirth discontinued his own research with the language after spending a sabbatical year at the Xerox Palo Alto Research Center (PARC). Modula had served its purpose as a programming tool designed for a specific task.

Finally, Modula-2

At Xerox PARC, Wirth had the opportunity to use the Alto personal computer and the Mesa programming language. Upon returning to Switzerland, he embarked on a project to design a similar but simpler computer system—including both hardware and software. Wirth states:

> This system (later to be called Lilith) was to be programmed in a single high-level language, which therefore had to satisfy requirements of high-level system design as well as those of programming of parts that closely interact with the given hardware. Modula-2 emerged from careful design deliberations as a language that includes all aspects of Pascal and extends them with the important module concept and . . . multiprogramming [see page 3 of reference 5].

Modula-2 is a general-purpose systems-implementation language that includes the best elements of its predecessors. Modula-2's statement structures and data types are a superset of Pascal's; the systematic syntax, module concept, machine access, and multiprocessing are improved versions of those features found in Modula-1. In addition, the design of Modula-2 systematically addresses Pascal's problems (see "Solving Pascal's Problems" on page 389).

Modules

The key difference between Modula-2 and Pascal is in the way they are extended. Pascal extensions are built into the language, so Pascal programmers cannot change them or add new extensions. Modula-2 is extensible—it allows Modula-2 programmers to create their own extensions. The key to this ability is the module structure.

A module is a collection of declarations that work together to perform a given task. A simple example of a

Listing 1: *The module RandomNumbers serves as a wall around the random function and its seed variable. The export statement allows the random function to be called outside of the module, but the seed variable remains hidden inside the module and can be accessed only by the random function. The outer block of the module is automatically executed when the program begins; it assigns an initial value to Seed by assigning it the value of the identifier SystemTime. SystemTime is declared outside of the module but can be accessed inside because it has been imported.*

Note how the module contains all the details concerning the operation of the random-number generator; only the identifier Random is visible outside the module. It is their ability to collect together and hide all the unnecessary details of a mechanism that makes modules such powerful constructs for organizing large programs.

```
MODULE MainProgram;

  VAR i: INTEGER;

  ...

  MODULE RandomNumbers;

    IMPORT SystemTime;
    EXPORT Random;

    VAR Seed: INTEGER;

    PROCEDURE Random( ): INTEGER;
    CONST Modulus = 7415;
          Inc     = 25543;
    BEGIN
      Seed := (Seed + Inc) MOD Modulus;
      RETURN Seed;
    END Random;

  BEGIN
    Seed := SystemTime;
  END RandomNumbers;

    ...

BEGIN
  i := Random( );
  ...

END MainProgram.
```

Listing 2: *This program uses three separately compiled modules: the library module SimpleFiles; the definition module, which exports the type FILE and file operations; and the implementation module.*

```
DEFINITION MODULE SimpleFiles;

  EXPORT QUALIFIED
    FILE, Open, Close, Read, Write, Error;

  TYPE FILE;     (* Opaque type... structure unknown outside *)


  PROCEDURE Open  (VAR f: FILE; name: ARRAY OF CHAR);
  PROCEDURE Close (VAR f: FILE);
  PROCEDURE Read  (f: FILE; VAR ch: CHAR);
  PROCEDURE Write (f: FILE; ch: CHAR);

  PROCEDURE Error (f: FILE): BOOLEAN;  (* TRUE if I/O error *)

END SimpleFiles.
```

```
 IMPLEMENTATION MODULE SimpleFiles;

 FROM SYSTEM IMPORT ADDRESS, ADR;

 CONST FileNameLength = 20;

 TYPE blockrange = [0..511];

 TYPE FILE = POINTER TO RECORD     (* Details hidden inside *)
              FileName: ARRAY [0 .. FileNameLength-1] OF CHAR;
              CASE diskfile: BOOLEAN OF
                TRUE:  diskblock: CARDINAL;
                       byteinblock: blockrange;
                       buffer: ARRAY blockrange OF CHAR;
              | FALSE: IOUnit: CARDINAL;
              END (* case *)
            END (* FILE *);

 PROCEDURE Open (VAR f: FILE; name: ARRAY OF CHAR);
  (* body of Open *)
 END Open;
 ...
  PROCEDURE DiskIO (unit: CARDINAL; buf: ADDRESS);
   (* low-level procedure hidden in module *)
  END DiskIO;

BEGIN
 ...
END SimpleFiles.
```

```
 MODULE MyProgram;

   FROM SimpleFiles IMPORT
     FILE, Open, Close, Read, Error;

   VAR f1, f2: FILE;
       ch: CHAR;

 BEGIN
   Open(f1, "myfile.data");
   ...
   Read(f1, ch)
   IF Error(f1) THEN HALT END;
   ...
   Close(f1);
 END MyProgram.
```

module is a random-number generator consisting of a random function and its seed variable (see listing 1). A module forms a wall around its objects; except for explicitly *imported* and *exported* identifiers, the module's contents are isolated from the surrounding program. In the random-number generator, the procedure Random( ) can be called from outside the module because it is exported; the variable Seed, however, remains hidden inside the module and is accessible only by the random function.

It is their ability to encapsulate related declarations that makes modules such a powerful concept—they are the software equivalent of a "black box." Modules partition large programs into logically related pieces with well-defined interfaces (i.e., the imported and exported identifiers); as a result, Modula-2 programs are easier to read, easier to understand, and less prone to erroneous side effects than Pascal's block-structured programs. (Anyone who has ever read a large Pascal program knows how they are structured: an army of procedures interconnected by pages of global declarations.)

The ability of modules to divide programs into semi-independent parts provides the foundation for separate compilation in Modula-2. Library modules are divided into two separately compiled parts: a *definition module* and its corresponding *implementation module.* The definition module contains declarations made available to other modules (called *client modules*). The implementation module contains the actual code and data that implement the operations defined by the definition module.

Listing 2 shows three separately compiled modules. The library module SimpleFiles provides a simple file I/O system, the definition module exports the type FILE and file operations, while the implementation module contains the code implementing the file system.

The type FILE is called an *opaque* type—its record fields are fully accessible within the implementation

module, but only the type name is visible outside the module. Opaque types are a form of the programming concept known as *abstract data types*. Abstract data types are objects whose only operations are defined by a set of procedures. Pascal's FILE type is an example of an abstract type; however, Pascal does not allow programmer-defined abstract types.

This example introduces the concept of *qualified* export. When an export list includes the symbol QUALIFIED, client modules must prefix all references to the exported identifiers with the name of their module; for instance, the identifier Open would have to be referenced as SimpleFiles.Open. Qualified export allows library modules to avoid clashes with identifiers already declared in client modules. Client modules in turn can "unqualify" identifiers by preceding their import lists with the symbol FROM and the library module name.

The module MyProgram imports SimpleFiles to perform its file I/O. MyProgram is an executable program; however, it can also be called by other modules as a subprogram. (Subprogram calls are performed with the procedure Call exported by the library module Program.) Programs and subprograms share information by importing the same library module.

Separate Compilation

The separate compilation facilities in most programming languages are more aptly termed "independent compilation" facilities; no type checking is performed between separately compiled parts. This has traditionally been a great source of problems, especially when parts of a large software system are developed by different people. In fact, data-processing professionals invented a special term to describe this sometimes harrowing task: they call it "system integration."

Modula-2 is specifically designed to maintain type checking across module boundaries. The compiled form of a definition module contains type information that is accessed when compiling both the corresponding implementation module and all client modules. The separation of definition and implementation enables you to change implementation modules without forcing recompilation of all client modules. Because the definition module remains unchanged, type consistency is preserved. This saves a lot of unnecessary system-generating (sysgen) time when maintaining large software systems.

Changing both definition and implementation, however, invalidates all client modules because the interface between the module and its clients has now changed. Executing an out-of-date client module might crash the system.

Wirth solved this problem in Modula-2 by maintaining a system-wide module-version control scheme. When a definition module is compiled, the compiler assigns a unique value to the module. This value is known as a *module key*. When the corresponding implementation module is compiled, it inherits the module key of its definition. When a

Solving Pascal's Problems

In a paper entitled "Why Pascal Is Not My Favorite Programming Language," the noted C language proponent Brian Kernighan identifies eight major problems with Pascal. R.T. Summer and R.E. Gleaves have shown how Modula-2 addresses each of these problems ("Modula-2—A Solution to Pascal's Problems," ACM SIGPLAN Notices, September 1982):

Pascal arrays are fixed in size, making string handling difficult and general-purpose math libraries impossible.

Modula-2 includes "open" array parameters, which accept arrays of varying length. Also, character strings are assignable to array variables of different lengths.

Pascal's lack of "own" variables forces programmers to use global variables, which have a larger scope than they ought to.

The module structure offers a superior method for hiding variables from most of a program.

Pascal's lack of separate compilation hinders the development of large programs and makes the use of libraries impossible.

Modula-2 offers separately compiled library modules and subprogram modules. Library modules are collections of procedures and data that are accessible by other modules. Subprogram modules are separately compiled modules that can be called by other modules. Unlike many languages, Modula-2 offers full type checking across separately compiled modules.

Pascal's required declaration order prevents related declarations from being grouped together.

Modula-2 allows constants, types, variables, procedures, and modules to be declared in any order. Modules provide an even better way to group related declarations.

Pascal's Boolean expressions are not conditionally evaluated, resulting in convoluted expressions and extraneous state variables.

Modula-2 explicitly defines the evaluation order of logical expressions as conditional "short-circuit" evaluation, allowing statements like "WHILE (p < > NIL) AND (p↑.data < 0) DO. . ."

Pascal's CASE statement is hampered by its lack of an OTHERWISE clause.

Modula-2 CASE statements have an optional ELSE part for catching unspecified case values. Also, subranges can be used in case constant lists, eliminating the need to explicitly declare all case constant values.

Pascal's I/O facilities are extremely limited; they cannot deal with real-world files or program arguments.

The Modula-2 language includes no I/O facilities. I/O is provided by standard library modules, but these can be supplemented (or replaced) by defining different I/O modules.

Pascal's strict enforcement of type checking prohibits low-level programming.

Modula-2's low-level programming facilities provide machine-level operations: type conversion, pointer arithmetic, bit manipulation, and direct access to memory. Unlike many languages, Modula-2 provides controlled low-level access, preventing erroneous high-level programs from merely becoming low-level programs.

client module imports the library module, a copy of the imported module's key is recorded in the resulting code file.

When a program is executed, the program loader checks that the module keys recorded in the program match those found in the compiled code of the imported implementation modules. As implementation modules receive their keys from the corresponding definition module, implementations can be optimized, modified, or entirely replaced without affecting any client modules. But if a definition module (and, subsequently, its implementation) is recompiled—perhaps to change a parameter list or add a variable to the module's interface—a new module key is assigned. Attempts to execute client modules compiled with the old library module result in a version error, indicating that the client module must be recompiled.

The implications for multiperson project management are revolutionary: system integration no longer needs to be plagued by mismatches between the agreed-upon interfaces and the actual code.

If a software system is sufficiently well understood to be fully defined beforehand, the system's definition modules can be distributed in compiled form to the programming team members, who can then write and modify implementation modules without forcing everybody else on the project to recompile when a change is made. Individual team members cannot alter a module interface, as the compiler enforces conformance between the procedure headings declared in the definition module and the corresponding headings in the team member's implementation module.

If team members are granted access to the source text of definition modules (to make small changes to the specification), several versions of the "same" definition module may proliferate; however, the version-control system prevents the execution of mismatched modules, allowing system testing to proceed only after all modules adhere to the same set of interfaces.

Libraries

Pascal requires an underlying operating system for its I/O and storage management. Modula-1 requires a small run-time system for scheduling processes. Modula-2 requires neither: because such operations are programmed as library modules, the language itself requires virtually no support above the hardware level.

A Modula-2 library typically contains modules for the following operations:

- Console I/O and keyboard polling
- Format conversion between text and binary representations
- File I/O operations—read, write, and seek
- File directory operations—create, delete, and rename
- Storage management—new and dispose
- Program execution
- Process scheduling
- Mathematical functions
- Dynamic string manipulation

It is no coincidence that these operations are normally the domain of an operating system; however, there is a crucial difference between module libraries and operating systems. Operating systems are traditionally written by elite bands of systems programmers who, in their attempts to deliver monolithic systems suitable for all applications, often create systems with so much overhead that they are unusable. Modula-2 lets you select the system facilities you need without having to pay for those you don't need. The module library constitutes a flexible and extensible operating system.

The library contains not only the usual system facilities, but also every library module and program module in the system. Any library module in the system can be imported by any other module; any program module in the system can be called as a subprogram by any other module. This encourages a building-block approach to the development of software systems: high-level library modules are built from collections of low-level modules; large programs are built from collections of smaller programs.

Modula-2's library concept offers the potential for writing portable software systems that can be moved with little or no change across different operating systems. A set of standard definition modules can provide client modules with an operating environment that is independent of any operating system. Moving software to a new operating system merely requires a set of implementation modules that use the host system's facilities to implement the standard definition modules. (This approach is equally suited for using large systems to develop software targeted for small stand-alone systems.)

Modula-2 also has a remarkable ability to incorporate existing software into the Modula-2 environment. Programs written in other languages can be called as subprograms, thus becoming part of a Modula-2 program. Specially defined modules can access non-Modula library routines, host-operating-system calls, and even machine instructions. Yet, because all these facilities are accessed via definition modules, they are uniformly referenced as Modula-2 library modules.

As Wirth so succinctly states, library modules are "an essential part of a Modula-2 implementation" (see reference 5).

Run-Time Binding

The modular nature of Modula-2-based systems requires a different environment from that of most software development systems. In particular, the compiler, program loader, and library form an integrated system, with module binding performed automatically at run time. Adding a module to the library (or updating an existing module) requires only that the module be compiled; the compiler writes the code file to the library, so when the module (or one of its clients) is executed, the loader can find it by searching the library.

Run-time module binding eliminates linking and the resulting problems associated with large linked object files containing multiple copies

of the same module code. Instead, a single copy of a module-code file can be shared by a number of programs. Because run-time binding is slower than executing prelinked object files, facilities are also provided for optionally linking collections of modules together to form a single object file. This yields faster program loading at the expense of extra effort to update any of the modules in the program.

Procedure Variables

The module structure encourages the development of reusable software components. (The philosophy of software components is simple: it is easier to use an existing program than it is to write one from scratch!) A common problem with software components is that they are often difficult to tailor to the needs of client modules. For instance, one client may want a library module to perform its own error handling, while another client of the same module may want to substitute different error-handling routines.

Modula-2 addresses this problem by introducing the concept of *procedure variables*, a generalization of Pascal's procedure parameters. Procedure variables are variables that are assigned procedures as values. Calling a procedure variable invokes the procedure assigned to it.

Procedure variables allow client modules to "plug" their own procedures into a library module. For instance, a client can plug an error-handling procedure into a library module; when the library module detects an error condition, it calls an internal procedure variable, in turn invoking the client's own error-handling procedure.

Another use of procedure variables is the definition of automatic initialization and termination sections for library modules. This enables a library module to start up and shut down its own resources independently of any client modules.

For example, a network-handler module might define an initialization procedure that performs the hardware operations necessary to hook itself up to a network; similarly, it would define a termination procedure to unhook the network connection. The network-handler module passes these procedures to the program loader, indicating that they are to be called when the module is first loaded into memory and when it is about to be released. Client modules are unaware of these actions; all they know is that the module gives them access to an open network connection.

Listing 3 shows how procedure variables can be used to implement error handling and initialization/termination sections in a network-handler module.

Machine Access

Because low-level system facilities are written as library modules, Modula-2 provides facilities for machine-level programming. Such facilities are by nature machine-dependent, so they may vary across

Listing 3: *In this example of procedure variables, the library module Network manages a network connection. Initialization and termination procedures are established by calling the procedure SetEnvelope imported from the loader (a module named Program). The initialization procedure is called when Network is first loaded; the termination procedure is called when it is about to be released from memory.*

The procedure SetHandler allows error handlers to be attached to open network nodes. (The type PROC is a predefined type denoting a parameterless procedure.) The client module NetWriter declares its own error-handling procedure and attaches it to the node variable by calling SetHandler. Note that Netwriter does not require error-checking code after every network operation, because the network module will automatically call NetWriter's error-handling procedure if a network error occurs.

```
DEFINITION MODULE Network;

  EXPORT QUALIFIED
    NODE, Open, Close, Send, Receive, SetHandler;

  TYPE NODE;

  PROCEDURE Open    (VAR n: NODE; device: CARDINAL);
  PROCEDURE Close   (VAR n: NODE);
  PROCEDURE Send    (n: NODE; ch: CHAR);
  PROCEDURE Receive (n: NODE; VAR ch: CHAR);

  PROCEDURE SetHandler (VAR n: NODE; handler: PROC);

END Network.
```

```
IMPLEMENTATION MODULE Network;

  FROM Program IMPORT SetEnvelope;

  ...

  TYPE NODE = POINTER TO RECORD
             HandleProc: PROC;    (* error handler procedure *)
             AccessMode: NetAccess;
             Buffer: ARRAY bufrange OF CHAR;
             ...
           END;

  PROCEDURE Send (n: NODE; ch: CHAR);
  BEGIN
    ...
    IF LostConnection THEN n^.HandleProc( ) END;
  END Read;

  ...
```

Listing 3 continued on page 392

Listing 3 continued:

```
PROCEDURE SetHandler (VAR n: NODE; handler: PROC);
BEGIN
  n^.HandleProc := handler;
END SetHandler;

PROCEDURE Startup;
BEGIN
  (* open network connection *)
END Startup;

PROCEDURE Shutdown;
BEGIN
  (* disconnect from network *)
END Shutdown;

BEGIN
  SetEnvelope(Startup, Shutdown);
END Network.
```

```
MODULE NetWriter;

  IMPORT Terminal;

  FROM Network IMPORT
    NODE, Open, Close, Send, SetHandler;

  PROCEDURE handler;
  BEGIN
    Terminal.WriteString("Network error!");
    HALT;
  END handler;

  VAR n1: NODE;
      ch: CHAR;

  CONST Copier = 121;

BEGIN
  Open(n1, Copier);
  SetHandler(n1, handler);
  ...
  Send(n1, ch)
  ...
  Close(n1);
END NetWriter.
```

Modula-2 implementations and should be avoided in programs designed for portability. Machine-level programming is usually isolated in a small number of modules to separate machine-specific from portable software.

The predefined type BITSET is defined as a set that fits in one machine word. Bitsets allow efficient bitwise manipulation of word quantities.

The predefined module SYSTEM exports the system-dependent identifiers WORD, ADDRESS, SIZE, TSIZE, and ADR. When the type WORD is used as a parameter type, it is compatible with any object occupying one word. When WORD is used as the base type of an unbounded array parameter (ARRAY OF WORD), the parameter is compatible with variables of any size or type, including records and sets. The type WORD allows for writing general-purpose routines that operate on variables of any type.

The type ADDRESS is compatible with the type CARDINAL (unsigned integer) and all pointer types. Arithmetic operators can be applied to variables of type ADDRESS, allowing pointer and address arithmetic. This is important for writing storage managers, especially since Modula-2 translates the standard procedures NEW and DISPOSE into calls to the low-level procedures ALLOCATE and DEALLOCATE. These procedures are usually imported from a standard storage-management module, but they can also be defined in other ways to allow different styles of storage management.

The functions SIZE(x) and TSIZE(t) return the size of variables and types. The function ADR(x) returns the memory address of variables.

Variables can be declared to reside at fixed memory addresses. This is useful for accessing memory-mapped device registers.

Type checking can be circumvented by using a type identifier as a *type-transfer function,* which converts the type of its parameter argument to the type of the function identifier. Type conversion is restricted to objects that occupy the same number of words.

Code procedures enable Modula-2 programs to directly access facilities provided by the underlying hardware or host operating system. A code procedure consists of a procedure heading followed by the reserved word CODE and a series of machine instructions; these instructions are substituted inline for each procedure call. The use of code procedures is generally restricted to low-level modules.

Listing 4 shows Modula-2's machine-level programming facilities in action.

Multiprocessing

Most modern systems-programming languages include multiprocessing facilities as part of the language. For instance, Modula-1 offers processes and semaphores, Ada includes tasks and rendezvous, and

Concurrent Pascal contains monitors. Modula-2 forgoes these higher-level multiprocessing models in favor of the simpler and lower-level *coroutine* concept.

Coroutines are procedures that execute independently but not concurrently. In a group of coroutines, only one coroutine executes at a time—the rest are inactive. Coroutines communicate by calling each other; in a coroutine call, the calling coroutine becomes inactive, and the called coroutine resumes execution.

Coroutine facilities exported by the module SYSTEM include the procedures NEWPROCESS, TRANSFER, and IOTRANSFER, and the type PROCESS.

The procedure NEWPROCESS (Procedure, Adr, Size, Coroutine) creates a new coroutine. The parameter Procedure specifies the procedure to be executed by the coroutine. The parameters Adr and Size specify an area of memory for the coroutine to execute in. The newly created coroutine is returned in the parameter Coroutine, which is a variable of type PROCESS.

Coroutine calls are performed with the procedure TRANSFER (with process variables Old and New). TRANSFER suspends the current coroutine, assigns it to the process variable Old, and then resumes execution of the coroutine previously assigned to the process variable New.

The procedure IOTRANSFER (with process variables Old and New, and integer value IntVect) allows coroutines to be used as interrupt handlers. IOTRANSFER initiates a coroutine call from Old to New; however, when the peripheral device specified by IntVect causes an interrupt, control is automatically transferred back to the interrupt-handling coroutine. Listing 5 shows how coroutines work as interrupt handlers.

Coroutines are appropriate for many common multiprocessing applications; however, when higher-level forms of process scheduling are needed (e.g., semaphores or message passing), they can be constructed in terms of coroutines and stored in library modules. Modula-2 thus has

Listing 4: *This program demonstrates Modula-2's machine-level programming facilities. The module MyStorage provides a very simple storage allocator: starting at memory address 0, it assigns successive memory words to dynamically allocated variables. Note that ALLOCATE accepts arguments of any pointer type and that any calls to NEW in this program are handled by the storage module.*

The variable Console is declared to reside at hexadecimal memory address FFE8. The variable Sneaky uses a type-transfer function to gain bitwise access to a 32-bit real number. The code procedure LoadByte provides direct access to the Apple Pascal p-code instruction LDB: it loads a byte from memory onto the P-machine evaluation stack. The procedure PrintHex accepts variables of any type as arguments. Inside PrintHex, the parameter is viewed as an array of words in the range 0 to HIGH(mem). HIGH is a standard function that returns the upper index of array parameters.

```
MODULE LowLevel;

  FROM InOut IMPORT WriteHex;

  MODULE MyStorage;
     EXPORT ALLOCATE;

     VAR HeapTop: ADDRESS;

     PROCEDURE ALLOCATE (VAR ptr : ADDRESS; size: CARDINAL);
     BEGIN
       ptr := HeapTop;
       HeapTop := HeapTop +  size;
     END ALLOCATE;

  BEGIN
    HeapTop := 0
  END MyStorage;


  VAR Console [0FFE8H]: BITSET;


  PROCEDURE LoadByte (base: ADDRESS; offset: CARDINAL): CARDINAL;
  CODE
     190; (* LDB p-code: gets base & offset off stack *)
  END LoadByte;


  PROCEDURE PrintHex (mem: ARRAY OF WORD);
  VAR i: CARDINAL;
  BEGIN
    FOR i := 0 TO HIGH(mem) DO WriteHex(mem[i], 0) END;
  END PrintHex;


  VAR  ch: CHAR;
       r: RECORD
            x,y,z: REAL;
          END;
       a: ARRAY [0..50] OF CARDINAL;

  TYPE SetReal = SET OF [0 .. 31];

  VAR  Sneaky: SetReal;

  BEGIN
    Sneaky := SetReal (1.0E-13);
    a[0] := LoadByte(3FFFH, 3);
    PrintHex(ch);
    PrintHex(r);
    PrintHex(c);
  END LowLevel.
```

Listing 5: *This program, which illustrates coroutines and interrupts, writes a continuous stream of "hos" to the screen, but an occasional "hi" pops up among the "hos."*

The main program creates the coroutines Hi and Ho, then transfers to Hi (suspending itself permanently). The first thing Hi does is execute IOTRANSFER, transferring control to Ho. Ho runs in a loop, continually writing "ho" out to the screen; however, when an interrupt occurs through interrupt vector 4, control is automatically transferred back to Hi. Hi writes out "hi," transfers back to Ho, and waits for the next interrupt. In this example, interrupt vector 4 might be triggered by typing a key on the keyboard. Interrupt-vector assignment varies on different systems.

```
MODULE HiHo;

  FROM SYSTEM IMPORT
    WORD, ADR, SIZE, PROCESS, NEWPROCESS, TRANSFER;

  FROM Terminal IMPORT WriteString, Writeln;

  CONST maxHiHo = 17;

  VAR i: CARDINAL;
      Hi, Ho, Main: PROCESS;
      A, B: ARRAY [1..200] OF WORD;

  PROCEDURE WriteHi;
  BEGIN
    LOOP IOTRANSFER(Hi,Ho,4);  (* intpt. vector = 4 *)
      WriteString("hi");
    END;
  END WriteHi;

  PROCEDURE WriteHo;
  BEGIN
    LOOP WriteString("ho");
      INC(i);
      IF i > maxHiHo THEN
        Writeln; i := 0;
      END;
    END;
  END WriteHo;

BEGIN  i := 0;
  NEWPROCESS(WriteHi, ADR(A), SIZE(A), Hi);
  NEWPROCESS(WriteHo, ADR(B), SIZE(B), Ho);
  TRANSFER(Main, Hi);
END HiHo.
```

the advantage of being able to provide most any kind of process scheduling (including none at all).

Miscellaneous Improvements

Modula-2 is more than just Pascal extended with modules, machine access, and multiprocessing. It also introduces the following changes to Pascal that simplify programming and improve program readability and efficiency, as shown in listing 6:

- Each structured statement has an explicit terminating symbol: UNTIL for the REPEAT statement, and END for the rest. This eliminates the need for Pascal's compound statement (i.e., BEGIN . . . END).
- Everywhere Pascal allows constants, Modula-2 allows constant expressions; for instance, TYPE a = ARRAY [0..$n-1$] OF CHAR.
- CASE statements can have subranges in their case constant lists (eliminating the need to specify each constant value); also, CASE statements have an (optional) ELSE part.
- Variant records use the same syntax as CASE statements.
- Functions can return any type, inluding records and arrays.
- Procedures can declare *unbounded* ("open") array parameters, which accept arrays of varying length.
- The symbols # and & are defined as synonyms for the often-used symbols < > and AND.
- The AND and OR Boolean operators skip the second operand if the expression value can be determined from the first operand. Conditional-expression evaluation simplifies the programming of many situations.
- The LOOP/EXIT statement allows for clear and efficient expression of loop-and-a-half constructs.
- The FOR statement has an optional BY part for specifying step values other than 1.

All characters in a Modula-2 identifier are significant, not just the first eight, allowing you to use long identifiers without having to worry about accidental aliasing. The capitalized reserved words stand out in larger programs, improving readability. Modula-2 enforces case sensitivity of identifiers to prevent identifier aliasing (e.g., MYIDENT being the same as myIdent).

Conclusion

Pascal is ill-suited for implementing systems software, yet its basic structure is sound enough that many have chosen to extend the language rather than abandon it. This has resulted in an irremediable Tower-of-Babel syndrome from which the only escape is a new and better language.

Other languages vie for this honor, notably C and Ada, but none can be demonstrated to be superior to extended Pascal. C has proven itself as a practical language, but it suffers from unreadability, lack of type checking, and inadequate separate compilation facilities. Ada is a jungle of intertwined features; one suspects it was designed as a challenge to compiler writers, not as a tool for software engineers.

With Modula-2, Niklaus Wirth has created the language that will replace Pascal. Modula-2 can express everything from device drivers and system software to libraries and ap-

Listing 6: *Modula-2 is more efficient and more readable than Pascal. The example shows a piece of Pascal code and its Modula-2 equivalent. The Modula-2 code is two lines shorter and has one less variable reference and two fewer statements. Modula-2's conditional-expression evaluation eliminates the need for the second Pascal "if" statement. The standard procedure INC shortens the expression (and produces more efficient object code) by eliminating the second reference to the variable accountbalance.*

```
(*   PASCAL    *)

     if p <> NIL then
       if p^.update then
         begin
           p^.accountbalance := p^.accountbalance + receipts * 2;
           p^.update := false;
         end;


(*   MODULA-2   *)

     IF (p # NIL) & p^.update THEN
       INC(p^.accountbalance, receipts * 2);
       p^.update := FALSE;
     END;
```

plication programs. Modula-2's module concept and improved syntax make it more readable than Pascal. Modula-2 is as simple as Pascal and is small enough to allow efficient program development on 8-bit microcomputers. Modula-2 has enough in common with Pascal that Pascal programmers are able to write Modula-2 programs in a matter of hours.

In short, Modula-2 contributes to the design of software systems what Pascal has contributed to the design of programs. It is indeed a worthy successor to Pascal. ■

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Where to Get Modula-2

The following organizations distribute Modula-2:

Institut für Informatik
ETH
CH-8092 Zurich
Switzerland

ETH Zurich is the university where Modula-2 was conceived. ETH distributes Modula-2 compilers for the PDP-11, 68000, 6809, and Lilith. Lilith is a high-speed personal computer with superior graphics, a mouse, and a bit-slice processor designed to execute M-code.

Modula Research Institute
950 North University
Provo, Utah 84604

MRI is a nonprofit research organization that builds Lilith computers and sells them to large organizations for about $15,000 apiece. Liliths include Modula-2 software developed at ETH.

Volition Systems
POB 1236
Del Mar, CA 92014

Volition Systems released the first commercial implementation of Modula-2. Volition's current Modula-2 system runs under the UCSD Pascal system; it is available for the Apple II, Apple III, Sage II, Scenic One, NCR ALP-2, TI 9900, and 8080/Z80-based systems. Modula-2 compilers for other processors and operating systems will be available in the near future.

Meet 1-2-3 – the remarkable new software package that puts more raw power at your fingertips than anything yet created for the IBM PC. 1-2-3 actually combines information management, spreadsheet, and graphing in one program that can perform all three functions interchangeably and instantly at the touch of a key. That's power.

To explain: since 1-2-3's information management, spreadsheet and graphing functions reside in memo y simultaneously, you can go from retrieval to spreadsheet calculation to graphing instantly, just by pressing a few keys. So now you can experiment and recalculate and look at data in an endless variety of ways. As fast as your mind can think up new possibilities. There's no lag between you and the computer. And that's a new kind of power – power that's greater than the sum of its programs.

The spreadsheet function.

If 1-2-3 were just a spreadsheet, you'd want it because it has the largest workspace on the market (2048 rows by 256 columns). To give you a quick idea of 1-2-3's spreadsheet capabilities: VisiCalc's spreadsheet for the IBM PC offers 15 arithmetic, logical and relational operators, 28 functions and 32 spreadsheet-related commands. 1-2-3 has 15 operators, 41 functions and 66 commands. And if you include data base and graphing commands, it actually has 110!

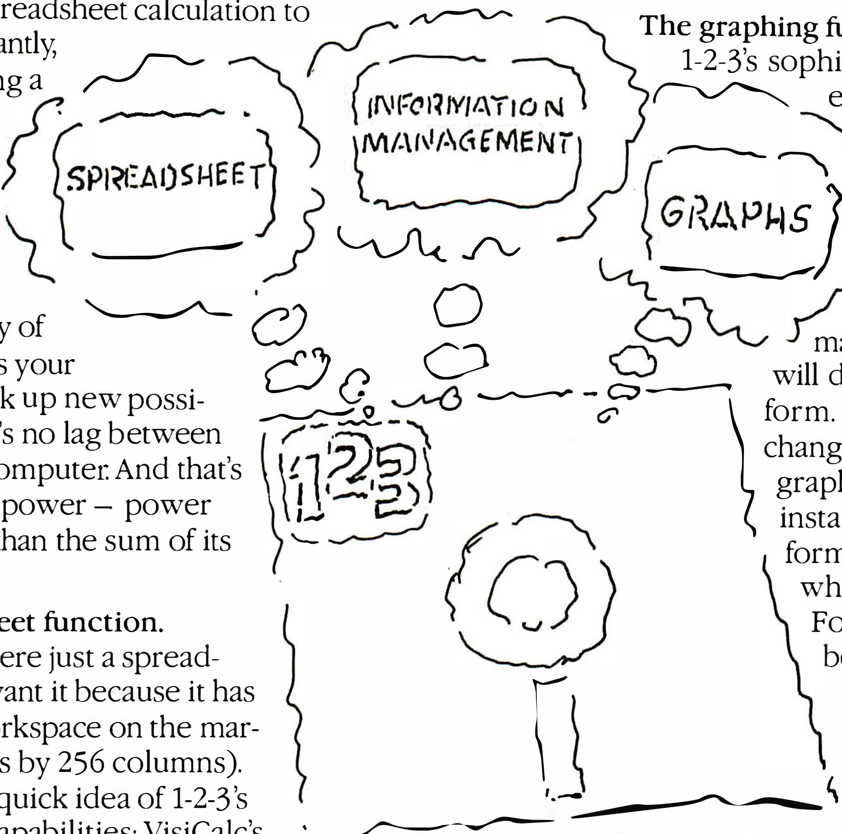
In addition, 1-2-3 is up to 50 times as fast as established spreadsheets. With all the features you've ever seen on spreadsheets. 1-2-3 also gives you the capability to develop customized applications (with 26 macro keys) and lets you perform repetitive tasks automatically with one keystroke. If 1-2-3 were just a spreadsheet, it would be a very powerful tool. But it's much, much more.

The information management function.

Add to 1-2-3's spreadsheet a selective information management function, and the power curve rises at an awesome rate. Particularly since 1-2-3's information management capability reads files from other programs such as WordStar, VisiCalc and dBase II. So you can accumulate information on a limitless variety of topics and extract all or pieces of it for instant spreadsheet analysis. Unheard of before. Specific 1-2-3 information management features include sorting with primary and secondary keys. Retrieval using up to 32 criteria. 1-2-3 performs statistical functions such as mean, count, standard deviation and variance. It can produce histograms on part or all of the data base. 1-2-3 also allows for the maintenance of multiple data bases and multiple criteria.

The graphing function.

1-2-3's sophisticated graphing commands enable you to create graphs of up to six variables using information already on the spreadsheet. And have it on screen in less than two seconds! Once you've made a graph, three keystrokes will display it in a different form. If data on the spreadsheet changes, you can display a revised graph with one keystroke. This instant relationship of one format to another opens up a whole new application area. For the first time graphics can be used as a "what if" thinking tool!



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The Design of an Advanced Logic Simulator

Macrocircuits and time-saving features make this new version easy to use.

Robert M. McDermott
33 Dora Circle
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In a previous article ("Simulation of Simple Digital Logic through a Computer-aided Design System," January 1983 BYTE, page 396), I described the design of a primitive logic simulator to replace hardware breadboarding in learning to design basic digital circuits. I also outlined enhancements that could give the program functions comparable to professional-level simulators available on large mainframe computers. After finding how easy it was to write a logic simulator for Radio Shack's TRS-80, I endeavored to write a professional-level program. This article includes the program and describes in detail the operation of the enhancements. While the description is oriented toward the logic simulator, the basic concepts employed could be used in other applications as well, particularly the processing of macroinstructions and the use of selective trace for event-driven phenomena.

Background

As described in the previous article, a logic simulator accepts the description of a proposed design in terms of logic-element interconnections and external stimuli. It applies the external stimulus to the simulated logic network and displays the resultant output.

A macrocircuit is a black box with specified input and output signals.

The simulator operates by keeping track of the states of all connection nodes. An *old* (before stimulus) state is used as the input to each simulated logic device, and results are stored as *new* state; once all devices have been stimulated using the old values as inputs, the new values replace the old and the process is repeated. This operation implies that every logic element produces the same delay. This fixed delay allows for the modeling of sequential devices because feedback loops work properly.

The propagation of signals among the various logic elements is controlled by a description of the logic network, consisting of a list of each element's logic type and the nodes to which the element's input and output are connected. The appearance of one node as the output of one element and the input to another element implies that the output and input are electrically connected. Node numbers serve as an index to an array that contains the logic values (old and new) for each signal.

The primitive version of this program was a direct implementation of this concept that merely filled the appropriate arrays directly from the input provided and proceeded to simulate the design in a single-step manner. The logic primitives supported were the standard logic operators: AND, NAND, OR, NOR, and XOR. This basic approach, while simple to implement, left much to be

About the Author
Robert M. McDermott is the manager of CAD (computer-aided design) software engineering at International Telephone and Telegraph's Large-Scale Integration Technology Center. The recipient of both BEE and MS degrees, he also teaches computer science at Bridgeport Engineering Institute.

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desired in terms of ease of use, error checking, and models of commonly used higher-level logic elements (flip-flops, counters, etc.).

A more professional system is shown in listing 1 (see page 428) and diagramed in figures 1 and 2; it supports named nodes rather than numbers, a "macro" capability for repetitiously used blocks of circuitry, an expanded library of logic primitives (see figures 3 and 4), procedures for rapid simulation, and a flexible output-display feature.

Named Nodes

Most nodes in a proposed design have functional names associated with them (e.g., Clock, Reset, etc.). For ease of use and a more meaningful input description, a well-designed program must support the use of named nodes. It is much easier to debug a design described by lines such as

```
AND DATA LOAD    DATA-IN
```

rather than

```
AND 3      7         33
```

The advanced version of this program uses a free-field input format. Spaces are used as string delimiters when a line is read and parsed into distinct names by the subroutine at line 10000. A table look-up assigns unique numbers to each signal name. The subroutine at line 11500 looks up each name, while the routine at line 11600 adds to the list names not already there. Note that unused entries have the name "0," and this is the only reserved signal name; any other combination of symbols can be used as a valid signal name (e.g., LOAD— could be used to signify a load-not signal). Additionally, some devices subsequently described contain numeric parameters, such as an N-bit shift register, and these numbers are distinguished from signal names by using # (the number sign) as the first character in the name.

Macrocircuit Capability

To support structured design, and to make entering input data easy,


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(1a) (1b)

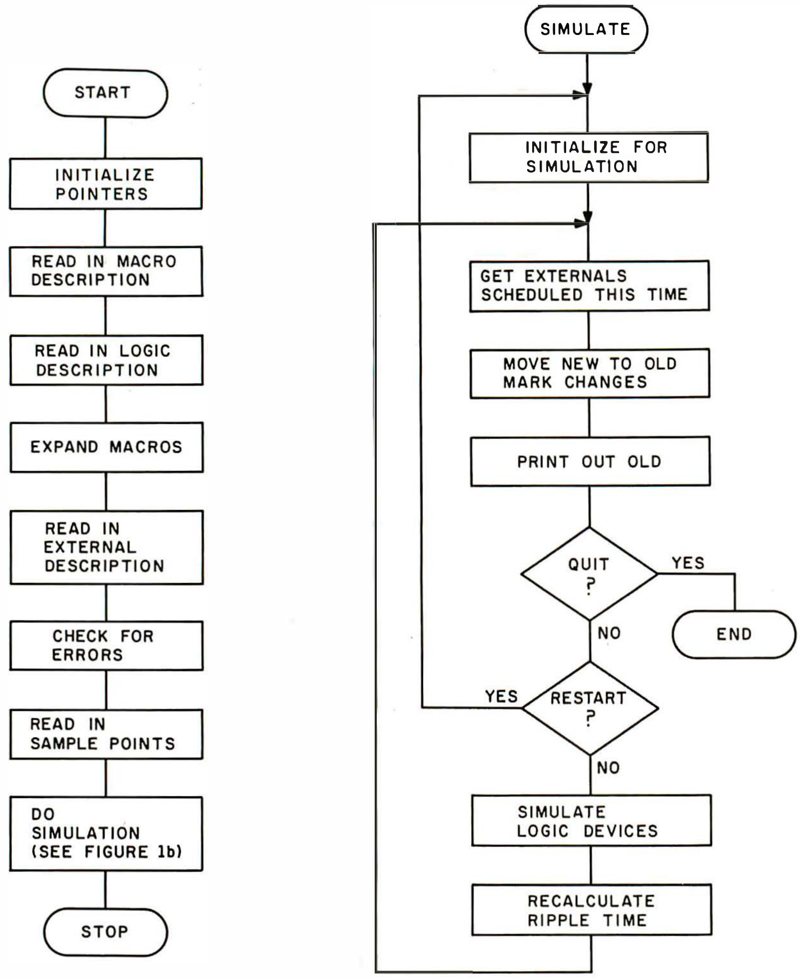


Figure 1: *Flowchart of the fundamental procedures used in the simulator. Figure 1a shows the arrangement of the functional blocks; figure 1b describes in more detail the actual simulation process.*

capability should be included to allow predefined blocks of circuitry—macrocircuits—to be installed simply. A macrocircuit is a black box with specified input and output signals; the description of the macrocircuit includes the logic devices required to generate the output from the inputs, using internal

A macrocircuit is similar to a function call in BASIC or a subroutine call in FORTRAN or Pascal.

signals as required. Handling a single-level macrocircuit involves the replication of a block of logic devices, with the appropriate translation of the signal names used within the macrocircuit to those used within the circuit.

A macrocircuit is similar to a FUNCTION call in BASIC (or more appropriately, a subroutine call in languages such as FORTRAN or Pascal). The definition of the macrocircuit is like BASIC's DEFFN definition in that the variables used in the definition are dummy variables. When the macrocircuit is called in the logic-description input, the dummy

Text continued on page 412

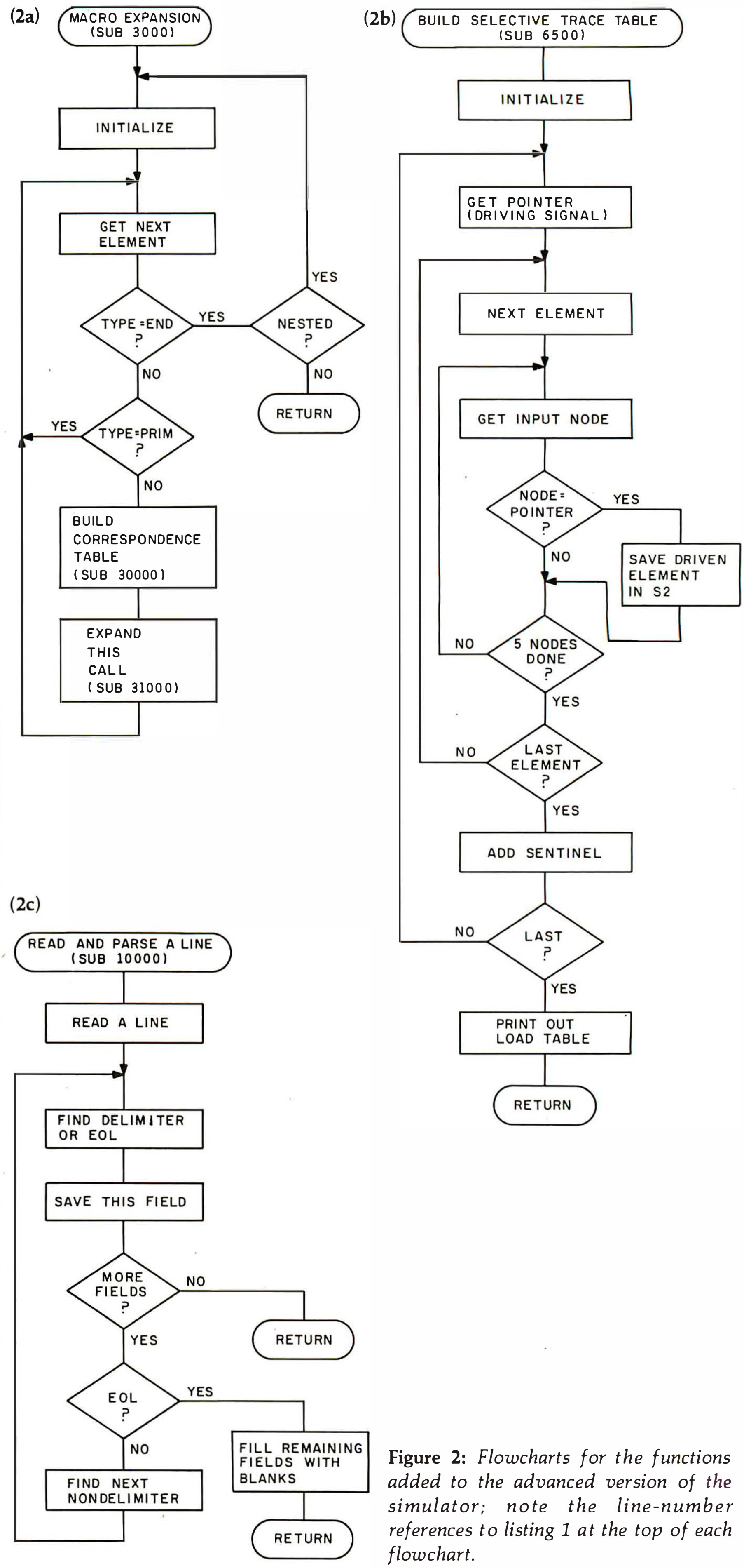
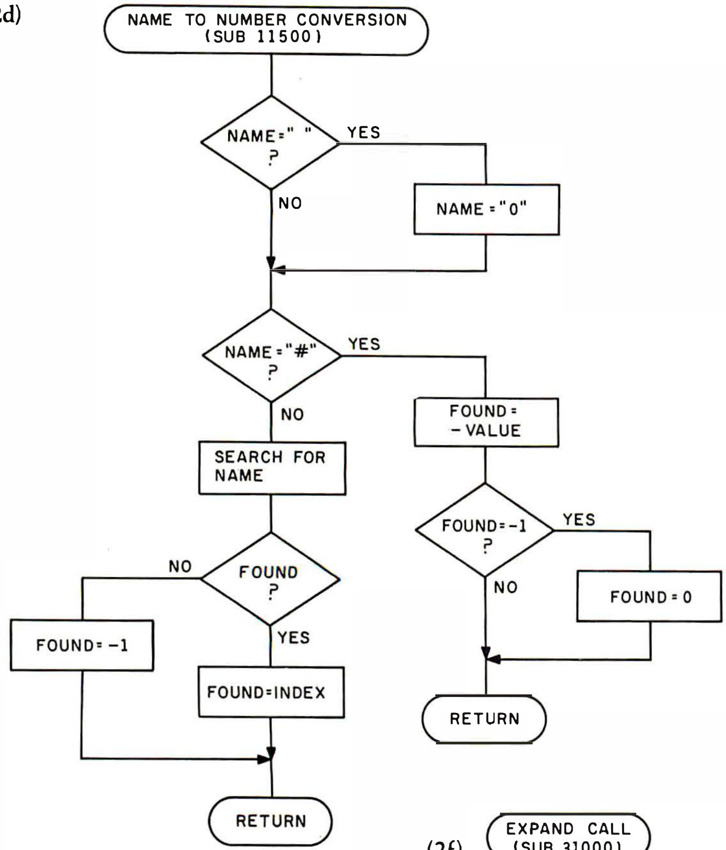
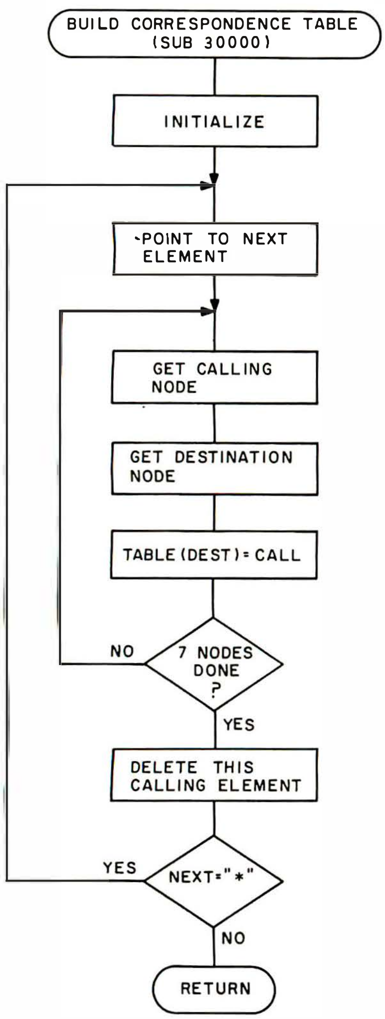


Figure 2: *Flowcharts for the functions added to the advanced version of the simulator; note the line-number references to listing 1 at the top of each flowchart.*

(2d)


NAME TO NUMBER CONVERSION (SUB 11500)
NAME=" " ?
YES
NO
NAME="0"
NAME="#" ?
YES
NO
FOUND= -VALUE
SEARCH FOR NAME
FOUND=-1 ?
YES
NO
FOUND=0
FOUND ?
NO
YES
FOUND=-1
FOUND=INDEX
RETURN
RETURN

(2e)


BUILD CORRESPONDENCE TABLE (SUB 30000)
INITIALIZE
POINT TO NEXT ELEMENT
GET CALLING NODE
GET DESTINATION NODE
TABLE (DEST) = CALL
7 NODES DONE ?
NO
YES
DELETE THIS CALLING ELEMENT
NEXT="*"
YES
NO
RETURN

(2f)

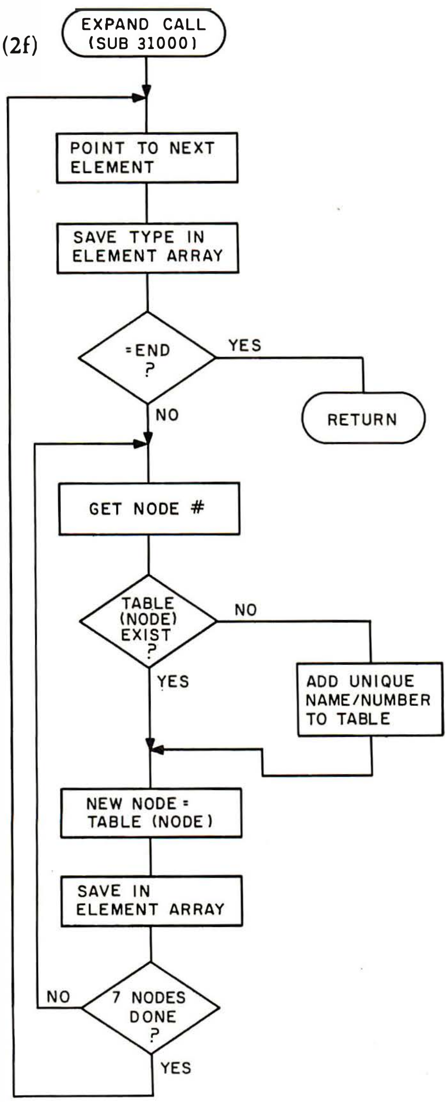

EXPAND CALL (SUB 31000)
POINT TO NEXT ELEMENT
SAVE TYPE IN ELEMENT ARRAY
=END ?
YES
NO
RETURN
GET NODE #
TABLE (NODE) EXIST ?
NO
YES
ADD UNIQUE NAME/NUMBER TO TABLE
NEW NODE = TABLE (NODE)
SAVE IN ELEMENT ARRAY
7 NODES DONE ?
NO
YES

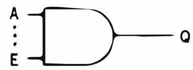
Figure 3: *The fundamental logic elements predefined within the logic simulator.*

(3a)

LOGIC TYPE: AND GATE

LOGIC EQUATION: $Q = A \cdot (B) \cdot (C) \cdot (D) \cdot (E)$

LOGIC SYMBOL:



TRUTH TABLE:

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

ELEMENT CODING: AND A (B) (C) (D) (E) Q $(\overline{Q})$

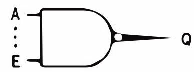
NOTES: ( ) DENOTES OPTIONAL FIELDS, "0" IF NOT USED.

(3b)

LOGIC TYPE: NAND GATE

LOGIC EQUATION: $Q = \overline{A \cdot (B) \cdot (C) \cdot (D) \cdot (E)}$

LOGIC SYMBOL:



TRUTH TABLE:

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

ELEMENT CODING: NAND A (B) (C) (D) (E) Q $(\overline{Q})$

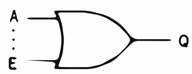
NOTES: ( ) DENOTES OPTIONAL FIELDS, "0" IF NOT USED.

(3c)

LOGIC TYPE: OR GATE

LOGIC EQUATION: $Q = A + (B) + (C) + (D) + (E)$

LOGIC SYMBOL:



TRUTH TABLE:

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

ELEMENT CODING: OR A (B) (C) (D) (E) Q $(\overline{Q})$

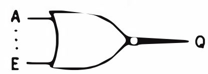
NOTES: ( ) DENOTES OPTIONAL FIELDS, "0" IF NOT USED.

(3d)

LOGIC TYPE: NOR GATE

LOGIC EQUATION: $Q = \overline{A + (B) + (C) + (D) + (E)}$

LOGIC SYMBOL:



TRUTH TABLE:

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

ELEMENT CODING: NOR A (B) (C) (D) (E) Q $(\overline{Q})$

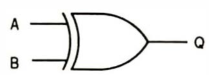
NOTES: ( ) DENOTES OPTIONAL FIELDS, "0" IF NOT USED.

(3e)

LOGIC TYPE: EXCLUSIVE OR GATE

LOGIC EQUATION: $Q = A \oplus B$

LOGIC SYMBOL:



TRUTH TABLE:

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

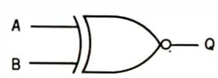
ELEMENT CODING: XOR A B 0 0 0 Q $(\overline{Q})$

(3f)

LOGIC TYPE: EXCLUSIVE NOR GATE

LOGIC EQUATION: $Q = \overline{A \oplus B}$

LOGIC SYMBOL:



TRUTH TABLE:

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

ELEMENT CODING: XNOR A B 0 0 0 Q $(\overline{Q})$

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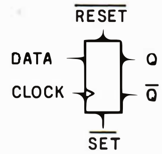


Figure 4: *Additional logic elements predefined within the advanced version of the logic simulator.*

(4a)

LOGIC TYPE: D-TYPE FLIP-FLOP

LOGIC SYMBOL:



TRUTH TABLE:

DATA	CLOCK	$\overline{RESET}$	$\overline{SET}$	Q	$\overline{Q}$
X	X	0	0	0	1
X	X	1	0	1	0
X	X	0	1	0	1
0	↑	1	1	0	1
1	↑	1	1	1	0
X	↓	1	1	Q	$\overline{Q}$

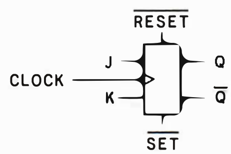
ELEMENT CODING: OFF DATA 0 CLOCK ($\overline{RESET}$) ($\overline{SET}$) Q ($\overline{Q}$)

NOTES: X = DON'T CARE.
SET AND RESET ARE ACTIVE LOW; IF UNUSED "0", THEY DEFAULT TO LOGIC 1.

(4b)

LOGIC TYPE: JK FLIP-FLOP

LOGIC SYMBOL:



TRUTH TABLE:

J	K	$\overline{SET}$	$\overline{RESET}$	Q	$\overline{Q}$	CLOCK	NEXT Q	NEXT $\overline{Q}$
1	X	1	1	0	1	↑	1	0
X	0	1	1	1	0	↑	1	0
0	X	1	1	0	1	↑	0	1
X	1	1	1	1	0	↑	0	1
X	X	1	1	X	X	↓	NO CHANGE	
X	X	0	1	X	X	X	1	0
X	X	1	0	X	X	X	0	1
X	X	0	0	X	X	X	0	1

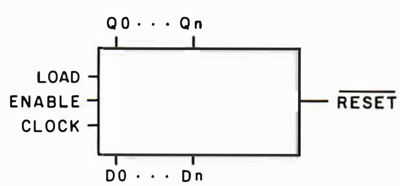
ELEMENT CODING: JKFF J K CLOCK ($\overline{RESET}$) ($\overline{SET}$) Q ($\overline{Q}$)

NOTES: X = DON'T CARE.
SET AND RESET ARE ACTIVE LOW; IF UNUSED "0", THEY DEFAULT TO LOGIC 1.

(4c)

LOGIC TYPE: N-BIT COUNTER

LOGIC SYMBOL:



TRUTH TABLE:

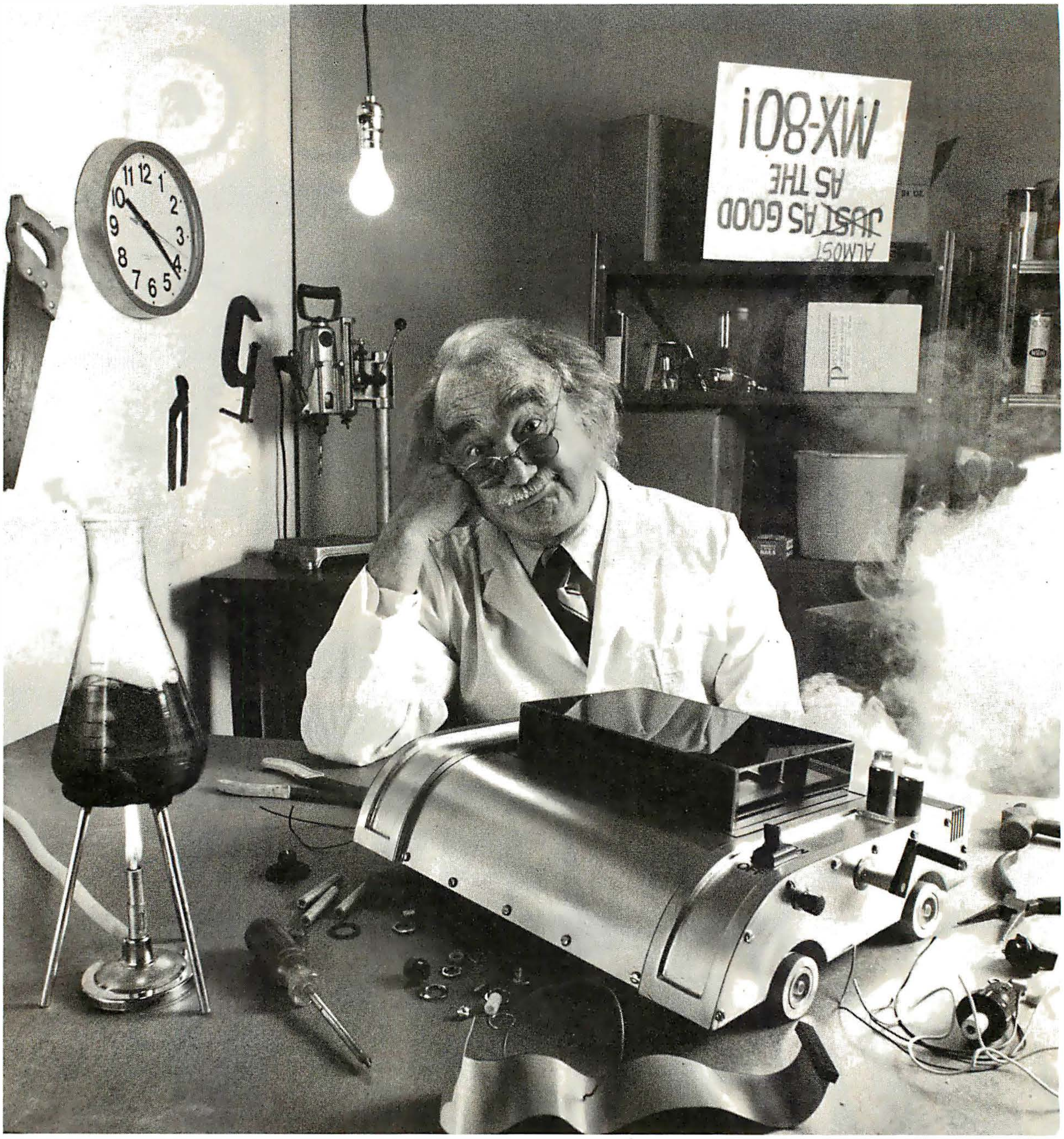
DATA	LOAD	ENABLE	$\overline{RESET}$	CLOCK	COUNT (Q0...QN)
0	1	X	1	↑	0
1	1	X	1	↑	1
X	0	X	0	X	0
X	0	1	1	↑	COUNT + 1
X	0	1	1	↑	NO CHANGE
X	0	0	1	↑	NO CHANGE

ELEMENT CODING:

CNTR	(D0)	ENABLE	CLOCK	(LOAD)	($\overline{RESET}$)	Q0	($\overline{Q0}$)
*	(D1)	0	0	0	0	Q1	($\overline{Q1}$)
*	.	0	0	0	0	.	.
*	Dn					Qn	($\overline{Qn}$)

NOTES: X = DON'T CARE. LOAD AND ENABLE ARE ACTIVE HIGH AND LOAD OVERRIDES ENABLE.

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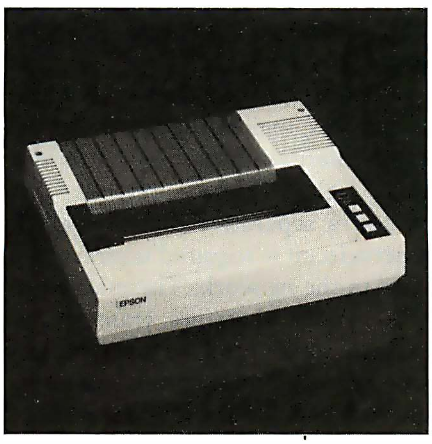
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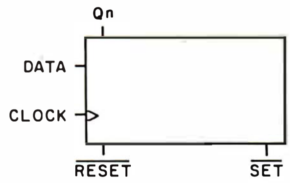
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(4d)

LOGIC TYPE: N-BIT SHIFT REGISTER

LOGIC SYMBOL:



TRUTH TABLE:

DATA	$\overline{RESET}$	$\overline{SET}$	CLOCK	Q1	Qn
0	1	1	↑	0	Qn −1
1	1	1	↑	1	Qn −1
X	1	1	↓	Q1	Qn NO CHANGE
X	0	1	X	0	0
X	1	0	X	1	1

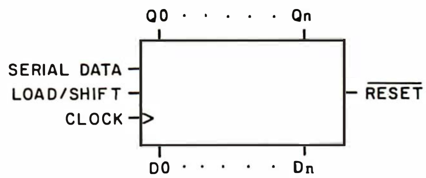
ELEMENT CODING: SREG DATA #BITS CLOCK ($\overline{RESET}$) ($\overline{SET}$) Qn ($\overline{Qn}$)

NOTES: #BITS IS THE TOTAL NUMBER OF SHIFT BITS REQUIRED. IF "0", THEN DEFAULTS TO 1.
X = DON'T CARE.

(4e)

LOGIC TYPE: PARALLEL LOAD SHIFT REGISTER

LOGIC SYMBOL:



TRUTH TABLE:

D0	DSER	LOAD	$\overline{RESET}$	CLOCK	Q0	Qn
X	X	X	0	X	0	0
1	X	1	1	X	1	1
0	X	1	1	X	0	0
X	0	0	1	↑	0	Qn-1
X	1	0	1	↑	1	Qn-1

ELEMENT CODING:

PLSR	D0	DSER	CLOCK	LOAD	($\overline{RESET}$)	Q0	($\overline{Q0}$)
*	D1	0	0	0	0	Q1	($\overline{Q1}$)
*	Qn	0	0	0	0	Qn	($\overline{Qn}$)

NOTES: X = DON'T CARE
LOAD/SHIFT- LOAD ON HIGH, SHIFT ON LOW.

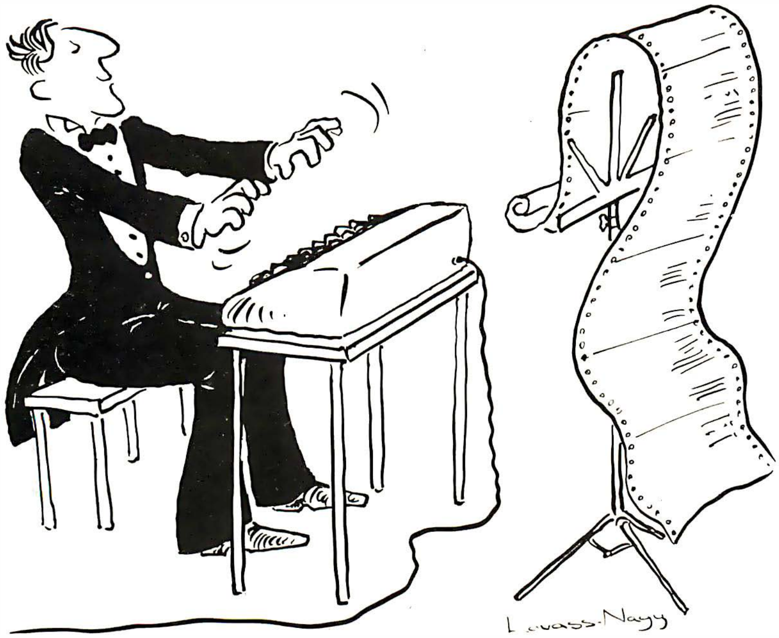
Text continued from page 402:

signal names are replaced by the signal names used in the actual network description.

A macrocircuit typically performs a complex logical function. Because some internal nodes may be used to hold values from previous time cycles, a separate replication of the macrocircuit is required wherever it is used in the network. The macro processor must therefore translate the defined inputs and outputs of each macrocircuit and generate unique signal numbers for the internal nodes.

A macrocircuit can be considered as a subcircuit; typically, a complex but common logical function is designed and simulated as a single circuit to verify its proper operation. Once this design is characterized with regard to the input and output pins, it can be used as a building block for other designs. This approach is comparable to structured programming, where a functional block is completely characterized by the arguments passed to and returned from it.

Because a macrocircuit is conceptually a subcircuit, the same routine used to read the logic circuit (at line 2000) is used to process the macrocircuit. Pointers are maintained to keep track of where in the logic-description array each macrocircuit starts. The NAME$ array is reused because the names used in each macrocircuit are



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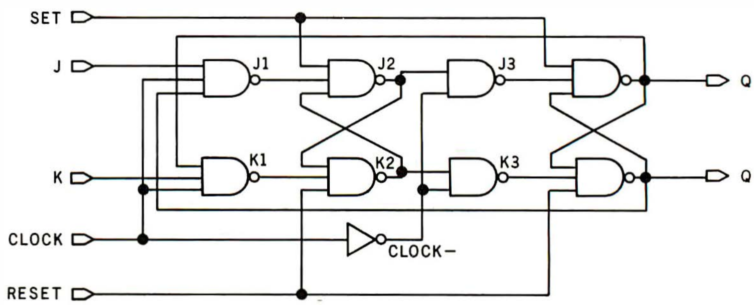
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JK FLIP-FLOP MACRO




```
*****   READING IN MACRO: JK

JK  J K CLOCK RSET SET Q Q-
NAND J CLOCK Q- 0 0 J1 0
NAND K CLOCK Q 0 0 K1 0
NAND SET J1 K2 0 0 J2 0
NAND RSET K1 J2 0 0 K2 0
NAND J2 CLOCK- 0 0 0 J3 0
NAND K2 CLOCK- 0 0 0 K3 0
NAND J3 Q- 0 0 0 Q 0
NAND K3 Q 0 0 0 Q- 0
NAND CLOCK 0 0 0 0 CLOCK- 0
END 0 0 0 0 0 0 0
```

***** EXPANDED LOGIC DESCRIPTION *****

TYPE	INPUTS 1	2	3	4	5	OUTPUTS Q	Q-
NAND	J1	CLOCK1	Q0-			&8	
NAND	K1	CLOCK1	Q0			&9	
NAND	SET	&8	&10			&11	
NAND	RESET	&9	&11			&10	
NAND	&11	&12				&13	
NAND	&10	&12				&14	
NAND	&13	Q0-				Q0	
NAND	&14	Q0				Q0-	
NAND	CLOCK1					&12	
END							

Figure 5: *Defining a macrocircuit. Using predefined logic elements, the JK flip-flop shown here can be described to the logic simulator once, then that description can be used wherever a flip-flop is needed; the user is not required to define the device every time it is used. (Multilevel or nested macros are also allowed.)*

dummy names and need not be retained after the macrocircuit's description is stored.

The use of a macrocircuit is demonstrated in figure 5. The logic coding for a JK flip-flop was described in the January article; once its proper operation is verified, it can be used as a macrocircuit. Using the black-box approach, the user need provide only the J, K, Clock, Reset, and Set inputs and name the Q and Q− outputs. The macro processor, however, must assign unique signal numbers to the internal nodes wherever this JK flip-flop is used.

Nested macrocircuits (a macrocircuit used within a macrocircuit) add a further level of complexity in this signal-translation and node-generation procedure. One approach typically taken is to maintain a list of the defined signals on a stack and push and pop the signal names as macrocircuits are called and expanded. This procedure is efficient in that macrocircuits can be expanded as they are encountered, but typically requires either large memory for the stack or a limit to the nesting depth.

A procedure that allows for unlimited nesting depth requires multiple passes through the logic-description array: one pass to expand each level of macrocircuit. This procedure is not processor-time efficient, but the signal names need be stored only once for cross-referencing to a single macro call at any one time. One example of a nested macro would be when a 4-bit ripple counter is defined as a macrocircuit containing the JK flip-flop macrocircuit.

The macro expander (at line 3000) must perform two tasks: maintaining correspondence to the simulated circuit's signal names and generating unique signal names for other internal nodes. This process is performed by maintaining a macro-to-logic corre-

spondence array; because the array used to store old logic values is not needed at this point, this array is used to maintain this correspondence, thus conserving memory.

The subroutine at line 30000 builds this correspondence by placing the calling signal number in the array position pointed to by the macrocircuit signal number; all other entries are set to a −1 to indicate that no correspondence has yet been made. This correspondence is location-dependent, i.e., the location of a calling signal within the calling description corresponds to a signal in the same location in the macrocircuit's definition line (the first input in the call corresponds to the first input to the macrocircuit definition, etc.).

The subroutine at line 31000 is called to expand the called macrocircuit and add it to the end of the logic-description array. If a macrocircuit name has no correspondence to a calling name, a unique number is assigned, as well as a reference name. As each macrocircuit is expanded, the calling entry in the logic-description array is deleted by moving the array up to overwrite the calling entry. The logic-description array is repeatedly scanned for macrocircuit calls, and the above process continues until no macrocircuit calls are found.

Error Checking

The basic error checking that should be performed consists of checking that a name is not used as the output of two or more logic elements and that each named input signal is defined as either an external stimulus or the output of a logic element. These checks are applicable for macrocircuit blocks, as well as for the total expanded logic description; although an error in a macrocircuit block will be found when the total network is checked, it is easier to debug an error if its location can be easily isolated. Each macrocircuit expansion involves a separate error check (at line 1500), and the total circuit is checked after expansion (at line 5000).

The check for multiple definitions of an output is performed by scanning the element-description array for the same signal number on two or more outputs. Rather than compare each output with every other output (requiring $N \times (N-1)/2$ comparisons), a single pass through the logic-description array can identify multiple uses of the same signal. The OL array (see line 12200) is used to mark the occurrence of a signal number as an output of a logic device or as an external stimulus; if a signal is already marked, it is flagged as an error.

This same marked array is then used to check for defined inputs (at line 12300); the logic array is scanned and each input is checked for a 0 in the OL array as being undefined. Additionally, for defined signals, this entry is incremented for each occurrence of the signal as an input, providing for an indication of the load on each signal. This count is also used to determine the array requirements for selective trace, as described in the



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next section.

As each error is reported, the user is given the option to have the program ignore the error and continue with simulation. This is particularly useful when a signal appears both as the output of a logic element and as an external stimulus for initialization.

Selective Trace

A logic element's output state will not change unless a change appears at its input; this fact can be used to optimize run-time by simulating an element only when such a change occurs. On a global scale, no element need be simulated until an external stimulus is applied.

The global optimization can be easily implemented by maintaining a single *change flag* used to skip the entire simulation process when no changes are noted. Additionally, if the next scheduled stimulus change time is known, the simulator clock (ripple time) can be automatically advanced to that point, skipping the intermediate (inactive) time steps. The variables C9 (change flag), E9 (next scheduled stimulus time), and S9 (next scheduled sample time) are used to determine RI (next scheduled ripple time) in the subroutine at line 7500.

Optimization at the logic-element level (selective trace) is slightly more complicated. A flag must be maintained for each logic element; the flag is set when one or more of the element's inputs changed state during the previous simulation cycle. A cross-reference array must be maintained to identify which logic elements are affected by each output signal; conceptually, an array is required where one dimension represents the logic elements and the other dimension is the number of signal nodes.

This array contains a 1 if the element is driven by the corresponding node; otherwise, it contains a 0. This array would contain primarily 0s, because few nodes would fan out to more than a few logic elements; as such, sparse-matrix techniques are used to minimize the memory requirements for such processing.

The S0, S1, and S2 arrays are used to perform this sparse-matrix tracing and marking. S0 contains the flag for each logic element; S1 is arranged by signal number and points to entries in S2 (which contains the list of elements driven by each signal number—the drive table). On entry to the routine that builds these arrays, a check is made to see that sufficient memory remains to store these values; because selective trace is not necessary for simulation, if sufficient memory is not available, this process is skipped entirely and the ST (selective-trace flag) is cleared.

The subroutine at line 6500 creates the drive table; this table is, in effect, a form of a linked list. Because the length of the list of elements driven by a particular signal is of variable size, this list is dynamically allocated and uses a delimiter to mark the end of the list for each signal (the next entries in the array are the list of elements driven by the next signal).

During simulation, as the output signals are moved from the NEW to the OLD array, a check is made to see if a change has occurred on a signal (at line 8500); if so, C9, the global-change flag, is set (as are the change flags of the elements driven by this signal if the selective-trace flag is set—see the subroutine at line 8620). The simulation of the logic elements is skipped entirely if the global-change flag is not set (line 40010); and, if the selective-trace flag is set, each element's simulation is skipped if its individual-change flag (in array S0) is not set (line 40030). The global optimization can produce a twofold to fivefold decrease in processing time, and the element-level selective trace another twofold to tenfold decrease, depending upon the relative activity of the logic network.

Sampled Output

The primitive version of this program produced a display of each selected logic signal at each simulation cycle. To get a more global view of the operation of the logic network, however, it is often desirable to display the outputs at periodic intervals rather than at each cycle. This is comparable to the sweep control on an oscilloscope. In the simulation of a

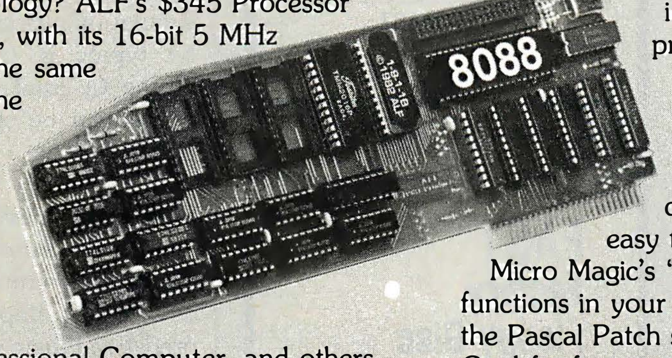
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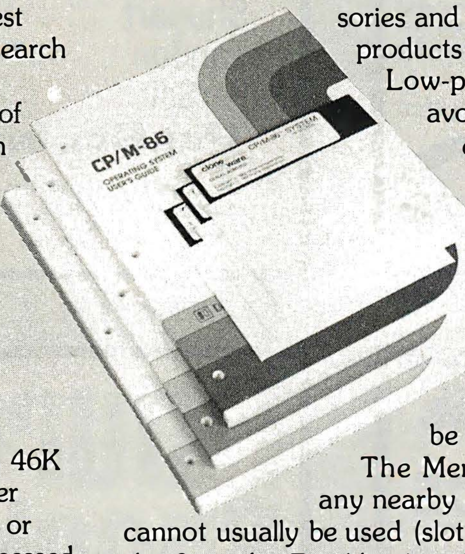
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counter, for example, it is often desirable to display the resultant count at each clock cycle rather than at each gate-simulation cycle.

This option is directly implemented by specifying the start time and the sampling interval. For every simulation cycle, the subroutine at line 9000 checks to see if a sample is required (RI=S9), and if so, displays the values. It also increments S9 for the next scheduled time and checks for a full screen. If the screen is full (50 samples displayed), the user is given options for continued processing. The simulation process can be reinitialized by typing R (restart), aborted by typing Q (quit), or the monitored points can be changed by typing C (change).

Sequential-Device Models

A logic simulator for advanced digital design must include sequential devices (flip-flops, counters, etc.) as predefined logic primitives. While sequential devices can be modeled as macrocircuits of the basic logic elements, such modeling is inefficient (requiring, for example, nine combinational devices to model a single JK flip-flop).

The combinational models previously described (AND, OR, XOR gates) each have inputs that are congruent; i.e., for a 2-input AND gate, it doesn't matter which signal is given as the first pin and which as the second. For sequential devices, however, each input has a specific function; i.e., the Clock pin operates differently from the J input pin on a JK flip-flop. To maintain this "pin significance," each sequential model uses a fixed order of signal pins in the input description shown in figure 4; in the JK flip-flop model, for example, the first input signal will be interpreted to be the J input, the second the K, third Clock, fourth Reset, and fifth Set. This assignment is used directly by the sequential models to accurately simulate the operation of these devices; in all cases, the devices are triggered on the *rising edge* of the clock and contain optional asynchronous, active-low Set and Reset pins.

The use of sequential devices as

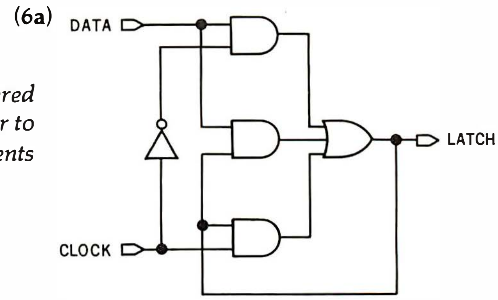
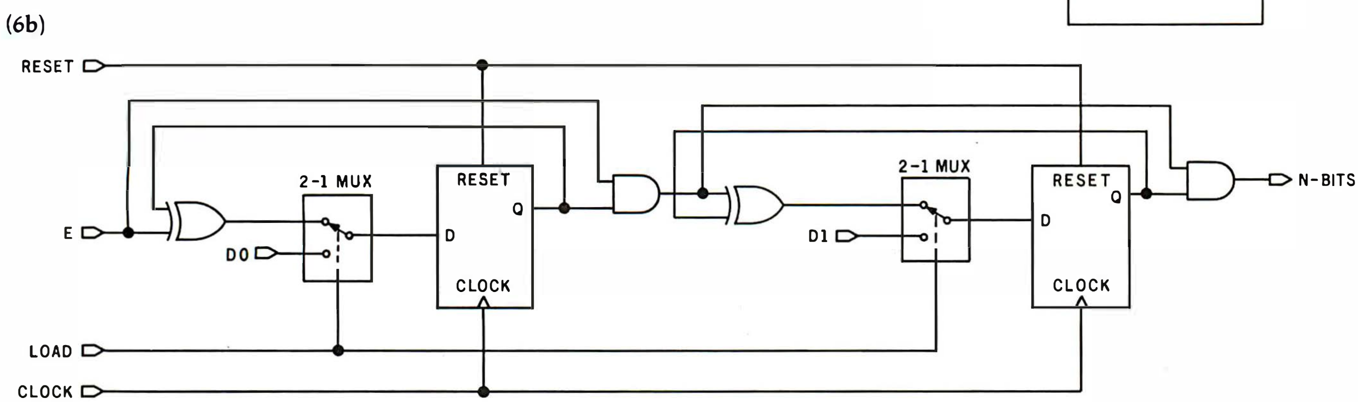


Figure 6: *Models of sequential devices. Figure 6a shows a level-sensitive, edge-triggered latch used in simulation of more complex devices. A parallel-loading counter (similar to a 74LS163) is modeled in figure 6b. Each stage is a combination of some logic elements and a shift register.*



primitives requires that such devices be predefined. Thus, we must address the fact that sequential devices, by definition, contain some memory of their prior state. For example, the operation of a counter is dependent upon its prior count, as well as its immediate inputs. Each logic element in the program includes an array position for maintaining this memory value (or a pointer to another array for maintaining multiple memory values).

Each of the sequential devices described herein is a level-sensitive, edge-triggered device. When the clock goes to a logic 1, the resultant output is latched to the desired state; it cannot change value (except by asynchronous Set or Reset), except on the rising edge. Such a level-sensitive, edge-triggered operation is typically designed by using dual latches on opposing clock values. When the clock is low, the input is latched to its appropriate value while the output retains its prior latched value; when the clock is high, the input latch is disabled from changes on the input and the output is driven by this internal latch value. Figure 6 shows such a latch; this logical model is used for simulation. Because the prior output value is available from the OLD array, the program need retain only the internal latch value for proper sequential modeling (this is the eighth entry in the logic-description array).

The subroutine at line 45000 performs the basic latch function (a 2-to-1 multiplexer); the subroutine at line 45100 performs the basic shift register function by two calls to the latch function, returning YL as the internal latch value and Y as the second (Q output) latch value. (The shift register function also calls the routine at line 45200 to process the asynchronous Set and Reset signals, if any.)

The model of a D-type flip-flop is merely a direct call to the shift register function; note that the optional Set and Reset pins are set to a default of logic 1 by presetting the 0 entry of the OLD array to a logic 1. If the signals are unused (signal number 0), this logic 1 is read as the current input (Set and Reset are active-low).

The model of a JK flip-flop is basically some combinational logic followed by a shift register. The internal D input should be the desired Q output upon receipt of an active clock edge; the combinational logic to generate the D input is

$$(J \text{ AND } \overline{Q}) \text{ OR } (\overline{K} \text{ AND } Q)$$

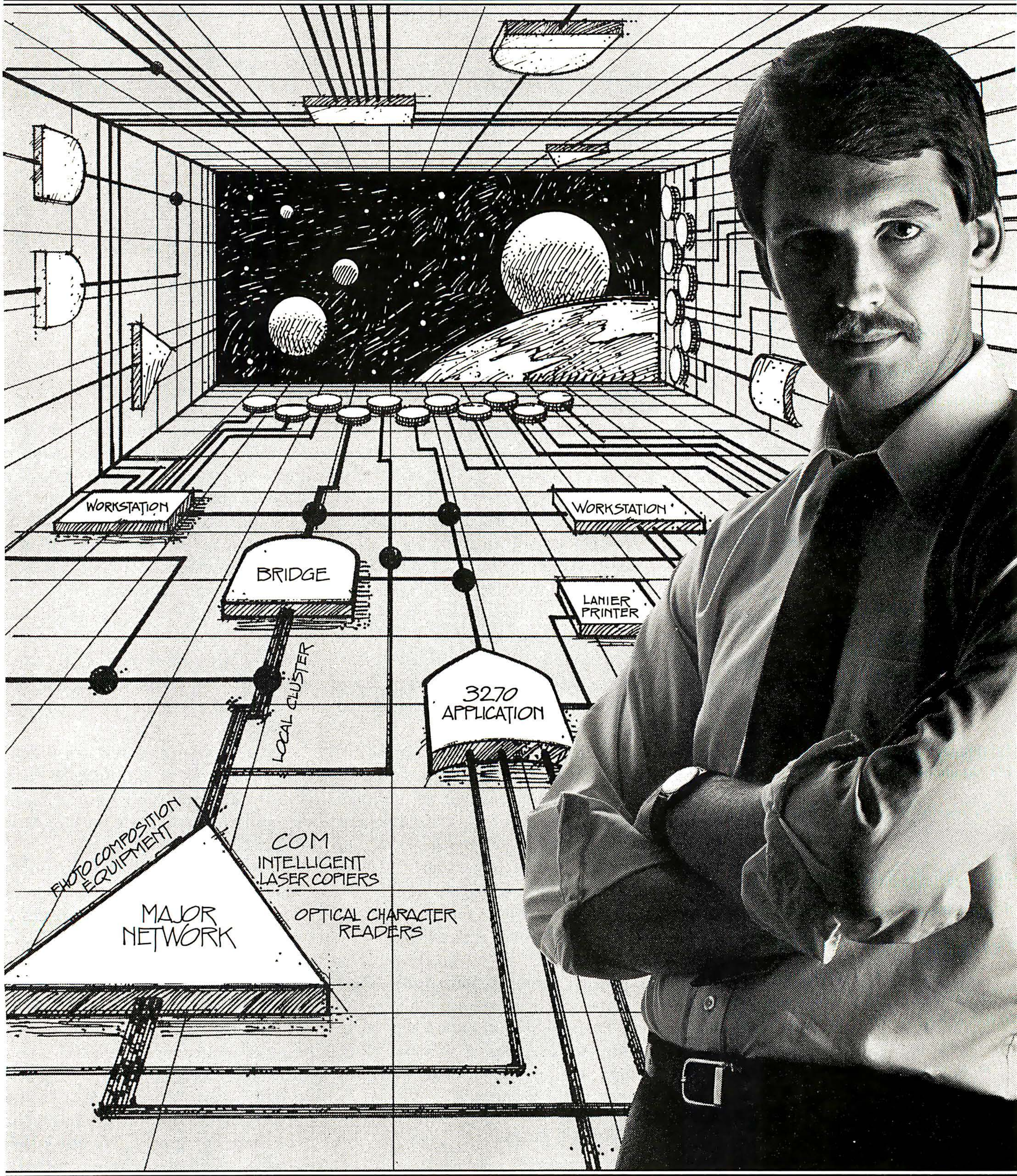
To properly model a possible Q-unknown value, however, a third term (J AND $\overline{K}$) is included.

A parallel load counter (similar to a 74LS163) is modeled as shown in figure 6b; again, each stage is merely some combinational logic followed by a shift register. Using one line of input coding for each stage of the counter provides for a latch position for each stage; note that the use of "continue" lines for the additional stages provides for an automatic determination of the number of stages used and required, precluding the necessity of predefining the number of stages.

A parallel load shift register is identical in concept to the parallel load counter, the only difference being in the combinational logic feeding each shift register.

The N-bit shift register, however, is implemented differently. For ease of coding, as well as efficient memory use, it is unreasonable to require a separate line of input coding for each of the N stages. The second input signal to the N-bit shift register is actually a numeric value specifying N. This input is treated as a numeric value rather than a signal name by using # (number sign) as a prefix to the numeric value, and having the input processor properly handle this numeric marking. (Note that the number/signal distinction is made during input processing without regard to the logic-element type; this

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approach is more flexible than having a separate processor for an N-bit shift register—logic devices defined later may also need such numeric values.) This number is actually stored as a negative number to distinguish it from signal numbers; the sum of these negative numbers is used to dimension array ME for retaining internal memory values.

The eighth entry in the logic-description array contains a pointer to this array for each N-bit shift register used rather than containing the single latch value. The model itself is simulated by N calls to the shift register function, using and storing values in the ME array.

Enhancements

The only obvious enhancement to the program is to add primitives (such as transmission gates and buses) and dynamic array allocation. The program is structured to support the addition of logic primitives by having no fixed limit on the number of primitives used. The initialization subroutine (line 500) reads a list of primitive logic-element names, ended by pseudotype "LAST"; adding primitive names before this "LAST" entry automatically adds it to the primitive list. The statement

```
ON LT GOSUB ...
```

at line 40130 calls the appropriate subroutine to model each primitive; these subroutines are called with IN(1) through IN(5), containing the input signal numbers, and Q0 and Q1, containing the output signal numbers. The subroutine for the added primitive is expected to store the resultant Q output in variable Y; upon return, this value will be stored in NEW(Q0) and its complement in NEW(Q1).

For proper modeling, particularly for proper handling of logic unknowns, a proposed primitive should first be simulated as a combination of existing primitives to verify its operation. The primitive subroutine should then be coded in terms of logical operations (AND and OR), and use the LN array for logical NOTS.

The program in listing 1 is not necessarily memory-efficient under all conditions. The maximum dimension for each array is predefined, independent of the actual number of array locations required by the circuit being simulated; some designs may contain few logic elements and many external stimuli, other designs may have many logic elements but few stimuli, yet the program preallocates a fixed portion of RAM for each array. If it is known, a priori, exactly how many logic elements are required, the dimension could be adjusted accordingly, providing more memory for external stimuli or selective trace; such a predefinition, however, is cumbersome for the user, particularly if macrocircuits are used.

Two approaches are available to optimize memory use. The most straightforward way is to perform a two-pass operation: on the first pass, the required array sizes are calculated; then the data is restored and the arrays are dimensioned to their required sizes for the second pass, which actually performs the storing of values and the simulation.

A more efficient process is "dynamic allocation," in which a single array is used to contain all numeric data. Such an array is dimensioned to the maximum available memory and as each element or external is read, an index is maintained to point to the start of each subarray, similar to the approach taken in LO (the logic-description array), which contains both the macrocircuit definitions and the actual network logic description. The external stimuli array, for example, would follow the network description in this array with a single variable used to store the start of this array; it would then be followed by the selective-trace arrays, the old and new value arrays, and so on.

Conclusion

The use of a logic simulator can replace the use of a hardware digital breadboarding system, particularly if the higher-level modeling capabilities described in this article are included in the system. The added features such as named nodes, macro processing, and sampled outputs make such a system easy to use and provide for a hard-copy logic description that is easier to debug than the equivalent breadboarded system.

Logic simulation is used at professional design centers to verify proper logical operation of proposed designs prior to the costly fabrication of printed-circuit boards. I find this system particularly useful for the simulation of designs presented in hobby magazines, before investing in parts to build these sometimes-untested designs.

One of the biggest advantages I find in using a software-based logic simulator is that I never run out of spare parts on a Saturday night when the local supply stores are closed, nor do I ever burn out expensive ICs by improper connections! ■

Listing 1 begins on page 428

The author can supply copies of the advanced logic simulator for the Radio Shack Model III (listing 1) for $20.

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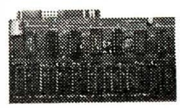
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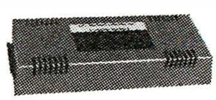


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Listing 1: *The advanced version of the logic-simulation program, written in BASIC for the Radio Shack Model III. The major subroutines are diagramed in figure 1 and figure 2; predefined logic elements are shown in the other figures. The program is very modular and can be expanded to include more predefined logic elements than it now contains. The data statements starting at line 50000 contain a sample set of input coding for a 4-bit counter using nested macros (CNTRM-MUXD-MUX) and as a logic primitive (CNTR).*

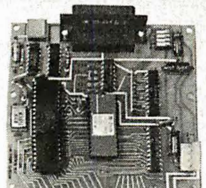
```
10 REM          AN ENHANCED LOGIC SIMULATION PROGRAM
20 REM                  ROBERT M. MCDERMOTT
30 REM                      AUGUST 1981
40 REM
50 REM
60 REM THE FOLLOWING PROGRAM SIMULATES A DIGITAL LOGIC DESIGN
70 REM THE LOGIC DESCRIPTION MAY CONSIST OF LOGIC 'PRIMITIVES'
80 REM (AND,OR,XOR,ETC. GATES; D, JK FLIP FLOPS; N-BIT COUNTER)
90 REM OR 'MACROS' (BLOCKS OF COMMONLY USED PRIMITIVES).
100 REM EACH LOGIC ELEMENT CONTAINS 5 INPUTS AND TWO OUTPUTS,
110 REM UNUSED 'PINS' ARE CODED AS "0".
120 REM THE LOGIC IS DRIVEN BY 'EXTERNAL STIMULI'. THE STIMULI
130 REM ARE DESCRIBED AS PERIODIC OR APERIODIC, THE SIGNAL NAME,
140 REM STARTING LOGIC VALUE, START TIME, AND 5 CHANGE TIMES.
150 REM
160 REM
170 REM THE FOLLOWING PARAMETERS DEFINE THE MAXIMUM ARRAY LIMITS
180 REM THEY CAN BE ADJUSTED TO FIT A DESIGN TO AVAILABLE RAM.
185 CLEAR 1000:DEFINT A-Z
190 MNAMS=200:MLGIC=200:MEXTERN=30:MSAMPLES=14:MTYPES=50
195 PRINT"     LOGIC SIMULATOR: ";MN;" NAMES ";ML;"LOGIC DEVICES"
196 PRINT"                 ";MT;" TYPES ";ME;" EXTERNAL STIMULI"
197 PRINT
198 PRINT
220 DIM NAMS$(MNAMS)                 'SIGNAL NAMES
230 DIM LO(MLGIC,8)                'LOGIC DESCRIPTION
240                                '(7 SIGNALS,LATCH)
250 DIM EXTERNALS(MEXTERNALS,10)         'EXTERNAL STIMULI
260 DIM TYPE$(MTYPES)                   'LOGIC TYPES (PRIM&MACS)
270 DIM TYPEP(MTYPES)             'POINTERS TO LOGIC DES.
275 DIM OL(MN)           'OLD LOGIC VALUE ARRAYS
280 DIM SA(MS)                 'SAMPLED NODES
290 DIM T(10),LI$(10)            'TEMP ARRAYS
300 REM    ******** START OF PROGRAM *************
310 PRINT:PRINT" *****    INITIALIZING ARRAYS    ***** ":GOSUB 500
'INITIALIZE POINTERS
320 PRINT:PRINT" *****    READING IN ANY MACROS     ***** ":GOSUB 1000
'READ ANY MACROS
330 PRINT:PRINT" *****    READING IN LOGIC NETWORK     ***** ":GOSUB 2000
'READ LOGIC NETWORK
340 PRINT:PRINT" *****                 EXPANDING ANY MACROS      *****":GOSUB
3000                     'EXPAND MACROS
345 GOSUB 3500                     'LIST EXPANSION
350 PRINT:PRINT" *****     READING IN EXTERNAL STIMULI      *****":GOSUB 4000
'READ EXTERNALS
360 PRINT:PRINT" *****     CHECKING FOR ERRORS       *****":GOSUB 5000
'CHECK FOR ERRORS
370 PRINT:PRINT" *****     READING IN NODES TO BE SAMPLED     *****":GOSUB 6000
'READ SAMPLE POINTS
380 PRINT:PRINT" *****     SETTING UP FOR SIMULATION     *****":GOSUB 7000
'DO SIMULATION
390 STOP
400 REM
500 REM ******** INITIALIZE POINTERS ***********
510 NL=0:NTYPE=0
520 READ Q$                                 'LOAD PRIMITIVES
530 IF Q$<>"LAST" THEN TY$(NTYPE)=Q$:NTYPE=NTYPE+1:GOTO 520
540 DATA "END","AND","NAND","OR","NOR","XOR","XNOR"
550 DATA "DFF","JKFF","CNTR","PLSR","SREG","*"
560 DATA "LAST"
570 NPRIM=NTYPE:NTYPE=NTYPE+1                       'NTYPE=NEXT TYPE PTR.
590 REM LOGIC PRINT VALUES AND INVERSIONS
600 LO=0:L1=3:LX=1           'INTERNAL VALUES FOR LOGIC VALS.
610 DIM LV$(3),LP$(3),LN(3)      'LOGIC INPUT SYMBOL, LOGIC PRINTSYMBOL, LOGIC
INVERSION
620 LV$(LO)="0":LP$(LO)=".":LN(LO)=L1:LV(LO)=LO
630 LV$(L1)="1":LP$(L1)="1":LN(L1)=LO:LV(L1)=L1
640 LV$(LX)="X":LP$(LX)="?":LN(LX)=LX:LV(LX)=LX
680 DIM TEX$(1):FOR I=0 TO 1:READ TEX$(I):NEXT I
690 DATA "A","P"
990 RETURN
1000 REM ************ READ IN MACROS *********
1010 GOSUB 10000                          'READ AND PARSE LINE
1020 IF LEFT$(L$,3)<>"MAC" THEN RETURN    'SHOULD SAY "MAC TYPE"
1030 X$=LI$(1)                            'GET MAC TYPE
1035 PRINT:PRINT " *****     READING IN MACRO: ";X$;"      *****"
1040 TPTR=-1
1050 GOSUB 11000                          'SEARCH FOR TYPE
1060 IF FOUND=-1 THEN 1100                'CHECK FOR DUPES
1065 IF TPTR=-1 THEN 1100
1070 PRINT "THIS MACRO NAME ALREADY EXISTS, SHOULD IT BE REPLACED WITH THIS
ONE?"
1080 INPUT "ENTER R(eplace) OR N(oreplace)";Q$
1090 IF LEFT$(Q$,1)="N" THEN 1200    'SKIP TIL NEXT END
1100 TPTR=NLGIC               'POINT TO NEXT LOGIC LOCATION
1110 GOSUB 11100 :MT=FO             'ADD TYPE TO LIST
1150 GOSUB 2000                           'READ CKT DESCRIPTION
1160 GOSUB 1500                           'CHECK FOR MACRO ERRORS
1170 GOTO 1000                            'LOOP FOR NEXT MACRO
1200 REM *** SKIP THIS MACRO ****
1210 GOSUB 10000:IF LI$(0)<>"END" THEN GOTO 1210
1220 GOTO 1000                            'GET NEXT MACRO
1500 REM **** CHECK FOR MACRO ERRORS *****
1510 PRINT:PRINT" *****     CHECKING MACRO ";TY$(MT);" FOR ERRORS      *****"
1520 X1=TY(MT):GOSUB 12000                              'CLEAR ARRAY
1530 FOR I=1 TO 5                         'STEP THRU INPUTS
1540 X=LO(X1,I):GOSUB 12100               'MARK EACH SIG #
1550 NEXT I
1560 X1=X1+1
1570 X=LO(X1,0):IF TY$(X)="*" THEN GOTO 1530 'LOOP FOR CONTINUES
1580 ST=X1
1590 GOSUB 12200                          'MARK AND CHECK OUTPUTS
1600 GOSUB 12300                          'CHECK INPUTS
1610 ER=0          'CLEAR ERROR FLAG, MAC ERRORS DONT COUNT.
1620 RETURN
2000 REM ********* READ IN LOGIC DESCRIPTION ***********
2010 SL=NL:NA$(0)="0":NNAM=1              'SIGNAL 0 IS PREDEFINED
```

Listing 1 continued on page 432

Micromint will put both a computer development system and an OEM dedicated controller in the palm of your hand for as little as $127.*

The Z8 Basic Computer/Controller represents a milestone in microcomputer price-performance. The entire computer is 4" by 4½" and includes a tiny BASIC interpreter, 4K bytes of program memory, one RS-232 serial port and two parallel ports plus a variety of other features. The Z8 microcomputer board is completely self-contained and optimized for use as a dedicated controller. Can be battery operated. Comes with over 200 pages of documentation.

Z8 BASIC COMPUTER/CONTROLLER



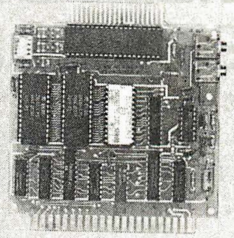
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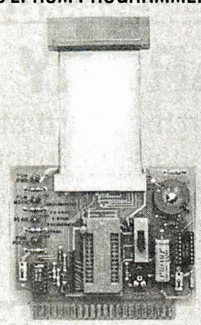
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The Z8 Memory, I/O Expansion & Cassette Interface Board (Z8 Expansion Board for short) allows you to add up to 8K of additional memory plus three 8-bit parallel ports to your Z8 Basic Computer/Controller. The memory expansion will support any combination of byte wide RAM memory chips or 2716 or 2732 EPROM. The cassette interface is 300 baud Kansas City Standard (2400Hz/1200Hz).

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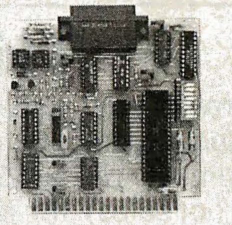
Z8 EPROM PROGRAMMER



The EPROM Programmer board allows you to transfer application programs in BASIC or Assembly language directly from RAM to either 2716 or 2732 EPROMS. Requires Z8 Basic Expansion Board for operation.
NOTE: We recommend the higher current UPS03 or UPS04 power supply when using the EPROM Programmer.

BCC07 Z8 EPROM Programmer Assembled & Tested . . . $145.00

Z8 SERIAL EXPANSION BOARD



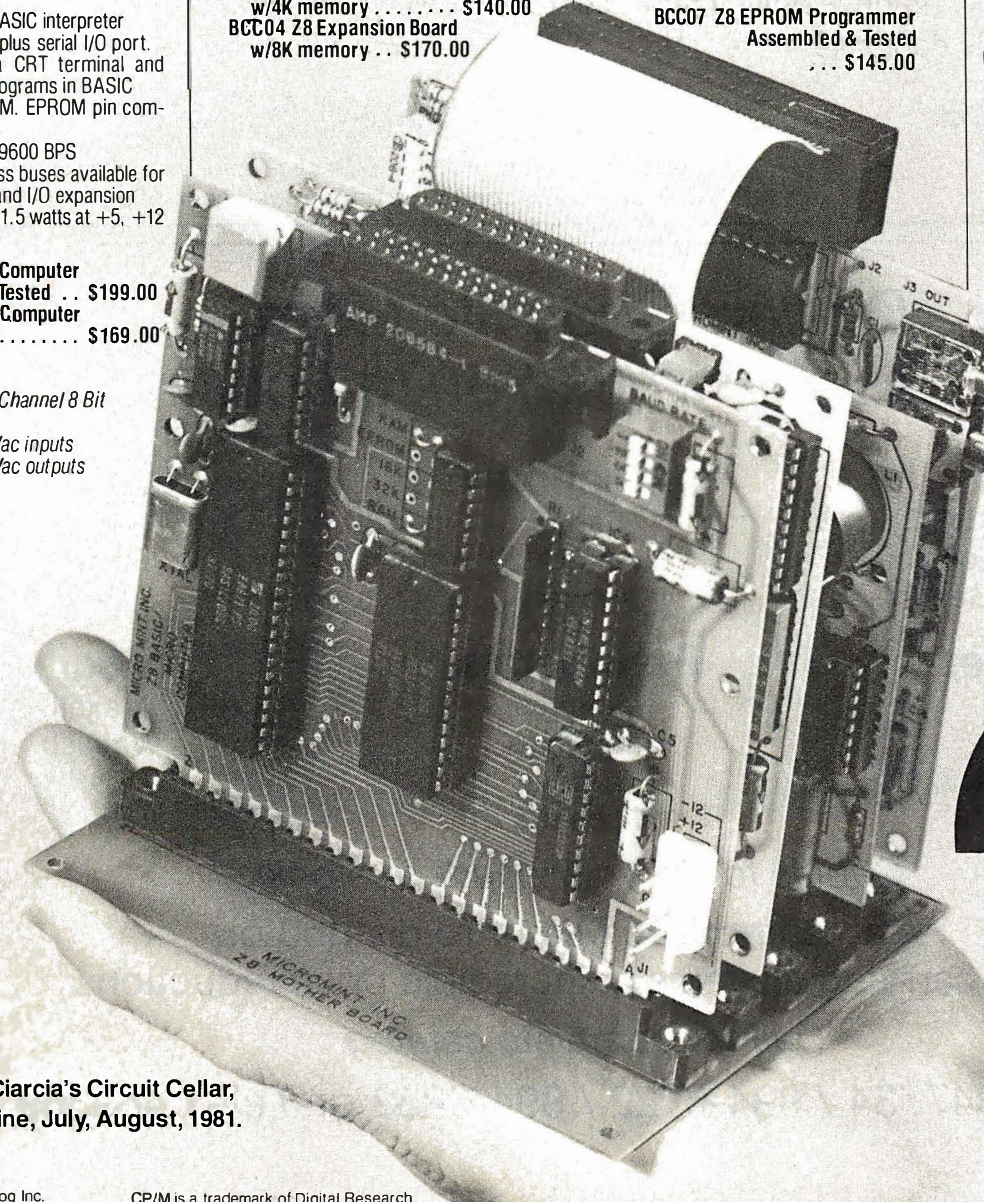
The Serial Expansion Board adds an additional RS-232C serial port to the Z8 system. It runs at 75 to 19,200 baud in all standard protocols. The 20 ma. current loop is opto-isolated for reliability and protection.

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.s featured in Ciarcia's Circuit Cellar, Byte Magazine, July, August, 1981.

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Circle 261 on inquiry card.

Z8 is a trademark of Zilog Inc. CP/M is a trademark of Digital Research

***In quantities of 100**

Listing 1 continued:

```
2020 FOR I=1 TO MN:NA$(I)="":NEXT I      'CLEAR ALL NAMES
2040 GOSUB 10000                         'READ NEXT LINE
2050 X$=LI$(0)                           'LOOK UP TYPE
2060 GOSUB 11000:IF FO=-1 THEN GOSUB 11100 'ADD IF NOT FOUND
2070 T(0)=FO
2080 FOR I=1 TO 7                        'GET ALL NAMES
2090 X$=LI$(I):GOSUB 11500               'LOOK UP NAME
2100 IF FO=-1 THEN GOSUB 11600           'ADD IF NOT FOUND
2110 T(I)=FO:NEXT I
2120 GOSUB 20000                         'ADD T(0)-T(7) TO LO ARRAY
2130 IF T(0)<>0 THEN GOTO 2040           'GET NEXT ELEMENT
2140 RETURN                              'RETURN ON "END"
3000 REM ********* EXPAND MACROS *************
3010 ST=SLGIC:FM=0       'START AT LOGIC ARRAY, CLEAR MAC FLAG
3020 FOR I=ST TO NLGIC-1                'SCAN ENTIRE LIST
3030 IF LO(I,0)<=NPRIM THEN 3100         'SKIP PRIMITIVES
3040 GOSUB 30000                         'BUILD CORRESPONDENCE
3050 GOSUB 31000                         'DO EXPANSION
3060 FM=1
3100 NEXT I
3110 REM REPEAT PROCEDURE UNLESS NO MACROS WERE FOUND
3120 IF FM<>0 THEN GOTO 3000
3130 RETURN
3500 REM ******** LIST OF EXPANDED LOGIC DESCRIPTION *****
3510 CLS:PRINT " *****      EXPANDED LOGIC DESCRIPTION      *****":PRINT
3511 PRINT "TYPE";TAB(20);"INPUTS";TAB(50);"OUTPUTS"
3512 FOR I=1 TO 5:PRINTTAB(8*I);I;:NEXT I:PRINTTAB(48);"Q";TAB(56);"Q-"
3515 NA$(0)=" "
3520 FOR I=SL TO NL-1
3530 PRINT TY$(LO(I,0));
3540 FOR II=1 TO 7
3550 PRINT TAB(8*II);
3552 XX=LO(I,II):IF XX<0 THEN PRINT "#";-XX;:GOTO 3560
3554 PRINT NA$(XX);
3560 NEXT II:PRINT:NEXT I
3565 NA$(0)="0"
3570 RETURN
4000 REM ******** READ IN EXTERNAL DESCRIPTION **********
4010 NEX=0:GOSUB 10000  'IGNORE "EXTERNAL"
4020 GOSUB 10000        'GET EXTERNAL DESCRIPTION
4030 IF LI$(0)="END" THEN RETURN
4040 FOR I=0 TO 1:IF LI$(0)=TEX$(I) THEN T(0)=I  'GET TYPE OF EXT
4050 NEXT I
4060 X$=LI$(1):GOSUB 11500        'GET SIGNAL NUMBER FROM NAME
4070 IF FO=-1 THEN GOTO 4020      'IGNORE IF UNDEFINED
4080 T(1)=FO
4090 FOR I=0 TO 3:IF LI$(2)=LV$(I) THEN T(2)=LV(I) 'LOGIC VALUE
4100 NEXT I
4110 FOR I=3 TO 9:T(I)=VAL(LI$(I)):NEXT I       'CHANGE TIMES
4120 GOSUB 21000                  'STORE T(0)-T(9) IN EX ARRAY
4130 GOTO 4020                    'LOOP TILL "END"
5000 REM ******** CHECK FOR ERRORS *********
5010 GOSUB 12000:MM=0         'CLEAR OLD ARRAY
5020 FOR I=0 TO NEX     'MARK EXTERNALS FIRST
5030 OL(EX(I,1))=1
5040 NEXT I
5050 ST=SL:GOSUB 12200   'MARK AND CHECK OUTPUTS
5060 GOSUB 12300         'CHECK ALL INPUTS
5070 RETURN
6000 REM ********* READ IN SAMPLE POINTS ***************
6010 NS=0:ON ERROR GOTO 6200
6020 GOSUB 10000         'READ IN LINE (IF ANY, IF NOT, GOTO 6200
6030 GOSUB 10000         'GET REAL LINE (PRIOR ONE WAS "EXTE.."
6040 IF LI$(0)="END" THEN ON ERROR GOTO0: RETURN
6050 FOR I=0 TO 10
6060 X$=LI$(I):IF X$=" " THEN 6100      'GET NAME, IGNORE BLANKS
6070 GOSUB 11500:IF FO=-1 THEN 6100     'LOOK UP NAME, IGNORE UNDEFINED
6080 IF NS<14 THEN NS=NS+1:SA(NS)=FO
6100 NEXT I
6110 GOTO 6030           'LOOP TIL "END"
6200 REM ***** ERROR TRAP FOR END OF INPUT  **********
6210 L$="END":RESUME NEXT
6500 REM ***** SELECTIVE TRACE TABLE BUILD **********
6510 STF=0               'SEL. TRACE FLAG
6520 A1=(NL+NN+(TL+NN))*2  'REQUIRED RAM (NN FOR 1ST, TL+NN FOR 2ND,NL FOR OTH
6530 A2=MEM-200          'AVAILABLE (ASSUME MAX 200 NEEDED LATER)
6540 IF A2<A1 THEN RETURN 'NOT ENOUGH RAM, FORGET IT
6550 PRINT:PRINT " *****     BUILDING SELECTIVE TRACE TABLE     *****":PRINT
6560 STF=1:DIM SO(NL),S1(NN),S2(TL+NN)
6570 T1=0         'T1 POINTS TO SECOND ARRAY
6580 FOR I=1 TO NN:S1(I)=T1              'FOR ALL NODES
6590 FOR J=SL TO NL:FOR K=1 TO 5         'SCAN ALL INPUTS TO LOGIC
6600 IF LO(J,K)=I THEN S2(T1)=J:T1=T1+1  'ON MATCH, SAVE LOGIC #
6610 NEXT K:NEXT J
6620 S2(T1)=-1:T1=T1+1             '-1 = "SENTINEL" BETWEEN BLOCKS
6630 NEXT I
6635 GOSUB 6700          'PRINT OUT LOAD TABLE
6640 RETURN
6700 REM **** PRINT OUT OF LOAD TABLE ********
6710 PRINT " *****      LOAD TABLE      *****":PRINT "NODE            DRIVEN
ELEMENTS"
6720 FOR II=1 TO NN:PRINT NA$(II);TAB(10);
6730 T1=S1(II)
6740 IF S2(T1)=-1 THEN GOTO 6760
6750 PRINT S2(T1)-SL+1;:T1=T1+1:GOTO 6740
6760 PRINT:NEXT II:RETURN
7000 REM ******* DO SIMULATION ****************
7010 DIM NE(NN),ME(MM,1):IF ER<>0 THEN RETURN      'NO SIMULATION ON ERROR
7020 NN=NN-1:NL=NL-1:NE=NE-1          'POINT TO ENDS, NOT NEXT
7030 GOSUB 6500                 'BUILD SELECTIVE TRACE TABLE
7040 GOSUB 7300                 'INITIALIZE, GET SAMPLE TIMES
7050 GOSUB 8000                 'GET EXTERNALS SCHED FOR THIS TIME
7060 GOSUB 8500                 'MOVE NEW TO OLD, MARK CHANGES
7070 GOSUB 9000                 'PRINT OUT OLD, GET RESPONSE
7080 IF Q$="Q" THEN RETURN
7090 IF Q$="R" THEN GOTO 7040   'RESTART
7100 GOSUB 40000                'SIMULATE LOGIC DEVICES
7110 GOSUB 7500                 'RECALC RIPPLE TIME
7120 GOTO 7050                  'LOOP
7300 REM ******INITIALIZE FOR SIMULATION ********
7310 FOR I=0 TO NN:NE(I)=LX:NEXT I      'ALL NEWS = LOGIC X
7320 FOR I=SL TO NL:LO(I,8)=LX:NEXT I   'ALL INTERNAL LATCHES =X
7330 PRINT:RI=0:INPUT "ENTER SAMPLE START TIME, INCREMENT TIME";S9,S2
7340 IF S2=0 THEN S2=1                  'CANT HAVE 0 INCREMENT.
7350 E9=32767:FOR I=0 TO NEX: E3=EX(I,3):GOSUB 8200:NEXT I         'PUT
EXTERNALS START TIME INTO NEXT SCHEDULED TIME
7360 IF NS=0 THEN GOSUB 9660   'GET NAMES FOR SAMPLING IF NOT READ
7370 IF MM<>0 THEN GOSUB 7400  'SET ASIDE MEMORY FOR SREGs
7390 Q$="":RETURN
7400 REM SET ASIDE MEM FOR SREGs
7410 M1=0           'M1 POINTS TO NEXT AVAIL MEM
7415 FOR I=0 TO MM:ME(I,0)=LX:ME(I,1)=LX:NEXT I
```

Listing 1 continued on page 434

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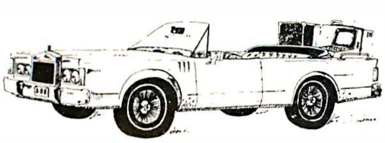
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Listing 1 continued:

```
7420 FOR I=SL TO NL          'THE LATCH POS. WILL CONTAIN PTR.
7430 IF TY$(LO(I,0))="SREG" THEN LO(I,8)=M1:M1=M1-LO(I,2)
7440 NEXT I:RETURN
7500 REM ********* RECALCULATE RIPPLE TIME ********
7510 IF C9=1 THEN RI=RI+1:RETURN
7520 RI=E9:IF RI>S9 THEN RI=S9  'GET MIN OF E9 (EXT) AND S9 (SAMPLE)
7530 RETURN
8000 REM ******* GET NEXT SCHEDULED EXTERNAL **********
8010 IF RI<>E9 THEN RETURN
8020 E9=32767
8030 FOR I=0 TO NEX              'SCAN EACH EXTERNAL STIMULI
8035 E3=EX(I,10)
8040 IF E3=RI THEN GOSUB 8100      'PROCESS IF SCHED.
8045 GOSUB 8200
8050 NEXT I
8060 RETURN
8100 REM *** FIND NEXT SCHED CHANGE (OR FIRST VAL) ***
8110 E0=EX(I,0):E1=EX(I,1):E2=EX(I,2):E3=EX(I,3)
8120 Y=NE(E1)                    'CURRENT NEW VALUE
8130 IF RI=E3 THEN Y=LN(E2)      'FIRST SCHED VALUE
8140 NE(E1)=LN(Y)                'STORE COMPLEMENT OF NEW (OR FIRST SCHED VALUE)
8150 REM SCHEDULE NEXT CHANGE
8160 IF TEX$(E0)="P" THEN E3=EX(I,10)+EX(I,4): RETURN
8170 J=4:E3=32767        'SCAN ENTRIES OF APERIODIC SIGNAL
8175 IF J>=9 THEN RETURN
8180 IF EX(I,J)<=RI THEN J=J+1 : GOTO 8175
8190 E3=EX(I,J): RETURN
8200 REM STORE NEXT SCHED, KEEP TRACK OF MIN (E9)
8210 EX(I,10)=E3  '10TH ENTRY IS NEXT SCHED TIME FOR THIS SIGNAL
8220 IF E9>E3 THEN E9=E3   'E9 IS NEXT SCHED TIME FOR ANY SIG.
8230 RETURN
8500 REM ******MOVE NEW TO OLD, MARK CHANGES ************
8510 C9=0:IF STF<>0 THEN GOSUB 8700     'CLEAR CHANGE FLAGS
8520 FOR I=1 TO NN       'GO THRU ALL NODES
8530 IF NE(I)<>OL(I) THEN GOSUB 8600    'MARK CHANGES
8540 NEXT I
8560 RETURN
8600 C9=1:OL(I)=NE(I)            'NOTE CHANGE
8610 IF STF=0 THEN RETURN
8620 II=S1(I)                    'MARK ALL DRIVEN ELEMENTS
8630 J=S2(II):IF J=-1 THEN RETURN 'RETURN ON HITTING A SENTINEL
8640 SO(J)=1:II=II+1:GOTO 8630  'MARK IT, GET NEXT LOGIC NUMBER
8700 REM CLEAR SO
8710 FOR II=SL TO NL:SO(II)=0:NEXT II
8720 RETURN
9000 REM ********** DISPLAY LOGIC VALUES
9002 PRINT @57,RI;
9005 IF S9<>RI THEN RETURN
9010 IF PC=0 THEN GOSUB 9100     'PUT NAMES ON SCREEN IF START
9020 GOSUB 9500                  'PRINT VALUES DOWN SCREEN
9025 S9=S9+S2
9030 PC=PC+1:IF PC>60 THEN GOSUB 9600  'END OF SCREEN, GET INPUT
9040 RETURN
9100 REM ******* SET UP DISPLAY (NAMES AND TICS) ******
9110 PC=11
9120 CLS:GOSUB 9200                    'DO TIC MARKS
9125 PRINT @5,"TIME";:PRINT @10,RI;
9130 X=128
9140 FOR I=1 TO NS:PRINT @X,NA$(SA(I));
9150 X=X+64:NEXT I
9160 RETURN
9200 REM ********PRINT TIC MARKS ********
9210 FOR X=75 TO 124:PRINT @X,CHR$(176);:NEXT X
9220 X=75
9230 FOR I=1 TO 5:PRINT @X,CHR$(191);:PRINT @X+5,CHR$(188);
9240 X=X+10:NEXT I:RETURN
9500 REM *******PRINT VALUES DOWN COLUMN ********
9510 X=PC+128                       'DOWN 2 LINES
9520 FOR I=1 TO NS:Y=OL(SA(I))  'GET LOGIC VALUE
9530 PRINT @X,LP$(Y);:X=X+64:NEXT I
9540 RETURN
9600 REM ***** FULL SCREEN, GET RESPONSE ******
9610 PRINT @15,"C(hange),R(eset),Q(uit), OR ANY OTHER KEY";
9620 Q$=INKEY$:FORX=0TO100:NEXTX: PRINT @15,STRING$(41," ");
9625 IF Q$="" THEN GOTO 9610
9630 PC=0  ' RESET AND QUIT ARE HANDLED ON RETURN
9640 IF Q$<>"C" THEN RETURN
9650 REM GET NEW SAMPLE NODE NAMES
9655 CLS
9660 PRINT "AS EACH CURRENT SAMPLE NODE IS DISPLAYED, HIT RETURN FOR NO
CHANGE, NEW NAME FOR CHANGE"
9670 FOR I=1 TO 14
9680 X$="":PRINT NA$(SA(I));:INPUT X$
9690 IF X$="" THEN GOTO 9720
9700 GOSUB 11500:IF FO=-1 THEN GOTO 9680
9710 SA(I)=FO
9720 IF SA(I)<>0 THEN NS=I
9730 NEXT I:RETURN
10000 REM ************ READ AND PARSE LINE ***********
10010 READ L$                        'INPUT IS DATA STATEMENTS, ASCII
10020 I=1:I3=1:LI=0:I2=LEN(L$)  'INITIALIZE
10030 I=I+1: IF I>I2 THEN 10050
10040 IF MID$(L$,I,1)<>" " THEN GOTO 10030   'FIND BLANK
10050 LI$(LI)=MID$(L$,I3,I-I3)  'PUT NAME IN LI$
10060 LI=LI+1
10070 IF LI>10 THEN RETURN
10080 I=I+1:IF I>I2 THEN 10120
10090 IF MID$(L$,I,1)=" " THEN GOTO 10080  'SKIP BLANKS
10100 I3=I:GOTO 10030
10120 FOR I=LI TO 10     'FILL REMAINING LI$s
10130 LI$(I)=" ":NEXT I
10140 RETURN
11000 REM ********* LOOK UP TYPE **********
11010 FO=-1                    'FOUND LOCATION
11020 FOR II=0 TO NTYPE-1
11030 IF X$=TYPES$(II) THEN FO=II:TP=TYPTR(II)
11040 NEXT II
11050 RETURN
11100 REM ******** ADD TYPE *********
11110 IF FO=-1 THEN FO=NTYP:NTYP=NTYP+1
11120 IF FO>NTYP THEN NTYP=FO
11130 TYPES$(FO)=X$
11140 TYPE(FO)=TPTR
11150 RETURN
11500 REM ******* LOOK UP SIGNAL NAME *********
11510 FO=-1:IF X$=" " THEN X$="0"         'BLANK =NO SIGNAL
11515 IF LEFT$(X$,1)="#" THEN GOTO 11560   'NUMERIC INPUT
11520 FOR II=0 TO NNAM
11530 IF X$=NAM$(II) THEN FO=II
11540 NEXT II
11550 RETURN
11560 REM "NAME" IS A NUMBER, STORE AS NEGATIVE
```

Listing 1 continued on page 436

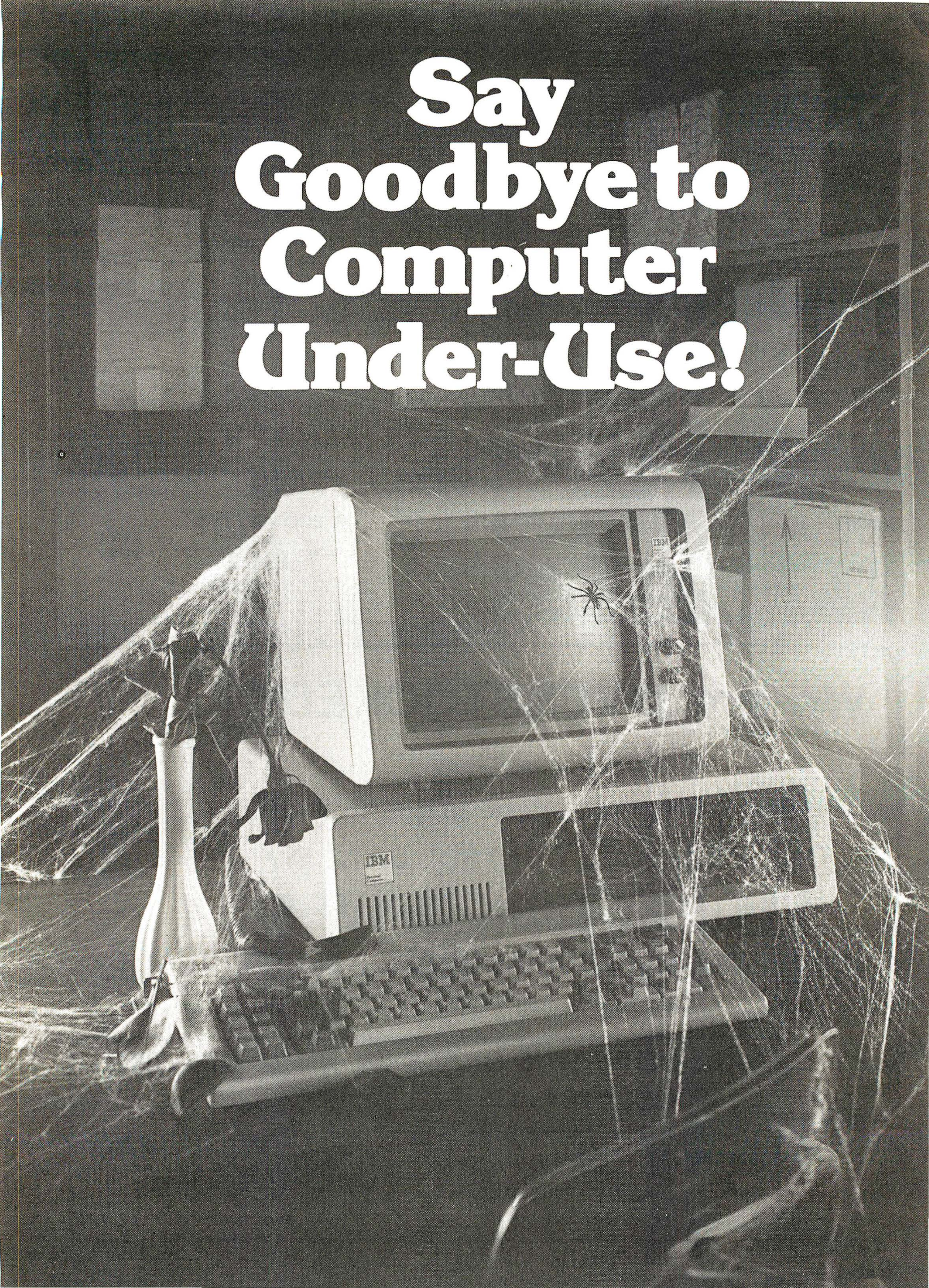
Listing 1 continued:

```
11570 XX$=RIGHT$(X$,LEN(X$)-1)  'STRIP OFF # SIGN
11580 FO=-VAL(XX$):IF FO=-1 THEN FO=0 'IGNORE N=1 (DEFAULT)
11590 RETURN
11600 REM ********  ADD NAME TO LIST *********
11610 IF FO=-1 THEN FO=NNAM:NNAM=NNAM+1
11620 IF FO>NNAM THEN NNAM=FO+1
11630 NAM$(FO)=X$
11640 RETURN
12000 REM ****** CLEAR OLD ARRAY ********
12010 FOR I=0 TO MN:OL(I)=0:NEXT I
12020 TL=0:RETURN
12100 REM ********* MARK (OUTPUTS) AND CHECK FOR DUPES ******
12110 IF X=0 THEN RETURN
12120 IF OL(X)<>0 THEN GOSUB 12150
12130 OL(X)=1:RETURN
12150 PRINT "ERROR, MULTIPLE DEFINITION OF OUTPUT ";NA$(X)
12155 GOSUB 12160:RETURN
12160 INPUT "ENTER I(gnore) TO IGNORE ERROR, ANY OTHER KEY TO PREVENT
SIMULATION";Q$
12170 IF LEFT$(Q$,1)<>"I" THEN ER=1
12180 RETURN
12200 REM ******* CHECK FOR MULTIPLE OUTPUTS ***********
12210 X1=ST
12220 FOR I=X1 TO NL-1
12230 FOR J=6 TO 7
12240 X=LO(I,J):GOSUB 12100               'MARK AND CHECK
12250 NEXT J:NEXT I:RETURN
12300 REM ******* CHECK FOR DEFINED INPUTS ************
12310 X1=ST
12320 FOR I=X1 TO NL-1
12330 FOR J=1 TO 5
12340 X=LO(I,J):GOSUB 12400               'CHECK FOR MARK
12345 IF X<0 THEN MM=MM-X       'KEEP TRACK OF MEM REQUIRED
12350 NEXT J:NEXT I:RETURN
12400 REM ******* CHECK FOR MARK ********
12410 IF X<=0 THEN RETURN
12420 IF OL(X)=0 THEN GOSUB 12450
12430 OL(X)=OL(X)+1:TL=TL+1:RETURN
12450 PRINT "ERROR, UNDEFINED INPUT ";NA$(X)
12460 GOSUB 12160:RETURN
12470 ER=1:RETURN
20000 REM ********** ADD T(0) THRU T(7) TO LOGIC ARRAY ******
20010 FOR II=0 TO 7
20020 LO(NL,II)=T(II)
20030 NEXT II
20040 PRINT TY$(LO(NL,0));" ";:FOR II=1 TO 7
20050 XX=LO(NL,II):IF XX<0 THEN PRINT "#";-XX;" ";:GOTO 20070
20060 PRINT NA$(XX);" ";
20070 NEXT II:PRINT:NL=NL+1:RETURN
21000 REM ********** ADD T(0) THRU T(9) TO EXTERNAL ARRAY ****
21010 FOR II=0 TO 9
21020 EX(NE,II)=T(II)
21030 NEXT II
21040 PRINT TEX$(EX(NE,0));" ";NA$(EX(NE,1));" ";LV$(EX(NE,2));" ";:FOR II=3 TO
9:PRINT EX(NE,II);:NEXT II:PRINT
21050 NE=NE+1:RETURN
30000 REM ******* BUILD MACRO CORRESPONDENCE ARRAY *********
30010 REM I=EL #, J=MACRO POINTER
30020 LO=I:X=LO(I,0):J=TYPE(X):Y=LO(J,0):M1=J:OL(0)=0
30025 PRINT:PRINT" *****     EXPANDING CALL TO MACRO: ";TY$(X);"      *****"
30030 REM USES OLD VALUE ARRAY FOR EXPANSION (SINCE NOT USED YET)
30040 FOR K=1 TO MNAM:OL(K)=-1:NEXT K    'CLEAR ARRAY
30100 IF X<>Y THEN GOTO 30900     'ERROR IF NO MATCH ON TYPE
30110 FOR K=1 TO 5          'DO THE INPUTS FIRST
30120 I1=LO(M1,K):I2=LO(LO,K)     'I1=MAC #, I2=TRUE SIG #
30130 IF I1=0 AND I2<>0 THEN GOTO 30150     'IGNORE UNDEF. INPUTS
30140 OL(I1)=I2             'OL WILL CONTAIN TRUE SIGNAL #S
30150 NEXT K
30160 FOR K=6 TO 7          'DO OUTPUTS NOW (DIFF PROCESSING OF OS)
30170 I1=LO(M1,K):I2=LO(LO,K)     'I1=MAC, I2=TRUE
30180 IF I1<>0 AND I2=0 THEN  GOTO 30195  'IGNORE UNUSED OUTS
30190 OL(I1)=I2
30195 NEXT K
30200 REM OK, GOT CORRESPONDENCE, DELETE THIS CALL
30210 GOSUB 30500           'MOVE LOGIC ARRAY UP ONE.
30220 M1=M1+1:Y=LO(M1,0):X=LO(LO,0)     'CHECK FOR CONTINUE
30230 IF TY$(Y)="*" THEN GOTO 30100     'LOOP FOR CONTINUES
30240 RETURN
30500 REM ******** MOVE EL ARRAY UP ONE (DELETE CURRENT LINE) **
30510 NL=NL-1
30520 FOR K=LO TO NL-1             'DO ENTIRE ARRAY
30530 FOR K1=0 TO 8                'ALL ENTRIES
30540 LO(K,K1)=LO(K+1,K1)          'MOVE UP EACH ENTRY
30550 NEXT K1:NEXT K
30560 RETURN
30900 REM ******* MISMATCH ON MACRO CALL ******
30910 REM THIS SHOULDNT HAPPEN, BUT NEVER CAN TELL.
30920 PRINT "MISMATCH ON MACRO CALL, CANT CONTINUE"
30930 STOP
31000 REM ******** ADD EXPANDED MACRO TO ELEMENT ARRAY *****
31010 NL=NL-1               'POINT TO PREVIOUS "END"
31020 T(0)=LO(M1,0)         'TYPE
31030 FOR K=1 TO 7
31040 X=LO(M1,K)            'MACRO SIGNAL NUMBER
31045 IF X<0 THEN T(K)=X:GOTO 31070    'DIRECT STORE OF -#S
31050 IF OL(X)=-1 THEN GOSUB 31500       'ADD SIG # IF NOT DEFINED
31060 T(K)=OL(X)                   'GET REAL SIGNAL NUMBER
31070 NEXT K
31080 GOSUB 20000                  'STORE T(0)-T(9) INTO LOGIC ARR
31090 M1=M1+1:IF T(0)<>0 THEN GOTO 31020 'REPEAT TILL END
31100 RETURN
31500 REM ******* ADD UNIQUE NAME, NUMBER ******
31510 OL(X)=NNAM:X$=STR$(NNAM)
31520 NAM$(NNAM)="&"+RIGHT$(X$,LEN(X$)-1)
31530 NNAM=NNAM+1
31540 RETURN
40000 REM **********  SIMULATE GATES *************
40010 IF C9=0 THEN RETURN          'NO ACTIVITY
40020 L=SL
40030 IF STF<> 0 THEN IF SO(L)=0 THEN GOTO 40050
40040 GOSUB 40100                  'SIMULATE THIS GATE
40050 L=L+1:IF L<=NL THEN GOTO 40030
40060 RETURN
40100 REM **** SIMULATE THIS GATE (L) ********
40110 LT=LO(L,0):FOR I=1 TO 5:IN(I)=LO(L,I):NEXT I
40120 Q0=LO(L,6):Q1=LO(L,7)        'GOT TYPE,INs,OUTs
40130 ON LT GOSUB
41010,41000,41110,41100,41210,41200,41500,41600,41700,41800,41900
40140 REM          AND   NAND   OR   NOR   XOR   XNOR  DFF  JKFF  CNTR  PLSR
SREG
40150 GOSUB 40200           'STORE Y INTO Q AND Y- INTO Q-
40160 RETURN
```

Listing 1 continued on page 438

Listing 1 continued:

```
40200 REM ******* STORE Q AND Q- **********
40210 NE(QO)=Y:NE(Q1)=LN(Y):RETURN
40300 REM *** GET Q INTO XQ *****
40310 OL(O)=LN(OL(Q1)):XQ=OL(QO):RETURN
41000 X=QO:QO=Q1:Q1=X    '*********    NAND GATE **********
41010 OL(O)=L1:Y=L1      '*********     AND GATE **********
41020 FOR I=1 TO 5:Y=Y AND OL(IN(I)):NEXT I
41030 RETURN
41100 X=QO:QO=Q1:Q1=X    '********    NOR GATE **********
41110 OL(O)=LO:Y=LO      '********     OR GATE **********
41120 FOR I=1 TO 5:Y = Y OR OL(IN(I)): NEXT I
41130 RETURN
41200 X=QO:QO=Q1:Q1=X    '********** XNOR GATE **********
41210 OL(O)=LX           '**********  XOR GATE **********
41220 YO=OL(IN(1)):Y1=LN(YO):YC=OL(IN(2))        'DO AS MUX
41230 GOSUB 45000:RETURN
41500 REM ******** D FLIP FLOP ***************
41510 GOSUB 40300:OL(O)=LX:XD=OL(IN(1)):XC=OL(IN(3)) 'GET VALUES
41520 XL=LO(L,8):OL(O)=L1:XR=OL(IN(4)):XS=OL(IN(5)) 'MORE INPUTS
41530 GOSUB 45100:LO(L,8)=YL     'SR FUNCTION CALL, YL=LATCH
41540 RETURN
41600 REM ********* J-K FLIP FLOP *******************
41610 REM SET UP AS A MULTIPLEXED DFF, Q CONTROLS MUX
41620 GOSUB 40300:XM=XQ:OL(O)=LX:XC=OL(IN(3))
41630 DO=OL(IN(1)):D1=LN(OL(IN(2)))  'D=J*Q- OR K-*Q
41640 OL(O)=L1:XR=OL(IN(4)):XS=OL(IN(5)):XL=LO(L,8)
41650 GOSUB 45300:LO(L,8)=YL:RETURN      'DO AS MUX-D
41700 REM **** PARALLEL LOAD COUNTER **************
41710 OL(O)=LX:YE=OL(IN(2)):XC=OL(IN(3)):OL(O)=LO:XM=OL(IN(4))
41720 OL(O)=L1:XR=OL(IN(5)):XS=L1
41730 GOSUB 40300:XL=LO(L,8)     'GET Q AND LATCH
41740 YC=YE:YO=XQ:Y1=LN(YO)      'COUNT =COUNT- IF ENAB=1, (MUX)
41750 GOSUB 45000:DO=Y:D1=OL(IN(1)):GOSUB 45300 'MUX THEN MUXD
41760 LO(L,8)=YL:IF TY$(LO(L+1,0))<> "*" THEN RETURN
41770 GOSUB 40200:L=L+1:IN(1)=LO(L,1):QO=LO(L,6):Q1=LO(L,7)
41780 YE=YE AND Y : GOTO 41730   'LOOP AFTER GETTING NEXT CARD
41800 REM **** PARALLEL LOAD SHIFT REGISTER ************
41810 OL(O)=LX:DO=OL(IN(2)):XC=OL(IN(3)):OL(O)=LO:XM=OL(IN(4))
41820 OL(O)=L1:XR=OL(IN(5)):XS=L1
41830 OL(O)=LX:D1=OL(IN(1)):GOSUB 40300:XL=LO(L,8):GOSUB 45300 'DO MUX-DFF
41840 LO(L,8)=YL:IF TY$(LO(L+1,0))<>"*" THEN RETURN
41850 GOSUB40200:L=L+1:IN(1)=LO(L,1):QO=LO(L,6):Q1=LO(L,7):DO=Y
41860 GOTO 41830          'LOOP AFTER STORING Q AND GETTING NEXT
41900 REM ******* N BIT SHIFT REGISTER ************
41910 IF IN(2)=0 THEN GOTO 41500         '(1 BIT IS SAME AS DFF)
41920 OL(O)=LX:XD=OL(IN(1)):XC=OL(IN(3)) 'GET D AND CLOCK
41930 OL(O)=L1:XR=OL(IN(4)):XS=OL(IN(5)) 'GET RESET AND SET
41940 M1=LO(L,8)         'LATCH POS. IS USED TO STORE MEMLOC.
41950 FOR I=1 TO -IN(2) 'LOOP THRU FOR EACH STAGE (N IS STORED -)
41960 XL=ME(M1,O):XQ=ME(M1,1)    'GET LATCH AND Q FROM MEM
41970 GOSUB 45100:XD=XQ:ME(M1,O)=YL:ME(M1,1)=Y 'DO SR AND STORE
41980 M1=M1+1:NEXT I
41990 RETURN
45000 REM ******* MUX FUNCTION *************************
45010 Y=(YO AND LN(YC)) OR (Y1 AND YC) OR (YO AND Y1)
45020 RETURN
45100 REM ******** SHIFT REGISTER FCN*********************
45110 YO=XD:YC=XC:Y1=XL '1ST MUX, CLOCKS IN XD ON CLOCK LOW
45120 GOSUB 45000 :GOSUB 45200         'MUX FCN AND SET,RESET
45130 YL=Y:YO=XQ: GOSUB 45000:GOSUB 45200 ' " " " AFTER STORING LATCH
45140 RETURN
45200 REM ***** SET AND RESET FUNCTION ***********
45210 Y= (Y OR LN(XS)) AND XR: RETURN
45300 REM ******* MUX AND DFF **********************
45310 YO=DO:Y1=D1:YC=XM:GOSUB 45000      'DO MUX
45320 XD=Y:GOSUB 45100                   'DO DFF
45330 RETURN
50000 DATA MACRO MUX
50010 DATA MUX   AO    A1    C     0     0     Q
50020 DATA AND   AO    C-    0     0     0     X1
50030 DATA AND   A1    C     0     0     0     X2
50040 DATA AND   AO    A1    0     0     0     X3
50050 DATA OR    X1    X2    X3    0     0     Q
50060 DATA NAND  C     0     0     0     0     C-
50070 DATA END
50080 DATA MACRO MUXD
50090 DATA MUXD  AO    A1    C     CLK   RSET Q
50100 DATA MUX   AO    A1    C     0     0     D-IN
50110 DATA DFF   D-IN  0     CLK   RSET 0     Q
50120 DATA END
50130 DATA MACRO CNTRM
50140 DATA CNTRM D1    LOAD  CLOCK  ENAB  RSET Q1
50150 DATA *     D2    0     0      0     0    Q2
50160 DATA *     D3    0     0      0     0    Q3
50170 DATA *     D4    0     0      0     0    Q4
50180 DATA AND   ENAB  0     0      0     0    E1
50190 DATA XOR   E1    Q1    0      0     0    DC1
50200 DATA MUXD  DC1   D1    LOAD   CLOCK RSET Q1
50210 DATA AND   ENAB  Q1    0      0     0    E2
50220 DATA XOR   E2    Q2    0      0     0    DC2
50230 DATA MUXD  DC2   D2    LOAD   CLOCK RSET Q2
50240 DATA AND   ENAB  Q1    Q2     0     0    E3
50250 DATA XOR   E3    Q3    0      0     0    DC3
50260 DATA MUXD  DC3   D3    LOAD   CLOCK RSET Q3
50270 DATA AND   ENAB  Q1    Q2     Q3    0    E4
50280 DATA XOR   E4    Q4    0      0     0    DC4
50290 DATA MUXD  DC4   D4    LOAD   CLOCK RSET Q4
50300 DATA END
50500 DATA ELEMENTS
50510 DATA CNTR DATAO  ENABLE CLOCK  LOAD RSET     QO
50520 DATA *     DATA1  0     0      0     0        Q1
50530 DATA *     DATA2  0     0      0     0        Q2
50540 DATA *     DATA3  0     0      0     0        Q3
50550 DATA CNTRM DATAO LOAD  CLOCK  ENABLE  RSET    QOM
50560 DATA *      DATA1 0     0      0       0       Q1M
50570 DATA *      DATA2 0     0      0       0       Q2M
50580 DATA *      DATA3 0     0      0       0       Q3M
50590 DATA END
60000 DATA EXTERNALS
60010 DATA P CLOCK 0 5 10
60020 DATA A RSET  0 0 2
60030 DATA A ENABLE 1 20 100 150 170 200
60040 DATA A DATAO 0 0 10 160
60050 DATA A DATA1 1 0 10 160
60060 DATA A DATA2 0 0 10 160
60070 DATA A DATA3 1 0 10 160
60080 DATA A LOAD  1 10 20 220 250
60090 DATA END
65000 DATA OUTPUTS
65010 DATA DATA1 DATA2 CLOCK LOAD ENABLE RSET
65020 DATA QO QOM Q1 Q1M Q2 Q2M Q3 Q3M
65030 DATA END
```


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Information Hiding
A Brief Example

Consider this helpful alternative to structured programming and modular design.

Gregg Williams
Senior Editor

While writing the display routine for a game-related program, I decided against a possible change in implementation detail because it would require me to rewrite almost the entire program. This is not an unusual situation for programmers to find themselves in. Had it not been for a vague memory that brought two words to mind, I probably would have continued to find myself in the same situation in years to come. The words were *information hiding*, recalled from an article I had read some time ago. They prompted me to do some thinking about program design, and the work I did refining the display routine algorithm became the basis for the material in this article.

The DRAWCUBE Problem

The problem was simple: I had a 3 by 3 cube (the Rubik's Cube puzzle), with each 1 by 1 square on the face of the cube being one of six colors; the task was to display the state of the cube on the video display of the computer I was programming. I quickly settled on the details of the representation: a given cube could be described by 54 consecutive bytes of memory (the larger problem to be solved—writing a game-related program—dictated that a large number of cube images had to be simultaneously stored in memory); each 1 by 1 square (to be called a *unit* for the rest of this article) was to be stored as a number from 1 to 6 in 1 byte of memory, with the sequence of bytes being taken as six faces of 9 bytes each and the units of a face being stored in row-major order. Also, the cube was to be displayed as a "cross" of six squares that fold together to make a cube (see figure 1).

```
    444
    444
    444

555 666 111 222
555 666 111 222
555 666 111 222

    333
    333
    333
```

Figure 1: *Initial display for DRAWCUBE problem. Each 3 by 3 square of numbers represents one face of a cube. The six faces fold together in three dimensions to represent the cube.*

With these representation choices already decided, I wrote the program DRAWCUBE1, shown in listing 1. The program is straightforward in design. The subroutine DRAWFACE draws one face as a 3 by 3 square, starting at the current cursor position. The subroutine UPDATEBASE positions the cursor to the upper left-hand corner of the next face to be drawn. Finally, the main program coordinates these two subroutines, thus displaying the cube represented in memory starting at the location BEGINCUBE. What could be simpler?

I found to my dismay that a lot of things could be simpler. The one change I rejected (because of the rewriting it would necessitate) led to another and another until I had a list of what-if suppositions, each of which would require major revisions to the DRAWCUBE program. For example:

• What if units were packed two to a byte?
• What if I wanted a perspective display that shows only three faces of the cube?
• What if each unit that had not changed since the last display were flagged in the top bit of its representation in memory?

These and other disruptive changes are listed in table 1.

Alternate Solutions

Design by flowcharting: My first attempt at writing the DRAWCUBE program represents a superficial level of design that most of us usually work at; it could easily be called "design by flowcharting" because it draws heavily on the structure of the coded program that the programmer already has in mind.

Even though the program in listing 1 uses structured programming, which is generally considered to be good programming practice, there is something vitally wrong with it. The flaw is invisible until you extrapolate to a program a thousand times the size of this one. It then becomes obvious that the program in question requires detailed knowledge of the implementation decisions made before the program was designed or coded. A well-written program, however, should be as independent of implementation decisions as possible; it should concentrate on the details of the *algorithm*, not the details of the implementation decisions.

Design by decomposition into modules: A somewhat deeper analysis of the problem might result in the design of the program as a series of modules, each of which is as independent of the others as possible. In such a simple example as I am considering here, the modules represent the three basic actions of any program—input, process, and output—as follows: input the cube from memory into a three-dimensional array; do any processing on the array that might be required (in this example, nothing); and display (or output) the cube on the video display screen.

This modular approach separates code *temporally*. For example, the cube contents are copied into an array before any processing or display operations take place; because of this, any change in the way a cube is stored can affect code only up to the point at which the cube is copied into the array. This temporal isolation of implementation decisions is a step in the right direction, but it is still somewhat related to the "design-by-flowcharting" philosophy. It is possible to obtain further separation by *functional* isolation of implementation decisions.

Design using information hiding: The premise of information hiding is to write a series of modules that hide implementation decisions from all other modules. Although this cannot always be carried out fully, the attempt to hide as much implementation information as possible results in programs that are increasingly less sensitive to implementation changes.

These modules are of a different sort from those previously discussed. They are instead groups of functions that provide a certain behavior when viewed from outside the module. In this way, the main program is provided with a set of modules that appear as "black boxes" to each other: the modules (boxes) can operate knowing only *what* functions the other modules provide; ideally, they are totally independent of *how* another module accomplishes its objective.

Nor are these modules necessarily used sequentially; in many cases, the main program uses several modules repeatedly to accomplish a given task. (This is the case with the DRAWCUBE2 example given in listing 2.) This switching among modules is a potential source for a severe decrease in program speed, especially if the program is large enough so that successive modules have to be swapped in and out of memory to be executed. However, this problem can usually be avoided by proper module design.

In the case of the problem given here, program DRAWCUBE2 (see listing 2) is divided into three modules: CREATEARRAY, which creates *the appearance of* an array CUBE (*facenum, rownum, colnum*) that allows other modules to access any unit of the cube; PROCESSARRAY, which manipulates the information to be displayed; and DISPLAYARRAY, which displays the processed information. These are conceptual modules that are implemented by one or several procedures and functions in this Pascal program. Table 2 lists and describes the modules and lists their component procedures and functions.

Comparison of Algorithms

The algorithm of DRAWCUBE2 is distinguished from that of DRAWCUBE1 and the modular approach discussed above in its use of *transactions* to separate the manipulation of the information to be displayed from the actual display of the same information. The subroutine GENERATETRANS generates transactions until it signals the end of the algorithm by setting the SITUATION flag to ALLDONE. A transaction is defined as a quartet of numbers (*facenum, rownum, colnum, colornum*), which is the minimal number that can completely describe an arbitrary unit for display by the DISPLAYARRAY module.

Consider the "normal-array-with-flag" change listed in table 1. The DRAWCUBE1 program would have to be changed in several places to accept the new cube format. The hypothetical modular program (call it DRAWCUBEM, with modules READCUBE and DISPLAYCUBE) would have to change both its modules: the change to READCUBE follows from the fact that the input format has been changed; the change to DISPLAYCUBE results from the necessity of skipping over units that remain unchanged from the last display operation. (I use the word necessity because the only reason for storing the units with flags is to speed up the display process by discarding the transactions of unchanged units.)

The information-hiding DRAWCUBE2 program handles the display operation so that the main program does not have to change when the input is changed to include flagged data. It does this by burdening the

	Implementation Change	Details
1.	Packed sparse Boolean array	The cube is represented as six strings of 54 bits each, one string for each color as given by a predefined sequence of colors. The 54 bits represent the 54 units (6 faces times 9 units per face) that make up the cube. A 1 bit in the 54-bit substring represents the presence of the associated color on the corresponding unit of the cube, while a 0 represents its absence. This method occupies 324 bits or 40.5 bytes to represent the cube.
2.	Cube stored on disk	The 54 bytes of the original 1-byte-per-unit method are stored in one sector of a floppy disk.
3.	Packed array	The cube is represented in the original manner except that the color numbers of units are represented as 4-bit numbers and packed two to a byte. This method occupies 28 bytes to represent the cube.
4.	Normal array with flag	This method assumes that the cube is already displayed on the video display. The top bit of a byte representing a unit can be 1 to represent the need of updating the unit or 0 otherwise. This scheme might be used to decrease the time needed to display the new representation of the cube.
5.	User viewpoint modification	Before the cube is displayed, the user can specify one of several rotations as multiples of a quarter turn around any of the three axes of the cube.
6.	Printed output	The cube is to be printed out in the "cross" format instead of being displayed on the video display.
7.	Perspective display	The video display shows a perspective view that leaves three faces visible. Each unit may be represented by either its color number or a diamond shape of the appropriate color.

Table 1: *A list of possible implementation changes to the DRAWCUBE problem.*

Module	Component Functions and Procedures	Purpose of Module
CREATEARRAY	INITARRAY CUBE	Once this module has been executed, calls to CUBE give the impression to the calling module that the contents of the given cube are stored in a three-dimensional array CUBE (*facenum, rownum, colnum*).
PROCESSARRAY	INITGENERATE GENERATETRANS	This module acts on the "array" CUBE to generate a series of transactions that, together, completely describe the cube to be displayed.
DISPLAYARRAY	INITPUT PUTTRANS FLUSHARRAY	This module contains the necessary subfunctions to ensure that the cube is displayed properly.

Table 2: *Modules within program DRAWCUBE2, the Pascal procedures and functions that represent them, and their purposes.*

transaction-generating routine (GENERATETRANS) with the task of discarding units that do not need to be redisplayed. Although this change is one of repositioning, not simplifying, a design guided by information-hiding principles might indeed result in simplifying the process of program conversion if the overall program were big enough. In any case, the main program of DRAWCUBE2 seems much more solid and un-

Change	Implementation Details Changed	Modules Needing to Be Changed (Y = yes, N = no)							
		DRAWCUBE1			DRAWCUBEM		DRAWCUBE2		
		UPDB	DRAW	INIT	READ	DISP	CRTE	PROC	PUT
1. Packed sparse Boolean array	input	N	N	Y	Y	N	Y	N	N
2. Cube stored on disk	input	N	N	Y	Y	N	Y	N	N
3. Packed array	input	N	N	Y	Y	N	Y	N	N
4. Normal array with flag	input and process	N	Y	Y	Y	Y	Y	Y	N
5. User-viewpoint modification	process	N	N	Y	N	Y	N	Y	N
6. Printed output	output	Y	Y	Y	N	Y	N	N	Y
7. Perspective display	output	Y	Y	Y	N	Y	N	N	Y

Abbreviations:
INIT = INITIALIZE
READ = READCUBE
CRTE = CREATEARRAY
UPDB = UPDATEBASE
DISP = DISPLAYCUBE
PROC = PROCESSARRAY
DRAW = DRAWFACE
PUT = PUTARRAY

Table 3: *A table of implementation changes and the modules affected by them.*

shakable than the corresponding main programs of DRAWCUBE1 and DRAWCUBEM.

Table 3 further displays the merits of information hiding by listing the modules in the current program version that would have to be altered to accommodate the change specified in the first column. Study of the results for DRAWCUBE1 (and reflection on the duties of each module within) point up the imbalance among the modules: modules INITIALIZE and UPDATEBASE deal only with the output phase of the task, while module DRAWFACE incorporates aspects of the input, process, and output phases. This results in its being modified for every change listed. It is true that, in all versions of the DRAWCUBE problem, all the changes discussed in this article result in only one or two modules being changed; but in a more complex problem, several modules may share the lack of information hiding displayed here by module DRAWFACE, thus making the process of changing an existing program more difficult and unmanageable.

Similar analysis of the two modules of DRAWCUBEM shows a cleaner separation of functions as a result of an emphasis on modularity. Module READCUBE is affected only by changes in the input format, while module DISPLAYCUBE is affected by changes in the process and output phases. The modules of DRAWCUBE2, however, show the greatest separation; modules CREATEARRAY, PROCESSARRAY, and

PUTARRAY are affected only by changes in input, process, and output phases, respectively.

Even though the differences between the modular program, DRAWCUBEM, and the information-hiding program, DRAWCUBE2, are minimal, the latter has a noticeable edge in modularity in that all the program changes discussed in tables 1 and 3 could be made without changing the main program routine. This explains the use of empty modules like INITARRAY and FLUSHARRAY; in other versions of this program, these modules might perform some needed function.

One final observation should be made about the difference in size of the program DRAWCUBE1 (which is highly implementation-dependent) when compared to DRAWCUBE2 (which is highly implementation-independent). The compactness of DRAWCUBE1 is specifically due to its ability to take shortcuts because of its knowledge of the specific implementation details. Conversely, DRAWCUBE2 is longer because it assumes no knowledge of these details and so must work harder to accomplish the same results.

For example, consider the output sections of both programs. DRAWCUBE1 must position the cursor only once every three units because it knows that the cursor will be in position for the next (sequential) unit on the same row. DRAWCUBE2, in assuming that the transactions might come in any order, must reposition the cursor for each unit.

The Case for Information Hiding

The advantages of information hiding include the increased separation among modules and the increased ease of making large implementation-based changes to the program. Its disadvantages include the increased size and execution time of the resulting program. The following paragraphs describe several situations that indicate the use of information hiding techniques:

- You should use information hiding for large programs, especially those designed in an uncertain environment. Examples of this are software designed before or during the choice of computer hardware and software that will be run on leased equipment, on several computer systems, or on equipment due to change.
- Information hiding is also appropriate for programs that are likely to be maintained over an indefinite period of time, especially programs written for a business environment. For example, it makes more sense to use information hiding if you know that someone will probably be modifying the program five years from now; it makes less sense if the program will be written, used several times, then discarded.
- Information hiding is useful if the amount of data being manipulated by the program might greatly increase in the future. Such an increase indicates the possibility of changing to another form of data storage, and such a change might be feasible only if the existing program has been designed to anticipate it.

Conclusions

Information hiding is a technique of program design that confines implementation-dependent details to as few modules as possible and organizes the modules to present a predefined appearance to all other modules. Because the implementation details are not visible to other modules, the program can be modified by changing only those modules that hide the pertinent details.

Information hiding is most appropriate to large programs that are to be maintained over long periods of time. The advantage of flexibility in the face of unknown future changes is offset by the disadvantages of larger program size and longer execution time, but these disadvantages can be controlled given proper planning.

Due to the necessary limitations in its size for tutorial purposes, the example given here does not correctly show the relative advantages and disadvantages of using information hiding; the advantages are more pronounced in a larger program (where a version of the program not using these techniques might be less receptive to implementation changes and where the increase in program size becomes proportionally smaller as the program size increases).

The disadvantages of increased program size and execution times are minimized by the extremely low cost of computer memory and the increasingly faster computers currently being manufactured. The most significant expense today is the time spent by the programmer in writing and, more important, *maintaining* a program. Any techniques (of which information hiding is only one) that increase a programmer's productivity should be seriously considered.■

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2. Ross, D. T., J. B. Goodenough, and C. A. Irvine. "Software Engineering: Process, Principles, and Goals." In P. Freeman and A. I. Wasserman (eds.), *Tutorial on Software Design Techniques* (3rd ed.). New York: IEEE Computer Society, 1980.

Listing 1: *Program DRAWCUBE1.*

```
PROGRAM DRAWCUBE1;

{  The purpose of this program is to simulate
   an algorithm that draws onscreen the six
   faces of a 3 by 3 by 3 cube stored in memory.
   In this implementation, each 1 by 1 "unit"
   is represented as anumber from 1 through 6,
   and the cube is drawn on the screen as shown
   in figure 1. }

   CONST RANK=3;
         MAXFACES=6;

TYPE  SCREENCONSTANTS=ARRAY[1..6] OF INTEGER;

      ONE_TO_MAXFACES=1..MAXFACES;

      ONE_TO_RANK=1..RANK;


VAR  BASEROW, BASECOLUMN, CURRENTFACE,
          CUBEBEGIN, MEMPOINTER: INTEGER;

    MEMORY: ARRAY[1..180] OF ONE_TO_MAXFACES;

    FACE_ROW_BEGIN, FACE_COL_BEGIN:
                        SCREENCONSTANTS;
```

Listing 1 continued:

```
PROCEDURE SIMULATEMEMORY;

{  This procedure is included only for the
   purpose of simulating the computer memory
   used to store the characteristics of one
   or more cubes.  Strictly speaking, this
   routine is not part of the DRAWCUBE
   algorithm.  }

VAR I, J, SUBSC: INTEGER;

BEGIN

  CUBEBEGIN:=19;
  MEMPOINTER:=CUBEBEGIN;

  FOR I:=1 TO 20 DO
     FOR J:=1 TO 9 DO
        BEGIN
           SUBSC:=J+9*(I-1);
           MEMORY[SUBSC]:=(I MOD 6)+1
        END;

END { SIMULATEMEMORY };


PROCEDURE INITIALIZE;

{  FACE_ROW_BEGIN[N] and FACE_COL_BEGIN[N]
  give the row and column position of the
  cursor at the beginning of the Nth face.   }

BEGIN
   FACE_ROW_BEGIN[1]:=3; FACE_COL_BEGIN[1]:=13;

   FACE_ROW_BEGIN[2]:=FACE_ROW_BEGIN[1] + 5;
   FACE_ROW_BEGIN[3]:=FACE_ROW_BEGIN[1] + 5;
   FACE_ROW_BEGIN[4]:=FACE_ROW_BEGIN[1] + 5;
   FACE_ROW_BEGIN[5]:=FACE_ROW_BEGIN[1] + 5;
   FACE_ROW_BEGIN[6]:=FACE_ROW_BEGIN[1] + 10;

   FACE_COL_BEGIN[2]:=FACE_COL_BEGIN[1] - 8;
   FACE_COL_BEGIN[3]:=FACE_COL_BEGIN[1];
   FACE_COL_BEGIN[4]:=FACE_COL_BEGIN[1] + 8;
   FACE_COL_BEGIN[5]:=FACE_COL_BEGIN[1] + 16;
   FACE_COL_BEGIN[6]:=FACE_COL_BEGIN[1]

END { INITIALIZE };


PROCEDURE UPDATEBASE;

{  This procedure updates variables BASEROW
   and BASECOL to the correct values for the
   beginning of the next face.  }

BEGIN
  BASEROW:=FACEROWBEGIN[CURRENTFACE];
  BASECOLUMN:=FACECOLBEGIN [CURRENTFACE];
END;


PROCEDURE DRAWFACE;

{  This procedure draws one face (9 units)
   of a cube starting at the current cursor
   and BASEROW positions.  }

  VAR CURRROW, CURRCOL:INTEGER;

  BEGIN
    FOR CURRROW:=1 TO 3 DO
    BEGIN
      BASEROW:=BASEROW+1;
      GOTOXY (BASECOLUMN, BASEROW);
```

Listing 1 continued on page 450

Listing 1 continued:

```
      FOR CURRCOL:=1 TO 3 DO
        BEGIN

        WRITE (MEMORY [MEMPOINTER]);
        WRITE (' ');
        MEMPOINTER:=MEMPOINTER+1;

        END;

      WRITELN;

    END;

  END { DRAWFACE };


BEGIN { MAIN PROGRAM }

  SIMULATEMEMORY;
  INITIALIZE;

  FOR CURRENTFACE:=1 TO 6 DO

    BEGIN
      UPDATEBASE;
      DRAWFACE;
    END;

END { MAIN PROGRAM }.
```

Listing 2: *Program DRAWCUBE2.*

```
PROGRAM DRAWCUBE2;

{  The purpose of this program is to simulate
   an algorithm that draws onscreen the six
   faces of a 3 by 3 by 3 cube stored.in memory.
   In this implementation, each 1 by 1 "unit"
   is represented as anumber from 1 through 6,
   and the cube is drawn on the screen as shown
   in figure 1. }


CONST RANK=3;
      MAXFACES=6;

TYPE  TYPESITN=(BEGINNING, NEXTCOL, NEXTROW,
       NEXTFACE, ALLDONE);

      SCREENCONSTANTS=ARRAY[1..6] OF INTEGER;

      ONE_TO_MAXFACES=1..MAXFACES;

      ONE_TO_RANK=1..RANK;

VAR   COLORNUM:ONE_TO_MAXFACES;

      FACENUM :ONE_TO_MAXFACES;

      ROWNUM, COLNUM:ONE_TO_RANK;

      SITUATION:TYPESITN;

      FACE_ROW_BEGIN, FACE_COL_BEGIN:
                      SCREENCONSTANTS;
```

Listing 2 continued:

```
      CUBEBEGIN:INTEGER;

      MEMORY:ARRAY[1..180] OF ONE_TO_MAXFACES;


PROCEDURE SIMULATEMEMORY;

{  This procedure is included only for the
   purpose of simulating the computer memory
   used to store the characteristics of one
   or more cubes.  Strictly speaking, this
   routine is not part of the DRAWCUBE
   algorithm.  }

VAR I, J, SUBSC: INTEGER;

BEGIN

  CUBEBEGIN:=19;

  FOR I:=1 TO 20 DO
     FOR J:=1 TO 9 DO
        BEGIN
           SUBSC:=J+9*(I-1);
           MEMORY[SUBSC]:=(I MOD 6)+1
        END;

END { SIMULATEMEMORY };


{ -------- begin module CREATEARRAY -------- }

PROCEDURE INITARRAY;

BEGIN

   { In this version, INITARRAY
     is empty. }

END { INITARRAY };


FUNCTION CUBE (FACENUM, ROWNUM, COLNUM: INTEGER)
                                  :INTEGER;

{  This function returns the value of the unit
   that is in face FACENUM, row ROWNUM, and
   column COLNUM of the current cube as defined
   by the pointer CUBEBEGIN.  }

VAR   UNITS_IN_FACE:INTEGER;
      UNITS_IN_ROW :INTEGER;
      CURRENTUNIT:INTEGER;

BEGIN

   UNITS_IN_FACE:=RANK*RANK;
   UNITS_IN_ROW :=RANK;

   CURRENTUNIT:=CUBEBEGIN
     + (FACENUM-1) * UNITS_IN_FACE
     + (ROWNUM -1) * UNITS_IN_ROW
     + (COLNUM -1);

   CUBE:=MEMORY[CURRENTUNIT]

END { CUBE };


{ -------- begin module PROCESSARRAY -------- }

PROCEDURE INITGENERATE;

{  This procedure must be executed once
   before GENERATETRANS is valid.  }

BEGIN
```

Listing 2 continued on page 452

Listing 2 continued:

```
    SITUATION:=BEGINNING

END ( INITGENERATE );


PROCEDURE GENERATETRANS;

{  This procedure generates one 4-tuple
   (facenum, rownum, colnum, colornum)
   to be processed by PUTTRANS.  }

BEGIN

   IF (SITUATION <> BEGINNING) THEN
      BEGIN
         IF (COLNUM < RANK)  THEN SITUATION:=NEXTCOL;

         IF (COLNUM >= RANK)  AND  (ROWNUM < RANK) THEN
            SITUATION:=NEXTROW;

         IF (COLNUM >= RANK)  AND  (ROWNUM >= RANK)
          AND  (FACENUM < MAXFACES)  THEN
            SITUATION:=NEXTFACE;

         IF (COLNUM >= RANK)  AND  (ROWNUM >= RANK)
          AND  (FACENUM >= MAXFACES)   THEN
            SITUATION:=ALLDONE
      END;

   CASE SITUATION OF

      BEGINNING: BEGIN
                    FACENUM:=1;
                    ROWNUM :=1;
                    COLNUM :=1;
                    SITUATION:=NEXTCOL
                 END;
```

Listing 2 continued:

```
      NEXTCOL   : COLNUM:=COLNUM + 1;

      NEXTROW   : BEGIN
                     COLNUM:=1;
                     ROWNUM:=ROWNUM + 1
                  END;



      NEXTFACE : BEGIN
                    COLNUM:=1;
                    ROWNUM:=1;
                    FACENUM:=FACENUM + 1
                 END;

      ALLDONE  : { DO NOTHING }

   END ( CASE );

   COLORNUM:=CUBE(FACENUM, ROWNUM, COLNUM)


END ( GENERATETRANS );


{ -------- begin module DISPLAYARRAY -------- }

PROCEDURE INITPUT;

{  This module initializes the two arrays
   FACE_ROW_BEGIN and FACE_COL_BEGIN, which
   are used to simplify cursor position
   calculations within PUTTRANS.  }

BEGIN

   FACE_ROW_BEGIN[1]:=3; FACE_COL_BEGIN[1]:=13;
```

Listing 2 continued:

```
    FACE_ROW_BEGIN[2]:=FACE_ROW_BEGIN[1] + 5;
    FACE_ROW_BEGIN[3]:=FACE_ROW_BEGIN[1] + 5;
    FACE_ROW_BEGIN[4]:=FACE_ROW_BEGIN[1] + 5;
    FACE_ROW_BEGIN[5]:=FACE_ROW_BEGIN[1] + 5;
    FACE_ROW_BEGIN[6]:=FACE_ROW_BEGIN[1] + 10;

    FACE_COL_BEGIN[2]:=FACE_COL_BEGIN[1] - 8;
    FACE_COL_BEGIN[3]:=FACE_COL_BEGIN[1];
    FACE_COL_BEGIN[4]:=FACE_COL_BEGIN[1] + 8;
    FACE_COL_BEGIN[5]:=FACE_COL_BEGIN[1] + 16;
    FACE_COL_BEGIN[6]:=FACE_COL_BEGIN[1];

END { INITPUT };



PROCEDURE PUTTRANS(FACENUM, ROWNUM,
             COLNUM, COLORNUM: INTEGER);

{  This procedure puts one transaction to the
   output device.  }

VAR   CURR_ROW_LOCATION:INTEGER;
      CURR_COL_LOCATION:INTEGER;

BEGIN

    CURR_ROW_LOCATION:=FACE_ROW_BEGIN[FACENUM]
                       + (ROWNUM - 1);

    CURR_COL_LOCATION:=FACE_COL_BEGIN[FACENUM]
                       + 2 * (COLNUM - 1);

    GOTOXY(CURR_COL_LOCATION, CURR_ROW_LOCATION);

    WRITELN(COLORNUM)

END { PUTTRANS };
```

Listing 2 continued:

```
PROCEDURE FLUSHARRAY;

{  This routine is used to trigger stored
   results to be output (in versions that
   cannot completely process a transaction
   within PUTTRANS).   }

BEGIN
   { In this version, FLUSHARRAY
      is empty.   }
END { FLUSHARRAY };


{ -------- begin main program -------- }

BEGIN { MAIN PROGRAM }

   SIMULATEMEMORY;

   INITARRAY;
   INITGENERATE;
   INITPUT;



   WHILE SITUATION <> ALLDONE DO

      BEGIN

         GENERATETRANS;
         PUTTRANS (FACENUM, ROWNUM, COLNUM,
                                COLORNUM)
      END;

   FLUSHARRAY

END { MAIN PROGRAM }.
```

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Adventures (#1-12)	129	97
American Training International, Inc.		
ATI-Power for CP/M	75	54
Anderson-Bell		
ABSTAT		359
Artificial Intelligence		
(Requires CBASIC 2)		
Medical	995	749
Dental	995	749
Ashton Tate		
dBase II [4]	700	425
Aspen Software		
Grammatik	75	56
Proofreader	50	38
Balcones		
The Boss: Financial Accounting System	2495	1496
Byrom Software		
BSTAM (Micro to micro comm.)	200	144
BSTMS (Micro to mainframe comm.)	200	144
Caxton		
Cardbox	245	177
Centa Systems		
CP/M Northstar (Horizon only)	179	150
CP/M Micropolis	189	156
Computer Control		
FABS (B-TREE file access)	195	146
Ultrasort II	195	146
Computer Development, Inc.		
Image	495	356
Comshare Target Software		
Plannercalc	50	38
Masterplanner	325	263
Condor Computer Corp.		
Condor 1	195	147
Condor 3	650	488
Data Base Solutions		
dNAMES		129
Designer Software		
Palantir	425	319
Digital Research		
Access Manager	300	225
MAC (macro assembler)	90	75
SID (symbolic debugger for 8080)	75	63
ZSID	100	88
CBASIC (language)	150	94
CB80	500	395
CIS COBOL	800	595
Display Manager	400	295
Pascal Mt+ w/SPP	500	395
DJR Associates		
FMS 80	995	625
FMS 80-1	495	312
FMS 80-2	495	312
Ecosoft		
MicroStat (stat package)	295	248
Epic Computer Corp.		
Supervyz	150	94
Faircom		
MICRO B+ (Keyed file accessing)		
For CBASIC 2	260	211
For MBASIC, COBOL, PL1/80, FORTRAN, Pascal MT+, CB 80	260	211
Fox and Geller		
dGRAPH	295	195
Quickscreen	149	125
Quickcode	295	195
dUTIL	99	59
FYI		
Superfile	195	129
Infocom		
Deadline	60	43
Zork I, II, III (ea.)	50	38
Star Cross	50	38
ISA (See Sorcim)		
ISM		
Mathemagic	99	72
Ithaca Intersystems		
Pascal Z	450	375
Pascal BZ (64K)	450	375
Pascal Z and BZ	650	542
Lexisoft		
Spellbinder	495	281
Lifeboat		
T-Maker II	275	215
Mark of the Unicorn		
Mince (text editor)	200	136
Final Word	300	229
Micro Pro		
Infostar [5]	495	327
Report Star	350	231
Wordstar [4]	495	327
MailMerge	250	165
Wordstar/MailMerge		426
Spellstar [4]	250	165
Wordstar/Spellstar [4]	695	426
Word/Spell/Mail [4]	845	558
Calcstar	145	96
Datastar	295	195
MicroSoft		
BASIC 80	350	252
BASIC Compiler	395	284
FORTRAN 80	500	360
COBOL 80	750	540
MACRO 80	200	156
EDIT 80	120	94
μ Math/μ Simp	250	194
μ LISP/μ Star	200	156
M-Sort	195	151
Multiplan	275	179
Microstuf		
CrossTalk	195	119
Northwest Analytical		
Statpak	495	369
OASIS		
The Word Plus	150	112
Organic Software		
Datebook	295	229
Milestone	295	229
Peachtree		
Series 4 Peach Pak (GL,AR,AP)	595	359
Pickles and Trout		
CP/M TRS 80 Mod II	185	169
Quality Software		
GBS-DB Apple Dev. Program	650	505
Relational Systems, Int.		
Personal Pearl	295	184
Select Information Systems		
Select with Superspell	595	369
Software Dimensions		
Accounting Plus™		
GL, AR, AP, Inv each		402
All four		1435
Sorcim		
Pascal/M (Z80 or 8080)	395	284
Pascal/M (8086, 8088)	495	356
ACT 80 (Z80, 8080, 8085)	175	126
ACT 65 (6502)	175	126
ACT 68 (6800)	175	126
ACT 69 (6809)	175	126
ACT 86/88 (8086, 8088)	175	126
TRANS 86	125	90
Spellguard	195	146
SuperCalc	295	185
Superwriter	395	249
Supersoft		
C Compiler	250	188
Ada Compiler	300	225
Systems Plus (see Software Dim.)		
Woolf Software Systems		
Move it	100	66

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HARDWARE

	List	Now
Corona		
5MB Hard Disk [6]	2495	1895
Daisywriter		
Printer [10]	1395	1235
Hayes Microcomputer Products		
Datacom Pascal Package	50	36
Hayes Stack Chronograph (RS-232) [4]	249	199
Hayes Stack Smart-Modem (RS-232) 300 Baud [4]	279	209
Hayes Stack Smart-Modem (RS-232) 1200 Baud [4]	699	509
NEC		
12" Green Hi-Res CRT [10]	285	167
7710 Printer [10]	3085	2295
3530 Printer [10]	2290	1735
8023 Printer [10]	795	520
Novation		
J-Cat [4]	149	119
Smart-Cat 103 [4]	259	207
Smart-Cat 103/312 [4]	595	476

APPLE® BUSINESS

Product	List	Now
Applied Software Technology		
Versa Form:		
VS-1 Apple II/64K	389	249
VH-1 (Corvus)	495	360
VP-1 Versaform Pascal/ Interface	245	180
ARTSCI (Softape)		
Magic Window II (40/70/80)	150	109
Magic Window	100	75
Magic Mailer	70	49
Magic Words	70	49
Magic Pack Combo (Contains all 3)	225	156
Ashton-Tate		
dBase II † [4]	700	425
Avant-Garde Creations		
Ultra Plot/D.I.F./Data Graph	99	71
Beagle Brothers		
Alpha Plot	40	28
DOS Boss	24	17
Utility City	30	22
Apple Mechanic	30	22
Broderbund Software		
General Ledger (with A/P)	495	305
Payroll	395	275
Commsoft		
Roots/M †	195	140
Computer Station		
Combined Enhanced Graphics Software	55	40
Station Master	175	136
Comshare Target Software		
Target PlannerCalc †	99	74
Image Maker	175	126
Continental		
Home Accountant	75	52
1st Class Mail	75	54
CPA #1 — GL	250	159
CPA #2 — AR	250	159
CPA #3 — AP	250	159
CPA #4 — PR	250	159
All four [5]	1000	609
CPA #5 — Property Management	495	352
Crane Software		
Menu Generator	40	29
Creative Curriculum, Inc.		
Speed Reading Courseware	99	75
Dakin 5/Level 10		
Depreciation Planner	395	299
Budget Planner	150	112
Business Bookkeeping System	395	299
Datamost		
Write On II	130	90
Real Estate Analysis Program	130	90
Tax Beater	130	90
Datasoft, Inc.		
Micropainter (48K)	35	25
BASIC Compiler (32K)	100	75
LISP Interpreter	125	94
Decision Support		
The Accountant	129	97
Accountant with DBCalc	149	107
Delta Software		
Bookkeeper Master Program	90	68
Bookkeeper Check Writer	40	29
Denver Software		
Pascal Tutor	125	97
Pascal Programmer	296	223
Financial Partner	250	188
Eduware		
Compu-Read	30	22
Perception	25	19
Statistics	30	22
Spelling Bee with Reading Primer	40	30
Compu-Math/ Fractions	40	30
Compu-Math/ Decimals	40	30
Compu-Math/Arithmetic Skills	50	37
Algebra 1	40	30
Fractions (New version)	49	37
Decimals (New version)	49	37
Algebra 2	40	30
Counting Bee	30	22
Compu-Spell/System	30	22
Compu-Spell/Data Disk Levels 4 thru 8	20	15
Uni-Solve	25	19
PSAT Word Attack Skills	49	37
SAT Word Attack	49	37
Hayden Software		
Pie Writer/Standard	150	108
Pie Writer/Double Vision	150	108
Pie Writer/Multi 80-col (for Smarterm, Videoterm, & Superterm)	150	108
Howard Software		
Creative Financing 1983	195	149
State Tax Prep. CA '83		
Tax Preparer 1983	225	179
Real Estate Analyzer II	195	146
Information Unlimited Software (IUS)		
Datadex	150	108
Datadex/Hard Disk	300	216
Professional Easywriter	175	126
Professional Easymailer	150	108
Easy Mover	100	75
Tellstar Level I	40	30
Tellstar Level II	80	58
FORTH Development System	140	101
Insoft		
GraFORTH II	75	56
Electric Duet	30	23
TransFORTH II	125	94
ALD System II	75	56
International Software Marketing		
Mathemagic (Advanced programmable calculator package)	90	65
Graphmagic	90	65
ISA (See Sorcim)		
Kensington Microware Ltd.		
Format II	250	169
Lightning Software		
Mastertype	40	30
Link Systems		
Datafax	199	149
Datalink	100	75
Link Index	195	149
Link Video	55	41
Link Sampler I	60	45
Link Disk	70	51
LJK Enterprises		
Letter Perfect with Mail Merge	150	112
Data Perfect	100	78
Edit 6502	100	78
Lotus		
Executive Briefing System	199	149
Micro Lab		
The Invoice Factory	200	144
The Merger	50	37
The Learning System	150	108
Painter Power	40	30
US Constitution Tutor	30	22
English SAT #1	30	22
VisiBlend	50	37
VisiFactory	75	54
The Asset Manager	200	144
The Tax Manager	180	129
Data Factory 5.0	300	216
Wall Streeter	300	216
Payroll Manager	300	216
Micropro		
Infostar † [5]	495	327
Report Star †	350	231
Wordstar † [4]	495	327
Wordstar Customization Notes [4]	500	327
MailMerge †	250	165
Wordstar/Mail-merge † [4]	645	426
SuperSort †	250	165
SpellStar †	250	165
DataStar †	295	195
CalcStar †	145	96
Microsoft		
FORTRAN 80 †	195	151
COBOL 80 †	750	584
BASIC Compiler †	395	295
TASC (Applesoft compiler)	175	119
Typing Tutor II	25	19
Time Manager	150	116
A.L.D.S. †	125	97
Adios μMath-80	125	97
Adios μMath/μSimp	250	194
M-Sort	195	151
μLisp/μStar	200	156
Multiplan	275	179
Multiplan †	275	179
MUSE		
Supertext 40/56/70	125	79
Supertext 40/80	175	126
Form Letter Module 48K	100	72
Address Book Mailing List 48K**	50	36
Data Plot 48K**	60	43
Elementary Math Apple Soft 48K**	40	29
The Voice 48K	40	29
**Requires Applesoft, ROM or Apple II Plus		
Oasis		
The Word Plus †	150	112
On-Line Systems		
The General Manager	230	168
Screenwriter II	130	85
The Dictionary	100	70
Expeditor II+ (Applesoft compiler)	135	94
LISA 2.5	80	56
EPFIV (Extended Programming Facility IV)	80	56
LISA Educational Package	120	83
Optimized Systems Software, Inc.		
Speed Read Plus	60	43
Peachtree		
Series 40 GL, AR, AP, Inventory, Payroll (ea)	400	239
Penguin Software		
Complete Graphics System	70	50
Special Effects	40	30
Graphics Magician	60	45
Additional Fonts and Character Sets	20	15
Complete Graphics System II (Apple Tab Ver.)	120	86
Special Effects (Apple Tab Ver.)	70	50
Program Design, Inc.		
The New Step-by-Step	80	58
Quality Software		
GBS-DB Apple Dev. Prog.	700	504
Sensible Software		
Super Disk Copy III	30	23
Multi Disk Catalog III	25	19
Disk Recovery ("The Scanner")	30	23
Image Printer-Letter Quality	40	30
Image Printer-Epson	40	30
Image Printer-NEC Dot Matrix	40	30
The Bug	50	37
Build Using	30	23
Edit Soft	30	23
Quadrant 6112	35	26
Sensible Speller	125	94
• for Supertext	125	94
• for Apple CP/M	125	94
• Pascal	125	94
BEST (Applesoft Program Optimizer)	40	30
Select Information Systems		
Select (with Super-spell)	595	356
Silicon Valley		
Word Handler	199	145
List Handler	90	68
Dictionary	125	94
Sirius		
Pascal Graphics Editor (48K II/II+)	100	69
Sof/Sys, Inc.		
Executive Secretary	250	169
Executive Speller	75	56
Softech Microsystems		
UCSD P-System Software Set [4]	625	450
BASIC Compiler and Runtime Package	225	169
Xenofile	50	39
Softeach	125	90
Software Dimensions		
Accounting Plus™ GL, AR, AP, Inv ea	395	239
All four	1250	669
Software Publishing		
PFS:File	140	99
PFS:Report	125	79
PFS:Graph	140	99
Sorcim		
Spellguard †	195	146
SuperCalc †	295	189
Southeastern Software		
Data Capture 4.0	65	45
Data Capture 4.0/Videx, Smarterm, Superterm	90	65
Southwestern Data		
Z-Term Professional †	150	99
ASCII Express	80	59
ASCII Express Professional	130	89
STC		
Professional Time and Billing	395	284
Language Reading Development Program	175	126
Apartment Manager	325	234
Stoneware		
DBMaster	229	148
Utility Pak #1	99	65
Utility Pak #2	99	65
DBMaster/Hard Disk	499	359
Stat Pac	99	71
Micro Memo	40	30
Electronic Price Sheet	100	72
Compucube	30	22
Graphics Processing System (Standard)	60	45
Graphics Processing System (Professional)	179	129
Synergistic Software		
The Linguist	40	30
The Directory Manager	25	19
Higher Text II	40	30
Higher Graphics II	35	26
Mailing List Data-Base	50	37
Program Line Editor	40	30
Modifiable DataBase	80	59
The Data Reporter	220	158
Integer BASIC Compiler	150	108
Global Program Line Editor	65	49
Data Reporter—Hard Disk	220	158
Versa Computing		
VersaWriter Expansion Pac-I	40	30
VersaWriter Expansion Pac-II	40	30
AXE (Apple Extended Editor)	70	50
VersaWriter Graphics Tablet (accessory)	299	252
VisiCorp (Personal Software)		
VisiCalc II 3.3	250	169
VisiFile	250	169
VisiLink	250	169
Desktop Plan II	250	194
VisiPlot	200	156
VisiTrend/Plot	300	234
VisiDex	250	194
VisiTerm	100	65
VisiSchedule	300	234
Business Forecasting Model (req. VisiCalc)	100	78

APPLE® HARDWARE

Product	List	Now
Hayes		
Micromodem II [4]	379	259
• with terminal pgm	409	289
Kensington		
System Saver (Fan)	90	65
Micro-Sci		
A2 35T Disk Drive [5]	479	329
Microsoft		
RAMcard (memory board)	100	69
Softcard (CP/M board)	345	219
Premium System: Softcard, 16K RAMcard, Videx Videoterm 80 col. Card, Softswitch, Osborne CP/M User Guide [5]	695	489
Personal Computer		
Appli-Card (6MHz)	595	429
Videx		
Keyboard Enhancer II	149	99
Videoterm w/Soft-Switch	375	239

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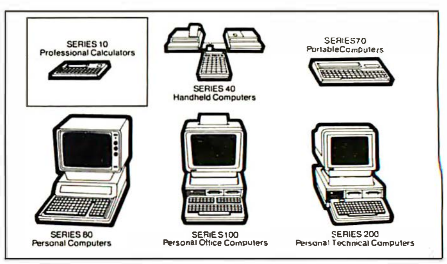
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BYTELINES

News and Speculation about Personal Computing

Conducted by Sol Libes

Random Rumors: Microsoft Inc. and Micropro International Corp. are both working on products to compete with the new Visi On system expected from Visicorp this summer. Visi On is a highly intelligent operating environment for the IBM Personal Computer that allows cursor control using a mouse device. . . . Seagate Technology is expected to introduce shortly two new 5¼-inch Winchester disk drives with capacities of 25 and 33 megabytes. . . . Hitachi Ltd. is reportedly readying an IBM-compatible personal computer for introduction this spring. . . . IBM and TI (Texas Instruments) are said to be jointly working on an IC (integrated circuit) for use in the new IBM LAN (local-area network) system.

It is predicted that at next month's NCC (National Computer Conference) at least 20 companies will introduce 68000-based computer systems running versions of the Unix operating system, at least two firms will demonstrate high-capacity optical disk mass-storage systems, and two or three new portable systems will emerge (probably compatible to some degree with the IBM Personal Computer).

TI is expected to drop the list price of the 99/4A to $149 soon and to introduce a new 64K-byte memory capacity computer with the hope of selling over 1 million computers this year. . . . It is believed that Commodore will also drop the price of the Commodore 64 when it introduces its P500, a 128K-byte machine, at $795. Look for the Commodore 64's price to drop to $399. . . . The price of the Timex/Sinclair 1000 is expected to drop to around $85, which means that we may see it discounted to as low as $60.

Apple Doings: Apple Computer Inc. has committed itself to using the Ethernet LAN system—at least for the coming year. It's rumored that Apple is working on its own LAN system for introduction in 1984. The selection of Ethernet was no doubt based on Apple's attempt to appeal to large corporations, particularly with its Lisa, Mackintosh, and Apple III systems. Apple has entered into a contract with 3Com Corp. to supply the Ethernet hardware, which Apple will then "private label" for resale. The Ethernet interface cards are expected to be available this summer and will sell for between $900 and $1000 apiece. Apple will publish its protocols to encourage the development of Ethernet software by independent software houses.

Sales of the Apple III have no doubt been a big disappointment to Apple. An estimated 60,000 units have been sold in the two years it has been on the market. Sales picked up in the second half of 1982 when Apple cut the price significantly and upgraded the product with larger-capacity floppy-disk drives, an IBM-3270 emulator, and an accounting package. In an attempt to further stimulate sales of the Apple III, Apple offered $100 rebates to floor salesmen on each Apple III they sold.

Analysts and dealers generally agree that the Apple III's lackluster sales are due to a lack of applications software from the independent software industry. They attribute this to the fact that independent software suppliers turned their attention to the IBM Personal Computer and ignored the Apple III. For example, Visicorp and Lotus Development Corp. both introduced significant new software packages for the IBM Personal Computer but do not plan to introduce versions for the Apple III. Their reasoning is that there are already four times as many IBM Personal Computers in operation as there are Apple IIIs and that the ratio is likely to tip even more in IBM's favor by the end of this year. Certainly the already introduced Lisa and the soon-to-be-introduced Mackintosh will have a further impact on sales of the Apple III.

In January, Apple officially introduced its 68000-based Lisa system. The primary marketing effort for this $10,000 machine will be directed to the large-corporation marketplace, traditionally dominated by IBM. No doubt IBM will fight hard to keep it that way. IBM, again demonstrating its marketing prowess, introduced a 68000-based machine more than a month before Apple. The IBM system, however, is directed more to the scientific community, while Apple's Lisa, intended for use as a very intelligent workstation, will be spearheading the "office-of-the-future." Apple appears to have established itself well in the corporate market and is expected to be much more successful with the Lisa than with the Apple III system.

In many ways, the Lisa resembles the Xerox 8010 (the Star), introduced in 1981. The 8010, which sells for $16,000, is at best only a modest commercial success. To ensure the success of the Lisa, Apple has doubled its sales force (now up to 100 people) selling directly to big national customers. Also, Apple has qualified about 200 dealers to sell the Lisa (a move that has angered some of Apple's other 1400 dealers).

In the meantime, the new Apple IIe, the long-awaited upgrade of the Apple II, is having an impact on suppliers of Apple II memory boards. The Apple IIe includes an enhanced memory that makes many current add-on memory boards obsolete. Two of the seven memory-board manufacturers have already decided to cease production of these boards when the demand lessens: Microsoft and Advanced Logic Systems have announced that they do not plan any new Apple II memory boards.

The Apple IIe has one less I/O expansion slot (slot zero is missing) than its predecessor. This position was previously used for the memory-expansion board. Further, the system contains 64K bytes of memory. Several of the other memory-board manufacturers plan to continue to make memory boards to extend the IIe's memory beyond 64K bytes (e.g., for disk emula-

tion).

Apple also cut costs on the Apple IIe by reducing the number of ICs from 109 to 31; however, the retail price of the Apple IIe is $45 more than the old Apple II's $1350. Last year I predicted that the IIe would have an 80-column display (see the October 1982 BYTELINES, page 456); however, Apple has decided to keep the 40-column format but offers the 80-column format as an option. Apple can expect tough competition from IBM, which is expected to introduce two new systems this summer—one lower in price and performance than the current Personal Computer and the other more powerful.

Congress defeated what has been referred to as "the Apple Computer Bill," which would have offered tax breaks to computer manufacturers for donating computers to schools. Opponents argued that the bill would have given Apple a marketing advantage and that the tax benefit would have cost the government $36 million in lost revenues, transferring the cost burden from corporations to the government. Apple Computer Inc. chairman Steve Jobs, who had promoted the bill, had stated publicly that "Congress would be crazy not to take us up on this." It is expected that the bill will be reintroduced in this year's Congress.

Market Share for the PC: International Data Corp., a market-research firm, estimates that, in its first full year of selling the Personal Computer, IBM sold almost 200,000 systems and that this year sales should rise to 350,000 systems. Thus the firm estimates that the IBM Personal Computer has already gained 17.3% of the market, behind Apple's 26.6% and Tandy's 23.3%. International Data Corp. also predicts that next year IBM will be the leader in the personal computer market, a market that keeps doubling each year. It has been estimated that 10% of the IBM Personal Computer systems sold have gone to IBM employees, who get discounts and payment plans for the system. The discount policy encourages IBM employees to write software for the system, often for extra pay.

IBM already dominates the medium-performance $3000-to-$5000 segment of the personal computer market. Already two dozen IBM-compatible machines have been introduced. The standard memory size for IBM-compatible machines now seems to be 256K bytes. Doubtless IBM's new machine, expected this summer, will have 256K bytes of memory onboard.

Although much lower than IBM in dollar volume, Commodore, TI, and Timex Computer Corp. are the leaders in unit volume. Timex Computer is estimated to have shipped 750,000 units last year, and Commodore and TI about 600,000 computers each. Radio Shack and Atari were not far behind. Thus it appears that close to 3 million personal computers were sold last year. With Timex Computer, Commodore, and TI each expected to sell over 1.5 million computers in 1983, we may see over 6 million computers sold this year.

Total sales for this year are expected to top $3 billion. Both Apple and Tandy have disclosed that they are shooting for $1 billion in sales, a 50% increase over last year. Tandy anticipates that its 1983 sales of home systems will top its sales of business systems for the first time. Apple is expected to introduce an under-$500 computer for the home market.

The Year of the Mouse: 1983 will surely go down as the "year of the mouse." Many of the new personal computers due for introduction at next month's NCC will have them as standard features of the system. Apple's new Lisa has a mouse, and it will no doubt be an option on the soon-to-be-announced Mackintosh. Televideo and several others are expected to show their mouse offerings at NCC.

IBM Buys Into Intel: IBM has bought a 12% stake in Intel Corp. The price was $250 million. IBM will have an option to increase this to 30% in eight years, and the firm will also get one representative on the Intel board of directors. No doubt this will tighten the association between the two companies. Intel is the primary supplier of add-on memory boards to IBM and a leading supplier of 64K-bit dynamic-memory ICs. Further, the microprocessor and many of the support ICs used in IBM's Personal Computer, Displaywriter, and Datamaster systems are furnished by Intel. IBM has also purchased rights to some manufacturing technologies from Intel. IBM, which has in the past grown by internal expansion, making virtually all of its own ICs, has become increasingly dependent on outside IC suppliers.

Many other IC makers have been acquired or invested in by large customers. For example: General Electric bought Intersil, Schlumberger Ltd. bought Fairchild, United Technologies bought Mostek, and Siemens Corp. owns a 16% interest in Advanced Micro Devices.

Intel, like other IC makers, has been in a slump for the past two years due to the recession and severe price competition from Japan. While other IC makers resorted to layoffs, Intel increased its staff by 3000 last year, anticipating an upturn that never came. For this year, Intel has cut all salaries by 10% and frozen them for the year. The firm has needed substantial amounts of capital to continue its aggressive research and product development programs. Thus experts speculate that IBM decided to buy a stake in Intel to boost this R & D and thwart a buy-in by a competitor such as AT & T (American Telephone and Telegraph, recently freed from an antitrust suit and reorganized).

Prices Drop: Commodore has been selling its VIC-20 in the U.S. for close to a year at a list price of $180; the price is expected to drop soon to $150 (hence it will be selling for the same price as the Timex Sinclair 2000). The VIC-20 has a better keyboard and better color graphics but less memory. Further, Commodore offers options that include a disk drive. TI is dropping the price of its 99/4A and bringing out a new lower-cost machine, called the 99/2, with a list price of $100. TI will shortly introduce a high-speed tape-storage unit for both the 99/4 and 99/2 with a list price of $140.

Sinclair has been talking about a microfloppy-disk drive for its color system that will sell for under $80. Although the drive will be slow (taking about 4 seconds to load a program), it will store about 100,000 bytes. When this unit becomes available, it should make the Spectrum and its American counterpart, the Timex Sinclair 2000, highly competitive with the VIC-20 and TI units. The machine is expected to be introduced in England this spring and in this country

later this year.

In England the ZX81 is reportedly still outselling the Spectrum (with its color capability) by about 3 to 1. This may be because other systems are competing for the Spectrum's part of the market, especially the Commodore VIC, the BBC Computer, and the Dragon 32 (the latter two sold only in England).

In the meantime, I have seen ads offering the Timex Sinclair 1000 for as low as $74. At this price, the unit may start cutting into the calculator market. Rumor has it that Memotech, a maker of add-on memory units for the ZX81, is working on a 5¼-inch floppy-disk drive add-on that will include the CP/M disk operating system and an enhanced keyboard. Memotech hopes to sell it for about $300, which means that a minimal CP/M system could be put together for under $800. Imagine spending $80 for the computer and another $740 for the rest of the system. In other words, the computer will be the cheapest component in the system.

VIC-20 Tops a Million: Commodore is boasting that more than 1 million VIC-20 machines have already been sold internationally, which would make it the most popular personal computer to date. Commodore admits that most of the VIC-20s have been purchased to play games and that only a small percentage of buyers use the system for educational or personal computer use.

Commodore has determined that its typical customers are young couples, with children between the ages of 9 and 18, who buy the VIC-20 for game playing, with the hope that it will also help educate their children in computer basics. Also, the widespread introduction of personal computers in schools has caused children to pester their parents for home computers because of the necessarily limited access in the school environment. Often parents feel that their children will be deprived if they do not have their own systems; however, parents have found that children are mainly interested in playing games rather than programming.

Computer Hobbyists Meet: On Saturday and Sunday, April 16 and 17, an estimated 15,000 computer hobbyists will flock to their largest annual gathering. The big attraction is an outdoor flea market that covers close to 20 acres. The annual event is now in its eighth year and owns the distinction of being the first of the personal computer shows ever held. Called the Trenton Computer Festival, it will be held on the campus of Trenton State College, Trenton, New Jersey. Buyers, sellers and traders of personal computer equipment set up tables or sell from the tail-gates of their cars everything from complete computer systems to tiny electronic parts.

Speakers, user-group meetings, an indoor commercial exhibitor area, and a banquet will also be featured. The Festival is sponsored by three nonprofit computer clubs: the Amateur Computer Group of New Jersey, Philadelphia Area Computer Society, and Trenton State Computer Society; the funds raised help support these organizations. For information, call (609) 771-2487 or write to TCF-83, Trenton State College, Trenton, NJ 08625.

Flat-Screen Video Status Report: At a recent engineering conference in San Francisco, Siemens AG of West Germany announced a 14-inch color video display that is only 3-inches thick, consumes only 20 watts of power, and is light enough to hang on a wall. Instead of using the traditional electron gun to produce a beam, Siemens employs an electrified gas to produce an electron cloud and a wire matrix to control the cloud. The tube is still in development, with no word on when it will be used in a terminal.

CMOS Gaining in Popularity: MOS (metal-oxide semiconductor) ICs have long been the workhorses of the microcomputer industry; however, many manufacturers are now shifting to CMOS (complementary metal-oxide semiconductor) ICs. CMOS uses far less electrical power than MOS, is more immune to electrical interference, and can operate over a wider range of temperatures. This makes CMOS much more desirable for portable and pocket-type personal computers. The two major drawbacks to CMOS are its higher cost and slower operating speed.

When more functions are squeezed onto a chip, a heat problem develops; a limit is eventually reached as to the number of functions that can be put into an IC package. Thus IC manufacturers are looking to CMOS to allow greater functionality of ICs. Intel, one of the last to jump on the CMOS bandwagon, expects that by 1985 half of its products will use CMOS.

CMOS was invented by RCA way back in 1961. The largest supplier of CMOS ICs today is Motorola, which (because of CMOS) has surpassed TI as the largest IC manufacturer in the world.

Low-Cost Voice-Input System: Milton Bradley, the toy manufacturer, has introduced a voice-input system for the TI 99/4A computer. The company originally intended to enter the personal computer market, but changed its mind when prices dropped to the under-$200 level. The voice-input system will sell for under $100 and will recognize 10 to 12 words commonly used in games.

It's interesting to note that other voice-input systems currently on the market start at over $1000. Back in 1978, Heuristics Inc. introduced a voice-input system for the Apple II that sold for $300. However, very few were purchased, and the company went out of business. It should be interesting to see how well Milton Bradley does with its unit and whether a consumer market develops for voice-input systems.

Random News Bits: Digital Equipment Corp. has agreed to distribute the Bridge software package from Virtual Microsystems Inc. The Bridge allows CP/M-based software to run on DEC minicomputers. . . . Brattle Research Corp. of Boston, Massachusetts, predicts that robots and other intelligent machines could replace an estimated 30% of manufacturing jobs. . . . Osborne Computer, seeking to increase the size of its market, is signing up office-equipment dealers to handle its portable computer. Osborne has also increased dealer margins to 42% on large volume purchases, while increasing system prices to $1800 (single density) and $2000 (dual density).

It's rumored that Intel, Motorola, and National Semiconductor plan to add a new op code to the instruction set for their microcomputers, to be called BFM, the mnemonic for the instruction "be fruitful and multiply". . . . Happy April first.

MAIL: I receive a large number of letters each month as a result of this column. If you write to me and wish a response, please include a self-addressed, stamped envelope.

Sol Libes
c/o BYTE Publications
POB 372
Hancock, NH 03449

Clubs and Newsletters

Forum for Sinclair Users

Sinclair Micronews contains programs, tutorials, and user reports on hardware and software for the ZX81 microcomputer and the Timex/Sinclair 1000. The newsletter also provides a forum for users to exchange original ideas and programs. To receive more information and a sample issue, send $2 to *Sinclair Micronews*, 1280 Paddington Way, San Jose, CA 95127.

VIC-20 Only

The Vic-Nic-News is produced by the Byte House for owners and users of the Commodore VIC-20 home computer. The newsletter features news, programs, and information about the VIC. For a free copy, send a self-addressed stamped envelope to the Byte House, POB 981, Salem, NH 03079.

Update on Electronics

The American Electronics Association (AEA) is a nonprofit trade organization that produces a monthly news journal, *Update*, which discusses electronics in relation to the environment and announces relevant seminars in its calendar. For further information, contact Leslie Conley, 2680 Hanover St., Palo Alto, CA 94304, or call (415) 857-9300.

Attention: Software Authors

The Software Author, a special-interest group that meets on the Compuserve Information Service, provides contacts for freelance programmers, publishers, and software authors. The Software Author includes an electronic bulletin board and databases of market reports. Regular online conferences with guests from the publishing industry allow members to ask questions. The Software Author is open to any Compuserve subscriber; membership is free. Access the Software Author with a "G PCS-117" command from any prompt or select option 13 from the group's menu on PCS-50.

Next: NECS

The New England Computer Society (NECS) produces a monthly newsletter and welcomes exchanges with other clubs. It meets on the first Wednesday of each month at 7 p.m. in Bedford, Massachusetts. Annual dues are $10. For further details, contact the New England Computer Society, POB 198, Bedford, MA 01730.

Pascal for DEC Owners

USUS (the UCSD Pascal-System User's Society) has formed a special-interest group (SIG) for users of the UCSD p-System on DEC (Digital Equipment Corporation) computers. The DEC SIG will serve as a clearinghouse for information relating to the implementation, optimization, and use of the p-System on DEC computers. Individual membership in USUS is $20 a year; membership in DEC SIG is free to USUS members. For further information, contact Eli Willner, Datronics Inc., 675 Third Ave., New York, NY 10017.

Microcomputing in British Columbia

The Island Microcomputer Society seeks beginners and experts to join a Canadian microcomputing club. In addition to the monthly newsletter, *The Datafile*, the club offers a library of computer magazines and books, a bulletin board, and an annual computer fair. For further information, call Gil Phillips at (604) 385-4063, or write to the Island Microcomputer Society, Station E, POB 1822, Victoria, British Columbia V8W 2Y3, Canada.

Fast Photo Service

The Photoletter sends newsletters and photos via computer. The twice-monthly market letter pairs buyers with photographers. Subscribers are charged $24 per hour of access time or a $15 monthly minimum. For more information, write to Rohn Engh, Pine Lake Farm, Osceola, WI 54020, or call (715) 248-3800.

NEC Group in San Francisco

Users of the NEC (Nippon Electric Company) PC-8001 series of computers have formed the NEC Computer Users group in the San Francisco area, which produces a newsletter containing technical articles on NEC PC-8000 components. Members meet monthly to exchange software and solutions to problems. Dues are $15 a year in the U.S. For more information, write to NEC Computer Users, POB 500, Benicia, CA 94510.

VIC Club in Chicago

An international clearinghouse in Chicago, Illinois, is devoted to the Commodore VIC-20, 64, and Max computers. The VIC International Computer Knowledge Information Exchange (VICKIE) membership fee is $20 a year and $17.50 for students. Sample newsletters are available for $1. For further information, write to John Rosengarten, VICKIE, 3822 North Bell Ave., Chicago, IL 60618.

Using the Osborne 1

The *Os/Tech* newsletter is designed to pass along tips that owners of the Osborne 1 have learned as well as to announce new products and software. It is produced six times a year. Subscriptions are $9 within the U.S. *Os/Tech* will be produced in Spanish if there is enough demand. For more information, contact *Os/Tech*, POB 517, Clearwater, FL 33517, or call (813) 446-7239.

Alternate with the Update

Computer Update is produced every other month by the Boston Computer Society (BCS). Subscription to the magazine is free with BCS membership. BCS contains 19 user/interest groups. Annual membership is $20, students are $12, and the international fee is $40. For further information, write to the Boston Computer Society Inc., Three Center Plaza, Boston, MA 02108, or call (617) 367-8080.

Clubs and Newsletters

Amateurs Meet In New Jersey

The Amateur Computer Group of New Jersey (ACG-NJ) produces a monthly newsletter that is available with membership in the group. The annual membership fee is $14 in the U.S. and Canada, and $27 overseas. For more information, write to the Amateur Computer Group of New Jersey Inc., POB 319, South Bound Brook, NJ 08880.

Puget Sound and Beyond

The Northwest Computer Society meets on the first and third Thursdays of each month at 7:30 p.m. at Seattle University. The annual membership fee is $12 and entitles you to receive the newsletter, *The Northwest Computer News.* For further information, write to the Northwest Computer Society, POB 4193, Seattle, WA 98104.

Electronics In Japan

What's Happening in Electronics, a newsletter produced in Japan by Fujitsu Ltd., provides news briefs on computers and communications-related fields in the Japanese electronics industry. For further information, contact the Editorial Office, IRM Inc., Rosei Building, 4-2, Higashi Azabu 1-chome, Minato-ku, Tokyo 106, Japan.

High-Tech News

Technology Trends Newsletter, produced monthly by DM Data, documents the impact of high-technologies on business and investments. The annual subscription is $295. Send inquiries to DM Data Inc., Suite 700, 6900 Camelback Rd., Scottsdale, AZ 85251, or call (602) 945-9620.

Audit & Account

The *Software Newsletter*, published quarterly by Coopers & Lybrand's Computer Audit Assistance Group (CAAG) and the National EDP (Electronic Data Processing) Auditors Foundation, focuses on the uses of software for auditing and accounting. For further information, call Kathleen Flynn at (212) 903-3112, or write to Coopers & Lybrand, CPA, 1251 Avenue of the Americas, New York, NY 10020.

Medically Speaking

Trinity Computing Systems offers its newsletter, *Currents*, about medical microcomputing systems, free to professionals in cardiology, radiology, internal medicine, and biomedical engineering. To subscribe to *Currents*, write to Trinity Computing Systems Inc., Suite 408, 1020 Holcombe Blvd., Houston, TX 77030, or call (800) 231-2445; in Texas, (713) 790-1894. ■

If you would like BYTE readers to know about your club or newsletter send the details accompanied by no more than one newsletter to Clubs and Newsletters, BYTE Publications, POB 372, Hancock, NH 03449. Overseas groups are encouraged to participate. Please allow at least three months for your announcement to appear.

Ask BYTE

Conducted by Steve Ciarcia

More on VIC Adapters

Dear Steve,

Your response to Mr. McIlwee's question about VIC-20 cassette adapters bears greater amplification. (See "VIC Cassette Adapter," October 1982 BYTE, page 453.)

For example, the VIC's F-6 pinout must be used to signal the computer that cassette operation is in progress. In addition, I found that the write signal tends to overdrive the recorder and must be attenuated and rolled off in frequency.

Figure 1 is a circuit that I devised which worked well with a Radio Shack Realistic recorder. The volume control *must* be set for 6 or above to assure a saturated (square wave) signal to the VIC-20.

When the computer requests "press record and play on tape," the operator reacts accordingly, and the play switch signal (S1) to the computer is closed. At the end of a save, the recorder is stopped and S1 opened. A similar action is taken during a load operation.

I don't know if this circuit will work with all recorders.

Charles A. King
McLean, VA

The VIC-20 is designed for digital input signals and not the normal analog output of the standard recorder. It can be made to work with a standard recorder, but it's very finicky and recorder-dependent.

A standard cassette recorder can be made to work properly with the VIC-20 if a simple interface circuit is used. William R. Hale's article "Add a Cassette Interface to Your VIC-20" (March 1982 BYTE, page 272) gives the necessary information. Note that the Play switch must be grounded during playback or the VIC will not know that the recorder is running. The volume level is rather touchy for proper operation and can be more easily adjusted if a pair of LEDs (light-emitting diodes) are connected back-to-back across the recorder audio output (i.e., earphone jack or equivalent). Also see Dr. Milan D. Chepko's article "How to Build an Inexpensive Cassette Level Indicator" (September 1981 BYTE, page 435). Adjust the volume control until one of the LEDs begins to flicker steadily and all will work fine. . . **.Steve**

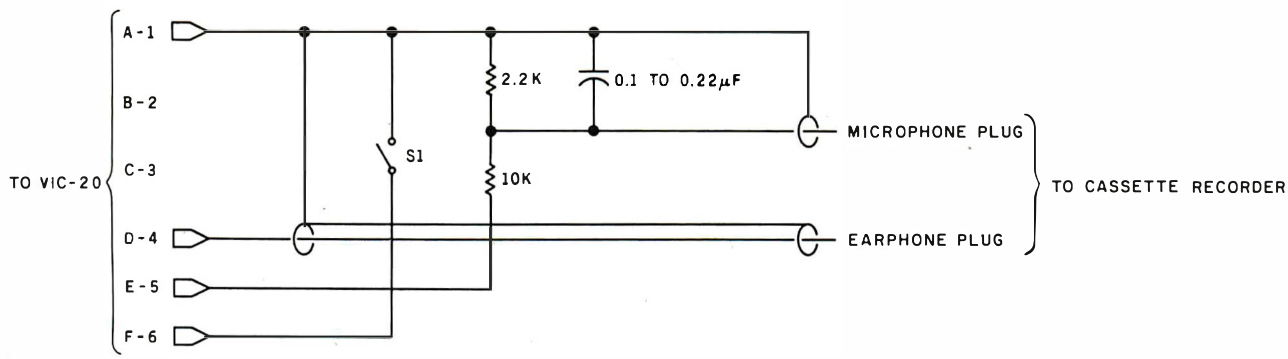


Figure 1: *Mr. King's circuit.*

Expanding the Z80 Computer

Dear Steve,

I am a graduate student in mathematics at the University of Tennessee. I have supplemented my education with personal and academic study in computer science and electrical engineering. I purchased your book, *Build Your Own Z80 Computer* (available for $17.95 from BYTE Books/McGraw-Hill, POB 400, Hightstown, NJ 08520). Using it and other sources, I have designed my own version. I have two partners who agree to finance its construction. If could add a disk controller for some 5¼- or 8-inch floppy-disk drives, it would be a much more useful product to us.

Do you have any information on the design of a floppy-disk controller, or can you point me toward some literature on the subject? I think there may be some BYTE articles on the subject; however, I wouldn't have the issues because my subscription began a little more than a year ago.

Also, in your book, you explain some of the important aspects of a serial interface. However, I would like to purchase a Heath/Zenith or RCA terminal and simply plug it in. Do you have any information on how to wire standard RS-232C plugs? Is there a source to explain RS-232C protocol?

Finally, in an Ask BYTE column, you mentioned that you can obtain disk access by configuring the computer to an S-100 bus. (See "Build Your Own," March 1982 BYTE, page 444.) That sounds great, but where can I find the specifics for doing that?

Thanks.

Wallace G. Hynds
Knoxville, TN

The June 1980 BYTE contained an article on serial interfaces, "I/O Expansion for the TRS-80, Part 2: Serial Ports" (page 42), that defines the pertinent RS-232C pinouts and gives theory and construction information on serial ports for a Z80-based system. Also, an excellent book that describes the interfacing of many computer buses to the S-100 is The S-100 & Other Micro Buses, *by Elmer C. Poe and James C. Goodwin (available for $9.95 from Howard W. Sams & Co. Inc., 4300 West 62nd St., POB 7092, Indianapolis, IN 46206).*

Here's a list of articles and books on floppy-disk controllers and interfacing the S-100 bus:

"Build the Disk-80: Memory Expansion and Floppy-

Disk Control," by Steve Ciarcia, March 1981 BYTE, page 36.

"Interface a Floppy-Disk Drive to an 8080A-Based Computer," by John Hoeppner, May 1980 BYTE, page 72.

Interfacing to S-100/IEEE 696 Microcomputers, *Sol Libes and Mark Garetz. Berkeley, CA: Osborne/McGraw-Hill, 1981, $15.*

"Build a Super Simple Floppy-Disk Interface," by James Nicholson and Roger Camp, Part 1: May 1981 BYTE, page 360; Part 2: June 1981 BYTE, page 302.
. . .Steve

Multichannel A/D Converters from Single Channels

Dear Steve,

Can I use transistors connected to the address lines of a computer to make a multichannel A/D (analog-to-digital) converter out of a single-channel A/D?

Joel Chaney
North Kingsville, OH

The answer to your question is yes. However, a simpler method uses a CMOS (complementary metal-oxide semiconductor) 4051-type bilateral switch. This device is the electronic equivalent of an 8-position rotary switch. When it is enabled, you simply send it a 3-bit address, which allows the voltage level on the corresponding input line to pass through to its single output line.

The 4051, along with its pin assignments, is shown in figure 2. To enable the device, you must ground the inhibit pin. To get it to work with negative-going analog signals, you must connect pin 7 to a −5-volt supply. This pin can be grounded with positive-only voltages.

If you are interested in learning more about CMOS devices, pick up a copy of the CMOS Cookbook, *by Don Lancaster. It costs $13.95 and is published by Howard W. Sams & Company.* . . .Steve

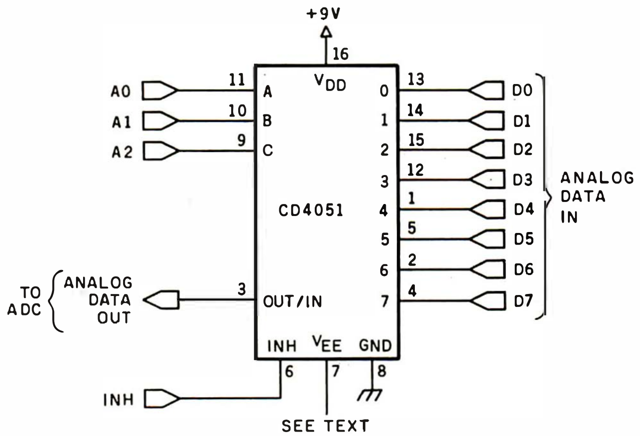


Figure 2: *The 4051-type bilateral switch and its pin assignments.*

Homebrewer's Nightmare

Dear Steve,

I have been attempting to interface National Semiconductor's MM58167A real-time clock integrated circuit to an Apple II I/O expansion bus. I have been using your article "Everyone Can Know the Real Time" as a reference (May 1982 BYTE, page 34). I have constructed a circuit (figure 3) on a Vector Plugboard. The MM58167A MOS (metal-oxide semiconductor) is sensitive to static, so it requires special handling procedures. When I installed the clock device, I found that only two of the seven registers could be accessed correctly. Some of the counters and registers were stuck on illegal values (only binary-coded decimal values are allowed), but the thing was apparently keeping time.

I asked the vendor, Jameco, of Belmont, California, to replace the device, which it did. The new chip's registers can be accessed properly, and it, too, seems to keep time. However, it doesn't respond to the GO command, so I can't set it. Finally, the seconds output is stuck on hexadecimal FF.

In both cases, I was careful to take all the precautions necessary with MOS devices, so I'm sure that I haven't caused the problem. How can I tell if it's the chip or the interface that's the culprit? Also, what is the "test mode" listed in table 1 of your article?

Edward Beighe
Bethlehem, PA

You have just experienced the dilemma of every hardware buff: "is it me or is it the chip?" The best way to test an LSI (large-scale integration) chip is to substitute another. The specification sheets describe the function of the device, and it's usually possible to set up a known condition on the input side and test for a correct output. If some of the outputs are correct and some are not, the chip can usually be suspected.

From the symptoms that you describe, it sounds like you have a defective chip. While you may have taken the proper handling precautions, it's possible that someone before you did not.

Other clock chips use the test mode for production testing. It speeds up certain functions so that the counting rate can be verified. It is not intended to be used in normal operation. . . **Steve**

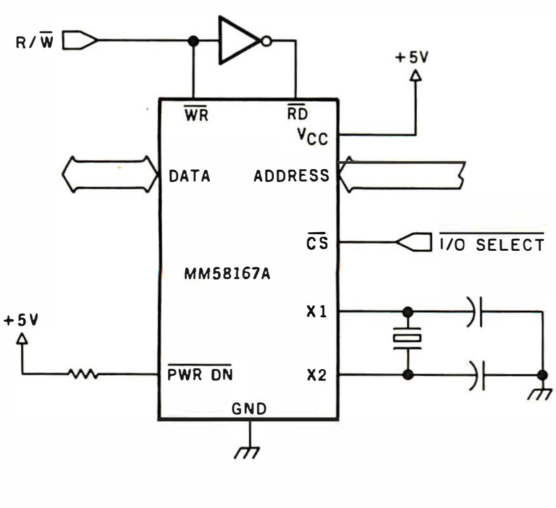


Figure 3: *Mr. Beighe's circuit.*

Where to Catch the S-100 Bus Standard

Dear Steve,

How can I get a copy of the IEEE S-100 bus standard?

Chip Wiggs
Miami, FL

Order copies of IEEE-696, as the S-100 bus standard is known, from the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854, (201) 981-0060. Write or call for the latest price and shipping details.

Information on this bus and many other buses can be found in the excellent book The S-100 & Other Micro Buses, *by Elmer C. Poe and James C. Goodwin. It's published by Howard W. Sams & Company (1981). Also see "The IEEE Standard for the S-100 Bus," by Mark Garetz (February 1983 BYTE, page 272). . .* **Steve**

In "Ask BYTE," Steve Ciarcia answers questions on any area of microcomputing. The most representative questions received each month will be answered and published. Do you have a nagging problem? Send your inquiry to:

Ask BYTE
c/o Steve Ciarcia
POB 582
Glastonbury CT 06033

If you are a subscriber to The Source, chat with Steve (TCE317) directly. Due to the high volume of inquiries, personal replies cannot be given. Be sure to include "Ask BYTE" in the address.

Event Queue

April 1983

April-May

Courses in C Language and Unix, various sites throughout the U.S. Three 5-day courses are offered by Plum Hall Inc. The "C Programming Workshop," a hands-on course, covers all aspects of the C language for individuals able to program in another language. The "Advanced C Topics Seminar" covers efficiency, portability, readability, debugging, packaging, and interfacing. The "Unix Workshop" is an introductory course that focuses on software development. Each course fee is $1000. For details, contact Joan Hall, Plum Hall Inc., 1 Spruce Ave., Cardiff, NJ 08232, (609) 927-3770.

April-May

Information Processing Seminars, various sites throughout the U.S. Datapro Research Corporation offers more than 35 seminars about information processing. Among the titles are "Optimizing Source Data Entry: Design Techniques," "User Friendly Information Delivery: Approaches to Online Systems Development," and "Distributed Systems Design: Microcomputers to Mainframes." These courses can be presented on an in-house basis. For a seminar catalog, contact Datapro Research Corp., 1805 Underwood Blvd., Delran, NJ 08075, (800) 257-9406; in New Jersey, (609) 764-0100.

April-June

Computer Literacy for Lawyers, various sites throughout the U.S. This seminar is intended to introduce attorneys to basic computer concepts and their application to the practice of law. Subjects covered include specific ways that computers can assist in operating legal practices, how computers can help lawyers service clients more effectively, and the uses, costs, and benefits of using computers in legal practice. The fee for each participant is $550, which includes reference materials. Group discounts are available. For further information, contact Kathryn Mann, Center for Legal Studies, 1926 Arch St., Philadelphia, PA 19103, (215) 732-6999.

April-June

Computer Showcase Expos, various sites throughout the U.S. This popular show will be held in several major cities between April and June. For a schedule, contact The Interface Group, 160 Speen St., POB 927, Framingham, MA 01701, (800) 225-4620; in Massachusetts, (617) 879-4502.

April-June

Courses from Q.E.D. Information Sciences, various sites throughout the U.S. Some of the courses listed are "Systems Analysis Workshop," "Project Management and Control," and "Data Analysis." Address inquiries to Priscilla Goudreault, Q.E.D. Information Sciences Inc., Q.E.D. Plaza, POB 181, Wellesley, MA 02181, (800) 343-4848; in Massachusetts, (617) 237-5656.

April-June

Data Processing Courses, the Hartford Graduate Center, Hartford, CT. Among the courses being offered are "ANS COBOL Programming Workshop 1" and "CICS/VS Command Level Coding Workshop." Hartford Graduate Center data-processing courses are available for on-site presentation. For details, contact Don Florek, The Hartford Graduate Center, 275 Windsor St., Hartford, CT 06120, (203) 549-3600, ext. 252, 253, or 254.

April-June

Fourth Generation Methodologies and **Seminars of Excellence,** various sites throughout the U.S. The five-day "Fourth Generation Methodologies" seminar explores information engineering, application creation methodologies, and management patterns. James Martin will be the seminar leader. The fee is $1495.

Some of the areas covered by the "Seminars of Excellence" are local data networks, relational databases, and distributed database systems. Fees range from $795 to $950. Details on these seminars are available from the Technology Transfer Institute, 741 10th St., Santa Monica, CA 90402, (213) 394-8305.

April-June

Intel Microcomputer Workshops, various sites throughout the U.S. Among the workshops to be held are "Introduction to Microprocessors" and "iAPX 86, 88, 186 Microprocessors." Intel Customer Training Courses are available for on-site presentation. For details, contact Intel Corp., Mail Stop SV3-1, 3065 Bowers Ave., Santa Clara, CA 95051.

April-June

Intensive Seminars of Interest to Data Processing Professionals, Boston metropolitan area. Among the two- to five-day seminars offered are "Project Management" and "Systems Design." Registration fees range from $495 to $975. For a seminar bulletin, contact Ms. Ginny Bazarian, Office of Continuing Education, Higgins House, Worcester Polytechnic Institute, Worcester, MA 01609, (617) 793-5517.

April-June

Management Development Programs, Providence, RI, Boston, MA, and Hartford, CT. The Center for Management Development offers seminars in a variety of areas, including communications, industrial relations, and electronic data processing. Many of the Center's programs can be conducted on location for your organization. For complete information, contact The Center for Management Development, Bryant College, Smithfield, RI 02917, (401) 231-1200, ext. 314.

April-June

Professional Development Seminars, various sites throughout the U.S. Data communications, database management, software and systems, and computer-aided design/manufacturing are some of the areas investigated in seminars offered by the Institute for Advanced Technology. For a detailed catalog, contact the Registrar, Institute for Advanced Technology, Control Data Corp., 6003 Executive Blvd., Rockville, MD 20852, (800) 638-6590; in Maryland, (301) 468-8576.

April-June

Seminars in Simulation, Management, Statistics, and Computer Science, various sites throughout the U.S. "Simulation Modeling for Decision Making," "Database Design," and "Satellite Communications Technology" are some of the topics to be presented. For information, contact the Institute for Professional Education, POB 756, Arlington, VA 22216, (703) 527-8700.

April-July

Courses from Integrated Computer Systems, various sites throughout the U.S. Course titles include "Com-

puter-Aided Design and Manufacturing," "Computer Graphics," "Hands-On Pascal Workshop," "Defining Software Requirements, Specifications, and Tests," and "Computerized Robots." Fees range from $695 to $845. For information, contact Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., POB 5339, Santa Monica, CA 90405, or call (213) 450-2060.

April-July

Productivity '83, various sites throughout the U.S. and Canada. This is Hewlett-Packard's hands-on showcase of more than 32 computer products and 17 seminars. It's designed to provide data-processing professionals and novices answers to problems confronting the industry. For details, call (800) 453-9500.

April-July

Technical Courses from Zilog, Campbell, CA. A wide variety of such courses as "The Computer: A Survey Course" and "C Programming" are offered. Fees range from $175 to $875. For a complete schedule, contact Zilog Inc., Training and Education Department, 1315 Dell Ave., Campbell, CA 95008, (408) 370-8092.

April-October

Courses from the AMA, various sites throughout the U.S. The American Management Associations (AMA) offers an on-going series of seminars in such areas as human resources, information systems, and manufacturing and technology management. In-house development and training seminars can be arranged. For information on AMA membership or seminar particulars, contact the American Management Associations, 135 West 50th St., New York, NY 10020, (212) 586-8100.

April-December

IEEE Conferences and Meetings, various sites around the world. The Institute for Electrical and Electronics Engineers (IEEE) sponsors conferences, meetings, and workshops covering high-technology issues. For details, contact the IEEE Computer Society, Suite 300, 1109 Spring St., Silver Spring, MD 20910, (301) 589-8142.

April 10-13

APL83, Sheraton Washington Hotel, Washington, DC. This conference and exhibition includes hands-on displays and presentations of technical papers. For details, contact D & S Whyte Associates, Conference and Exhibits Manager, Suite 200, 117 King St., Alexandria, VA 22314, (703) 548-2802.

April 10-15

Data Processing Training Managers' Workshop, Dallas, TX. This workshop is intended for individuals with less than 18 months of experience in coordinating data-processing programs. Participants will learn how to establish in-house education programs that meet management's objectives and ensure a high return on their organization's investment in training. The fee is $1000. Contact Deltak Inc., 1751 West Diehl Rd., Naperville, IL 60566, (312) 369-3000.

April 11-13

Gate Arrays, Boston, MA. For full details, contact the Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Treader Way, Columbia, MD 21044, (301) 596-0111; on the West Coast, call (213) 824-9545.

April 11-13

IBM-MVS Training Seminars, Chicago, IL. Two seminars are offered: "MVS Internals Overview for Data Processing and Operations Management" and "MVS Internals for Systems Programmers." These courses run for 1½ and 2½ days, respectively. For complete information, contact ACTS Corp., 11910 Gate Way, Austin, TX 78759, (512) 258-7869.

April 11-13

Personal Computers for Scientists and Engineers, Center for Professional Advancement, East Brunswick, NJ. Participants will learn how to use disk-operating systems, electronic spreadsheets, filing systems, and a word processor. Other programs will be demonstrated. Each attendee will work with an Apple II Plus computer. Two session formats are available. The fee is approximately $750. Contact the Center for Professional Advancement, General Information, POB H, East Brunswick, NJ 08816, (201) 249-1400.

April 11-15

Intergraphics '83, Takanawa Prince Convention Center, Tokyo, Japan. This conference and exhibition will cover a wide range of computer-graphics topics, including business and management graphics, virtual machine languages, and chemical and biochemical appli tions of computer graphics. Complementing formal programs will be speakers, discussions, and tutorials. For complete details, contact the World Computer Graphics Association, Suite 250, 2033 M St. NW, Washington, DC 20036, (202) 775-9556.

April 12-13

Selecting a Microcomputer for Scientific and Engineering Applications, Golden, CO. This short course reviews hardware and software technology for potential buyers of microcomputers in relation to specific scientific and engineering applications. The fee is $195. Contact the Space Office, Colorado School of Mines, Golden, CO 80401, (303) 273-3321.

April 12-13

The Seventh Annual University of Dayton Computer Fair, University of Dayton Arena, OH. This fair is sponsored by the Office for Computing Activities of the University of Dayton. It features terminals, computers, and word processors. Further information can be obtained from Don Schumacher, University of Dayton, 300 College Park Ave., Dayton, OH 45469, (513) 229-3511.

April 12-14

The Ninth Annual Federal Data Processing Expo, Convention Center, Washington, DC. More than 150 companies will display and demonstrate computer and communications products and services. The conference portion of this event will offer 46 sessions on a variety of topics of interest to federal data-processing professionals. For further information, contact The Interface Group, 160 Speen St., POB 927, Framingham, MA 01701, (800) 225-4620; in Massachusetts, (617) 879-4502.

April 12-14

The Sixth Annual Southwest Computer Conference-SWCC, Myriad Convention Center, Oklahoma City, OK. The theme of this conference is "Managing Information Technology in the '80s." Seminars and an exhibition area are planned. For details, contact SWCC, POB 950, Norman, OK 73070, (405) 329-3660.

April 13-15

Local Area Networks: Design and Management, Hyatt Hotel, Los Angeles, CA. This seminar is intended to provide an understanding of the theory and practical implementations of local-area net-

works. Areas of interest include techniques of evaluating proposals for systems, methods in analyzing conflicting information, and probable future developments. The fee is $595; group discounts are available. This seminar can be presented within your organization. Contact the Center for Advanced Professional Education Inc., 11928 North Earlham, Orange, CA 92669, (714) 633-9280.

April 13-20

Hanover Fair '83—Cebit '83, Hanover, West Germany. The Hanover Fair is one of the world's largest industrial trade fairs. Attention will be paid to office equipment and data-processing technology. More than 1200 exhibitors from 30 countries will display their products to a crowd of more than 200,000. Full information is available from the Hanover Fairs Information Center, Salem Industrial Park, POB 338, Whitehouse, NJ 08888, (800) 526-5978; in New Jersey, (201) 534-9044.

April 14-17

The Second Annual New York Computer Show and Software Exposition, Nassau Coliseum, Uniondale, NY. This show features printers, software, hard disks, modems, memory cards, cartridges, publications, support services, and other peripherals and accessories. Admission is $5 for adults and $3 for children. Contact Northeast Expositions, 822 Boylston St., Chestnut Hill, MA 02167, (617) 739-2000.

April 15-16

The Thirteenth Annual Virginia Computer Users Conference—VCUC, Marriott Hotel, Blacksburg, VA. This conference is organized and run by the Virginia Tech Student Chapter of the Association for Computing Machinery in cooperation with the Virginia Polytechnic Computer Science Department. Topics of interest include Ada, human factors, and computer graphics. For more information, contact Luanne Melown or Paula Brimer, Virginia Polytechnic Institute and State University, 562 McBryde Hall, Blacksburg, VA 24061, (703) 961-6931.

April 15-17

Applefest, Convention Center, Anaheim, CA. This event features conferences, workshops, and panel discussions designed to show users how to effectively use their Apples. Approximately 350 exhibitors will participate. For more information, contact Northeast Expositions, 826 Boylston St., Chestnut Hill, MA 02167, (800) 841-7000; in Massachusetts, (617) 739-2000.

April 15-17

The Use of Computers in Psycholog , Hilton, Wilmington, NC. With a focus on microcomputers, the five planned symposia will cover such issues as statistical and therapeutic applications and the use and misuse of microcomputers in psychological assessment. For complete details, write to Steven R. Edelman, Association of Eastern North Carolina Psychologists, 105 Lou Dr., Goldsboro, NC 27530.

April 16

The First Annual Oak Ridge Hamfest/Computerfest, Civic Center, Oak Ridge, TN. Manufacturer displays, trading opportunities, technical talks, demonstrations, and hourly door prizes will highlight this show. For further information, write to the Oak Ridge Amateur Radio Club Inc., POB 291, Oak Ridge, TN 37830.

Circle 476 on inquiry card.

April 16-17
The Eighth Annual Trenton Computer Festival, Trenton State College, NJ. This festival includes short courses, user group meetings, demonstrations, commercial exhibits, and a flea market. Admission for the two days is $5. Contact Dr. Allen Katz, Trenton State College, Hillwood Lakes CN 550, Trenton, NJ 08625, (609) 771-2487.

April 18-20
Personal Computers for Scientists and Engineers, East Brunswick, NJ. For details, see April 11-13.

April 18-21
The Thirteenth International Symposium on Industrial Robots and The Robots 7 Conference and Exposition, Conrad Hilton Hotel and McCormick Place, Chicago, IL. The theme for this event, "Robotics: The Emerging Challenge," will be investigated through more than a dozen conference sessions, four special forums, and three basic sessions. More than 150 companies will exhibit industrial robots and components. This event is cosponsored by Robotics International of the Society of Manufacturing Engineers (RI/SME) and the Robot Institute of America (RIA). Details are available from Ms. Pat Van Doren, SME Technical Activities, One SME Dr., POB 930, Dearborn, MI 48128, (313) 271-1500, ext. 369.

April 18-22
Auditing in the Contemporary Computer Environment, Las Vegas, NV. This course is designed for internal auditors and financial and data-processing professionals. Participants will learn a comprehensive audit approach for computer-based systems, including how to evaluate controls and how to design a program of tests using questionnaires, checklists, software tools, and flowcharts. Contact Marge Umlor, EDP Auditors Foundation, 373 South Schmale Rd., Carol Stream, IL 60187, (312) 682-1200.

April 18-22
Auditing Integrity Controls in the Contemporary Computer Environment, Las Vegas, NV. This program is designed to provide an overview of the computer environment, its controls, and its interrelationships. It combines theoretical and practical approaches for electronic data-processing auditing, with an emphasis on integrity controls and related operational concerns. Further details are available from Marge Umlor, EDP Auditors Foundation, 373 South Schmale Rd., Carol Stream, IL 60187, (312) 682-1200.

April 18-22
Digital Communication and Satellite Systems, University of California, Los Angeles. For details on this short course, contact the UCLA Extension Short Course Program, POB 24901, Los Angeles, CA 90024, (213) 825-1295 or (213) 825-3344.

April 19-20
Workspace 83, Civic Auditorium, San Francisco, CA. This show will feature the latest in electronic office furnishings, systems, and services for corporate, institutional, and commercial offices. Exhibits will include open-plan systems, lighting, fabrics, accessories, and telephone systems. Seminars and workshops relating to automated office space will be held. For details, contact The Charles Co., Suite 500, 44 Montgomery St., San Francisco, CA 94104, (415) 931-8255.

April 19-21
Electro/83—High-Technology

Electronics Exhibition and Convention, Coliseum and Sheraton Centre, New York, NY. This show runs concurrently with the Mini/Micro-Northeast exposition. For information, contact Electronic Conventions Inc., 999 North Sepulveda Blvd., El Segundo, CA 90245, (800) 421-6816; in California, (800) 262-4208 or (213) 772-2965.

April 19-21
Infocom 83, Town and Country Hotel, San Diego, CA. The theme for this second annual joint conference of the IEEE Computer and Communications Societies is "Computers and Communications Integration: Reality and Illusion." Topics of interest include computer network architectures, computer communications standards, and integrated services digital networks. A series of tutorials will be held the day before this conference begins. For further information, contact the IEEE Computer Society, POB 639, Silver Spring, MD 20901, (301) 589-3386.

April 19-22
Applied Time Series Analysis, Columbia Inn, Columbia, MD. For full details, contact the Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Treader Way, Columbia, MD 21044, (301) 596-0111; on the West Coast, call (213) 824-9545.

April 20-22
Local Area Networks: Design and Management, Hilton Inn, Natick, MA. For details, see April 13-15.

April 20-22
Symposium on Computer-Aided Geometry Modeling, Hampton, VA. For information, contact John Shoosmith, Mail Stop 125, NASA Langley Research Center, Hampton, VA 23665, (804) 827-3466.

April 21-22
Broadband Local Networks, Washington, DC. This program is the first of four parts in the Architecture Technology Corporation's 1983 Forum Series. The series will bring together manufacturers and users of local network schemes to exchange views and information in an informal setting. The format includes presentations, panel discussions, and a technological summary. The cost is $395 per person. For additional information, contact the Architecture Technology Corp., POB 24344, Minneapolis, MN 55424, (612) 935-2035.

April 21-22
Computers in Construction, New York, NY. This seminar is designed to assist construction contractors and construction management firms in acquiring computer systems. The registration fee is $395. For further information, contact CIP Information Services Inc., 1105-F Spring St., Silver Spring, MD 20910, (301) 589-7933.

April 21-22
Individualized Language Teaching Through Microcomputer-Assisted Instruction, Tampa, FL. This seminar will provide the theoretical background and hands-on experience necessary to enable participants to make practical use of microcomputer-assisted language instruction. For a brochure, contact Ms. Anita Mires, American Language Academy, Suite 200, 11426 Rockville Pike, Rockville, MD 20852, (301) 984-3400.

April 21-24
Virginia/Carolinas Computer Show and Office Equipment Exposition, Pavilion Exhibition Center, Virginia Beach, VA. For details, contact Dee Harris, Computer Expositions Inc., POB 3315, Annapolis, MD 21403, (800) 368-2066; in Maryland, (301) 263-8044.

April 22
Microcomputers in Physics Instruction, Wilkes College, Wilkes-Barre, PA. This session is sponsored by the Central Pennsylvania Section of the American Association of Physics Teachers. For information, contact F. J. Donahoe, Wilkes College, Box 111, Wilkes-Barre, PA 18766.

April 22-23
The Third Annual Role of the Computer in Education Conference, New Trier High School-West, Northfield, IL. This show is sponsored by Micro-Ideas. The keynote speaker will be Arthur Luehrmann. Further information is available from Richard Nelson, Micro-Ideas, 1335 North Waukegan Rd., Glenview, IL 60026, (312) 998-5065.

April 24-29
Data Processing Training Managers' Workshop, San Francisco, CA. For details, see April 10-15.

April 24-29
The HP 3000 International Users Group Conference, Montreal, Quebec, Canada. The theme for this conference is "Systems Designed with Users in Mind." Technical papers, vendor exhibits, and a lecture by Isaac Asimov will highlight this conference. Full details are available from Ms. Renaye Lee, Conference Manager, HP 3000 IUG, Suite 205, 289 South San Antonio Rd., Los Altos, CA 94022, (415) 941-9960.

April 25-27
The 1983 Symposium on Security and Privacy, Claremont Hotel, Oakland/Berkeley, CA. Papers and panel sessions will explore such topics as security testing and evaluation, application security, and cryptographic protocol. For further details, contact the IEEE Computer Society, POB 639, Silver Spring, MD 20901, (301) 589-3386.

April 25-27
Workshop on Software Engineering Technology Transfer, Konover Hotel, Miami Beach, FL. This workshop will probe some of the problems affecting the use of software engineering tools, techniques, and methodologies, in such areas as marketing, engineering, sales, and customer service. For further information, contact the IEEE Computer Society, POB 639, Silver Spring, MD 20901, (301) 589-3386.

April 25-29
Auditing in the Contemporary Computer Environment, Oklahoma City, OK. For details, see April 18-22.

April 26-28
Exploitation '83—The HP1000 International User Group Conference, Heathrow Penta Hotel, Heathrow, London, England. Papers and commercial exhibits about getting the most from your system will be featured. For full details, contact the HP1000 Conference Centre, Conference Services Ltd., 3 Bute St., London SW7 3EY, England; tel: 01-584 4226; Telex: 916054.

April 26-28
Info/Manufacturing and **Hi-Tech** 83, McCormick Place, Chicago, IL. These joint conferences and expositions cover information systems and advanced manufacturing technologies. The intent is to coordinate efforts and solve common problems confronting manufacturing technology

and information system companies. More than 50 conference sessions are planned. Topics on the agenda include database management and systems integration, office automation, and artificial intelligence expert systems. Conference programs are available from Clapp & Poliak, 708 Third Ave., New York, NY 10017, (212) 370-1100.

April 26-29
Comdex/Spring, Georgia World Congress Center and the Apparel Mart, Atlanta, GA. More than 600 companies will display and demonstrate computers, word-processing systems, peripherals, software, media, supplies, services, and other computer-related items. This third annual conference will offer 56 sessions on business, marketing, and financial subjects of interest to ISOs (independent sales organizations). Contact The Interface Group, 160 Speen St., POB 927, Framingham, MA 01701, (800) 225-4620; in Massachusetts, (617) 879-4502.

April 28-30
Ed Com/Spring '83, Washington, DC. In more than 300 session hours educators will address, evaluate, and analyze the development of computers in education. Demonstrations, seminars, hands-on experience, and panel sessions will display hardware, software, and publications. For more information, contact Carol Houts, Judco Computer Expos Inc., Suite 201, 2629 North Scottsdale Rd., Scottsdale, AZ 85257, (800) 528-2355; in Arizona, (602) 990-1715.

April 28-30
Microcomputers in Education, Cambridge, MA. This hands-on workshop is designed for teachers and administrators at all levels. Topics include microcomputers in science and mathematics instruction, Logo, Pascal, machine language, and microcomputers and the education of students with special needs. Contact Ms. Sharon Woodruff, Technical Education Research Centers, 8 Eliot St., Cambridge, MA 02138, (617) 547-3890.

April 28-30
Teaching Math with Microcomputers, Chicago, IL. This seminar is designed to inform elementary, intermediate, and secondary school educators how to effectively use the microcomputer as a tool in mathematics teaching. Participants will be divided into workshop groups by academic levels. Guest speakers will explore such areas as computer literacy and awareness, software, programming, and hardware selection. For members of the National Council of Teachers of Mathematics (NCTM), the registration fee is $145. For nonmembers, the fee is $245. Address inquiries to NCTM '83 Seminar Series, 1906 Association Dr., Reston, VA 22091, (703) 620-9840.

April 28-May 1
The Third Annual Southwest Computer Show and Software Exposition, Market Hall, Dallas, TX. This show features printers, modems, video displays, plug-in boards, cartridges, software, and support services. Admission is $5 for adults and $3 for children. Full details are available from Northeast Expositions, 822 Boylston St., Chestnut Hill, MA 02167, (617) 739-2000.

May 1983

May 1-4
The Thirtieth International Technical Communication Conference, Sheraton-St. Louis Hotel, St. Louis, MO. This conference is sponsored by the Society for Technical Communication (STC). It will focus on such issues as industrial instruction, consumer education, and safety. For full details, contact the STC, 815 15th St. NW, Washington, DC 20005, (202) 737-0035.

May 2-5
Test and Measurement World Expo, Convention Center, San Jose, CA. More than 50 workshops will explore instruments and techniques critical to performing timely and cost-effective failure analyses of microelectronic circuits and components. Topics to be addressed include X-ray microradiography and surface analysis techniques. Full particulars are available from Meg Bowen, Test and Measurement World Expo, 215 Brighton Ave., Boston, MA 02134, (617) 254-1445.

May 2-6
Auditing Integrity Controls in the Contemporary Computer Environment, Oklahoma City, OK. For details, see April 18-22.

May 2-6
Systematic Software Maintenance in COBOL, Chicago, IL. This seminar incorporates a mixture of structured methodologies, management strategies, solutions for effective testing, criteria development, analysis, and feedback accountability. Contact Eduteach Inc., Suite 907, 162 North State St., Chicago, Il 60601, (312) 641-1370.

May 4-6
The Sixth Annual Rocky **Mountain Data Processing Expo and Conference**, Currigan Hall, Denver, CO. Some of the products to be exhibited include computers, word processors, graphics systems, peripherals, and support services. Complete particulars are available from Industrial Presentations West, Suite 304, 3090 South Jamaica Court, Aurora, CO 80014, (303) 696-6100.

May 5-7
Teaching Math with Microcomputers, New York, NY. For details, see April 28-30.

May 9-13
The Twenty-fourth ADCIS International Conference, Marriott City Center, Denver, CO. The annual conference of the Association for the Development of Computer-based Instructional Systems (ADCIS) features workshops, novice and technical programs, presentations, poster sessions, and exhibits. For more information, contact the ADCIS International Headquarters, Miller Hall 409, Western Washington University, Bellingham, WA 98225, (206) 676-2860.

May 10-11
Selecting a Microcomputer for Scientific and Engineering Applications, Golden, CO. For details, see April 12-13.

May 10-12
Mini/Micro-Northwest, Portland, OR. Running concurrently with Northcon/83, this show addresses such topics as aerospace electronics, laser applications, and signal and image processing. Contact Electronic Conventions Inc., Suite 410, 999 North Sepulveda Blvd., El Segundo, CA 90245, (800) 421-6816; in California, (800) 262-4208 or (213) 772-2965.

May 11-15
Computa '83: The Third International Exhibition on Computer and Information Processing Technology, World Trade Centre, Singa-

pore. Complete information is available from Kallman Associates, 5 Maple Court, Ridgewood, NJ 07450, (201) 652-7070.

May 12-13
The Fourth Annual Computer Law Institute, University of Southern California Law Center, Los Angeles. This year's Institute will present a program on structuring agreements for the distribution of computer products domestically as well as internationally. Other topics include proprietary rights, antitrust issues, and major systems procurement. An optional session on the basics of computer products and technology will be offered. Contact Ami Silverman, USC Law Center, University Park, Los Angeles, CA 90007, (213) 743-2582.

May 13-15
Applefest, Bayside Exposition Center, Boston, MA. This is the third annual Boston Applefest. More than 400 displays and booths of Apple-compatible products will be featured. Complementing the exposition will be seminars, conferences, workshops, and panel discussions. Call or write Northeast Expositions, 826 Boylston St., Chestnut Hill, MA 02167, (800) 841-7000; in Massachusetts, (617) 739-2000.

May 14-15
Toronto PET User's Group Conference, George Brown College, Casa Loma campus, Toronto, Ontario, Canada. Speakers, workshops, a trader's corner for used equipment, and exhibits of hardware, software, and accessories highlight this event. Contact Chris Bennett, TPUG Corresponding Secretary, 381 Lawrence Ave. W, Toronto, Ontario M5M 1B9, Canada, (416) 782-9252.

May 16-18
Computer Graphics for Engineering/Drafting Practice, University of Texas, Austin. This course will stress developing the ability to prescribe and implement computer graphics equipment for specific engineering applications. A two-day hands-on workshop follows the course. Contact the College of Engineering, University of Texas, Austin, TX 78712, (512) 471-3396.

May 16-18
Mini-Conferences and Professional Growth Seminars, Loews Anatole, Dallas, TX. A special feature of this event will be the introduction of the data-entry certification program. Among the topics to be addressed are motivation, training, and interviewing. Contact Marilyn S. Bodek, Data Entry Management Association, POB 3231, Stamford, CT 06905, (203) 322-1166.

May 16-19
National Computer Conference, Anaheim and Disneyland Hotel Convention Centers, Anaheim, CA. This show features exhibits of computer products and services, technical sessions, seminars, and formal addresses. For complete information, contact the American Federation of Information Processing Societies Inc., 1815 North Lynn St., Arlington, VA 22209, (703) 558-3624.

May 16-19
Patent Your Software for Profit, Anaheim, CA. This seminar, which runs concurrently with the National Computer Conference, will explore software patent examples and offer advice on patenting and licensing software. Patent reference materials will be provided. Full details are available from Delbert L. Keenon, Automation Inc., 3410 Mona Lee, Houston, TX 77080, (713) 462-4151.

May 16-20
Auditing in the Contemporary Computer Environment, New York, NY. For details, see April 18-22.

May 16-20
Auditing Integrity Controls in the Contemporary Computer Environment, Washington, DC. For details, see April 18-22.

May 17-20
Technology/Invention New Product Expo, Expo Mart, Monroeville, PA. This show will feature everything from diesel fuel-injection systems to spring-loaded fly swatters. Further details can be obtained from Gary F. Brown, Technology/Inpex, Suite 400, 701 Smithfield St., Pittsburgh, PA 15222, (412) 288-1344.

May 18-20
The Fifth National Conference of the Cognitive Science Society, University of Rochester, Rochester, NY. This conference will consist of lectures, panels, commentaries, and papers. Contact the Cognitive Science Conference, Dewey Hall, University of Rochester, Rochester, NY 14627, (716) 275-5402.

May 18-20
Man Machine Interface, Palo Alto, CA. For full details, contact the Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Treader Way, Columbia, MD 21044, (301) 596-0111; on the West Coast, call (213) 824-9545.

May 18-20
Mipro-83: The Sixth Microprocessors/Microcomputers Course/Conference, Congress Center, Hotel Adriatic, Opatija, Yugoslavia. The theme for this conference is "Advanced Microcomputer Application Techniques and New Trends." It is geared toward hardware and software specialists and managers involved with the development, production, and management of microcomputer-based systems. For details, contact Mr. P. Dragojlović, Mipro Secretariat, Trg P. Togliatti 4, 51000 Rijeka, Yugoslavia.

May 19-20
Computers in Construction, Denver, CO. For details, see April 21-22.

May 19-22
Maryland Computer Show and Office Equipment Exposition, Convention Center, Baltimore, MD. Address inquiries to Dee Harris, Computer Expositions Inc., POB 3315, Annapolis, MD 21403, (800) 368-2066; in Maryland, (301) 263-8044.

May 20-22
Computers and Personal Values: Sharing from Experience, Sign of the Dove, Temple, NH. This workshop offers individuals in the computer community the opportunity to examine personal, ethical, or moral questions associated with their work and with the impact of computers on society. The format includes small and large discussion groups and invited speakers. The cost is $150. For more information, contact Arthur Fink, Prince St., Box 614, Wilton, NH 03086, (603) 654-6518.

May 21
The Sixth Annual Spring Microcomputer Show & Tell Conference, University of Oklahoma, Norman. This conference is designed to let computer enthusiasts share

ideas and information. Six show and tell periods allow speakers to demonstrate their devices and field questions from the audience. Also featured is an on-the-spot programming contest. For additional information, contact Dr. Richard V. Andee, Mathematics Department, University of Oklahoma, Norman, OK 73019, (405) 325-3410.

May 22-25
The Eighteenth Annual Meeting and Exhibit Program of the AAMI, Loews Anatole, Dallas, TX. Topics on the docket include anesthesia instrumentation and technology, computer applications, personnel management, and technology transfer. Roundtable discussions, tutorials, and an exhibit program will be featured. For details, contact the Association for the Advancement of Medical Instrumentation, Suite 602, 1901 North Fort Meyer Dr., Arlington, VA 22209, (703) 525-4890.

May 23-27
Auditing Integrity Controls in the Contemporary Computer Environment, New York, NY. For details, see April 18-22.

May 24-26
Microprocessor Background for Management Personnel, Palo Alto, CA. The fee for this course is $565, which includes text and program materials. Contact Continuing Education in Engineering, Department 532N, University of California Extension, 2223 Fulton St., Berkeley, CA 94720, (415) 642-4151.

May 31-June 2
The Second Canadian Computer-Aided Design/Computer-Aided Manufacturing and Robotics Exposition and Conference, International Centre of Commerce, Toronto, Ontario, Canada. Leading international companies will demonstrate industrial robots, automatic assembly equipment, optical scanners, and numerically controlled machine tools. Technical papers will focus on such topics as robot-vision systems and design analysis. For information, contact Hugh F. Macgregor & Associates, 662 Queen St. W, Toronto, Ontario M6J 1E5, Canada, (416) 363-2201.

May 31-June 4
The Twelfth Annual MUMPS Users' Group Meeting, Hilton Hotel, San Francisco, CA. Introductory and advanced tutorials, workshops, roundtable discussions, site visits, and hardware, software, and systems demonstrations and exhibits will be offered. Registration information is available from Charles White, Professional Associates, 2012 Big Bend Blvd., St. Louis, MO 63117.

June 1983

June
Continuing Engineering Education Courses, George Washington University, Washington, DC. Among the courses available are "Database and File Management for Microcomputers," "Computer Communications Systems and Networks," and "A Phased Approach to Software Conversion." For information, contact Douglas Green, Continuing Engineering Education, George Washington University, Washington, DC 20052, (800) 424-9773; in the District of Columbia, (202) 676-8512.

June 1-4
The First Annual Sunbelt Educational Computing Conference, Texas Tech Univer-

Event Queue

sity, Lubbock. The theme for this conference is "Practical Applications and Current Issues in Educational Computing." For complete details, write to Dr. Cleborne E. Maddux, College of Education, Texas Tech University, POB 4560, Lubbock, TX 79409.

June 5-8

Consumer Electronics Show (CES), McCormick Place, Chicago, IL. This show is sponsored by the Electronic Industries Association (EIA). For information on this popular event, contact the Consumer Electronics Shows Office, Suite 1607, Two Illinois Center, 233 North Michigan Ave., Chicago, IL 60601, (312) 861-1040.

June 5-8

Mini-Conferences and Professional Growth Seminars, Registry Resort Hotel, Scottsdale, AZ. For details, see May 16-18.

June 5-9

The Twelfth Annual International Software AG Users' Conference, Fairmont and Royal Sonesta Hotels, New Orleans, LA. This conference will feature speakers, presentations, workshops, and tutorials. Contact Paula J. Brooks, Software AG of North America Inc., 11800 Sunrise Valley Dr., Reston, VA 22091, (703) 860-5050.

June 6-8

The Fifth Annual National Educational Computing Conference–NECC 83, Towson State University, Baltimore, MD. This conference provides a broad forum for discussion among individuals at all levels and from all institutions sharing an interest in educational computing. Papers will address such issues as computer education for teachers, computer education and job opportunities for the handicapped, and accreditation and certification programs. Tutorials will be held, and demonstration and exhibit areas will emphasize computer uses in instruction. For registration forms, contact Doris K. Lidtke, NECC 83, Department of Mathematics and Computer Science, Towson State University, Baltimore, MD 21204.

June 6-8

The Sixth International Conference on Computers and the Humanities–ICCH/83, North Carolina State University, Raleigh, NC. This conference serves as a forum for the exchange of ideas on the use of computers in all areas of the humanities. Features include formal sessions and related activities, discussion groups, tutorials, workshops, and exhibits. For details, write to Dr. Sarah K. Burton, Department of English, POB 5308, North Carolina State University, Raleigh, NC 27650.

June 7-8

International Conference on the Use of Micros in Fluid Engineering, Tara Hotel, London, England. All aspects of the use of microcomputers and microprocessors in fluid engineering will be covered. Subjects of interest include developing software for fluid-engineering design, rapid response controllers, and data-acquisition and analysis on-site. Full details are available from the Organizing Secretary, Micros in Fluid Engineering, BHRA Fluid Engineering, Cranfield, Bedford MK43 0AJ, England; tel: (0234) 750422; Telex: 825059.

June 7-9

International Computer Show, Velodrome, Olympic site, Montreal, Quebec, Canada. This trade show is designed for businesses wish-

ing to identify or compare computers and equipment for automating the office or for industrial activities. The public is invited. Contact Industrial Trade Shows of Canada, 20 Butterick Rd., Toronto, Ontario, M8W 3Z8, Canada, (416) 252-7791.

June 7-9
Maptek Europe 1983: Annual Strategy Conference, Hotel Excelsior, Venice, Italy. This meeting will provide detailed market forecasts and strategic recommendations for computer systems, network information services, communications and teleconferencing, office systems, and departmental integration. Contact Robert B. King, Quantum Science Corp., 1114 Avenue of the Americas, New York, NY 10036, (212) 997-0070. In Europe, contact Constantine E. Adraktas, Quantum Science Corp., 16 Charles II St., London SW1Y 4QU, England; tel: (01) 839-5347.

June 7-11
The Third Rochester FORTH Applications Conference, Laboratory for Laser Energetics, University of Rochester, NY. This conference is sponsored by the Institute for Applied FORTH Research Inc. Guest speakers will cover robotics and FORTH in a special one-day session. For complete details, contact Diane Ranocchia, Institute for Applied FORTH Research Inc., 70 Elmwood Ave., Rochester, NY 14611, (716) 235-0168.

June 8-10
The International Conference on Consumer Electronics-ICCE, Ramada the O'Hare Inn, Des Plaines, IL. Technical papers and panel discussions will address such issues as personal computing, low-cost printers, and computer-aided design/manufacturing techniques. Products will be displayed. This conference is sponsored by the Consumer Electronics Society of the Institute of Electrical and Electronics Engineers. Contact ICCE, POB 149, Bloomingdale, IL 60108.

June 9-11
Microcomputers in Education, Watertown, CT. For details, see April 28-30.

June 13-15
Analysis and Design-Oriented Techniques, Los Angeles, CA. For details on this power electronics course, contact Teslaco, Suite 6, 490 South Rosemead Blvd., Pasadena, CA 91107, (213) 795-1699.

June 13-15
Systematic Software Maintenance, Chicago, IL. Topics to be addressed include structured methodologies, solutions for effective testing, resource allocation, and status determination. Full details are available from Eduteach Inc., Suite 907, 162 North State St., Chicago, IL 60601, (312) 641-1370.

June 14-16
Introduction to Microprocessors, University of Texas, Austin. This course will stress basic concepts and hands-on experience. Participants will write and run simple programs on a Z80-based Micro-Professor training system. Contact the College of Engineering, University of Texas, Austin, TX 78712, (512) 471-3396.

June 14-16
Ohmcon/83, High-Technology Electronics Exhibition and Convention, Cobo Hall, Detroit, MI. For information, contact Electronic Conventions Inc., 999 North Sepulveda Blvd., El Segundo, CA 90245, (800) 421-6816; in California, (213) 772-2965.

June 14-18
Tectronica, Earls Court Exhibition Centre, London, England. This exhibition on laboratory technology, aims to show the latest in instrumentation, equipment, and services for life and physical sciences. For details, contact Good Relations Ltd., 15 Adeline Place, London WC1B 3AJ, England; tel: (01) 636-6561; Telex: 265903.

June 15-17
Basics of Power Electronics, Los Angeles, CA. For information on this course, contact Teslaco, Suite 6, 490 South Rosemead Blvd., Pasadena, CA 91107, (213) 795-1699.

June 15-17
The Twenty-first Annual Meeting of the Association for Computational Linguistics, Massachusetts Institute of Technology, Cambridge, MA. Papers to be presented will address syntax, the representation of knowledge, machine and machine-aided translation, and other linguistically and computationally significant topics. Information is available from Don Walker, Artificial Intelligence Center, SRI International EJ278, Menlo Park, CA 94025, (415) 859-3071.

June 15-18
1984 Oceania Party Nominating Convention, London. Delegates to this plenipotentiary assembly will discuss the latest developments in viewscreen technology and select candidates for Inner-Party offices and for the office of Big Brother. For information, contact Eric Arthur Blair, Ministry of Truth, Wigan Pier, Craighouse, Jura, UK.

June 16-17
Clinical Laboratory Computers: Symposium 1983,

Event Queue

Towsley Center for Continuing Medical Education, Ann Arbor, MI. Course credit will be offered. Contact the Office of Continuing Medical Education, Towsley Center Box 057, University of Michigan Medical School, Ann Arbor, MI 48109, (313) 763-1400.

June 17-19

PC '83/West, Brooks Hall/Civic Center Complex, San Francisco, CA. This show will bring together users, developers, distributors, and retailers of products compatible with the IBM Personal Computer. Seminars, workshops, demonstrations, and a conference program will aim to educate users on product features and capabilities. Conference information is available from Northeast Expositions, 826 Boylston St., Chestnut Hill, MA 02167, (800) 841-7000; in Massachusetts, (617) 739-2000.

June 19-23

Conference on Computer Vision and Pattern Recognition–CVPR '83, Crystal City Hyatt, Arlington, VA. This program was formerly known as the Pattern Recognition and Image Processing Conference. Papers on vision, pattern recognition, and image processing will be delivered. For full details, write to CVPR '83, POB 639, Silver Spring, MD 20901.

June 23

The Twenty-second Annual Technical Symposium of the Washington DC Chapter of the Association for Computing Machinery, National Bureau of Standards, Gaithersburg, MD. The theme for this event is "Microcomputer Systems: Tools or Toys?" Topics of interest include systems software, human factors, and office systems. Contact Howard Weeks Associates, 15201 Shady Grove Rd., Rockville, MD 20850.

June 27-30

The World of CAD/CAM, Marriott Resort, Newport Beach, CA. This seminar consists of four one-day presentations: computer-aided engineering (CAE), computer-aided design (CAD), computer-aided manufacturing (CAM), and computer-integrated manufacturing (CIM). It seeks to give a complete overview of how manufacturing will change in the future as the automated factory becomes a reality. For a brochure, write or call the Center for Manufacturing Technology, 4170 Crossgate Dr., Cincinnati, OH 45236, (513) 791-8801.

June 28-30

National Educational Computer Conference, New York Statler, New York, NY. The theme is "Higher Instructional Techniques in Education." Seminars, exhibits, hands-on demonstrations, and workshops will highlight this event. Further information is available from the National Educational Computer Library, POB 293, New Milford, CT 06776, (203) 354-7760. ■

In order to gain optimal coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, POB 372, Hancock NH 03449. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

Books Received

Apple II Assembly Language Exercises, Leo J. Scanlon. New York: John Wiley & Sons, 1982; 205 pages, 50 by 66 cm, softcover, ISBN 0-471-86598-2, $9.95.

BASIC Analysis of Variance Programs for Microcomputers, Allen H. Wolach. Monterey, CA: Brooks/Cole Publishing Co., 1983; 162 pages, 44 by 55 cm, softcover, ISBN 0-534-01423-2, $8.95.

Basic Mathematics for Electronics, 5th edition, Nelson M. Cooke, Herbert F. R. Adams, and Peter B. Dell. New York: Gregg/McGraw-Hill, 1982; 698 pages, 46 by 58 cm, hardcover, ISBN 0-07-012514-7, $21.65.

The Computer Tutor, Learning Activities for Homes and Schools, Gary W. Orwig and William S. Hodges. Boston, MA: Little, Brown and Company, 1982; 203 pages, 50.5 by 66 cm, softcover, ISBN 0-87626-147-0, $10.95.

The Cosmic Mind-Boggling Book, Neil McAleer. New York: Warner Books, 1982; 207 pages, 31.6 by 47.6 cm, softcover, ISBN 0-446-97663-6, $7.95.

CP/M Simplified, Jeffrey R. Weber. Cleveland, OH: Weber Systems Inc. (8437 Mayfield Rd.), 1982; 316 pages, 32 by 51 cm, softcover, ISBN 0-938862-04-9, $13.95.

Developing Computer Solutions for Your Business Problems, Henry H. Petersohn. Englewood Cliffs, NJ: Prentice-Hall, 1982; 157 pages, 41 by 56 cm, softcover, ISBN 0-13-204305-X, $14.95.

The 8086/8088 Primer, 2nd edition, Stephen P. Morse. Rochelle Park, NJ: Hayden Book Co., 1982; 276 pages, 36.6 by 54 cm, softcover, ISBN 0-8104-6255-9, $10.95.

Engineering a Compiler, VAX-11 Code Generation and Optimization, Patricia Anklam, David Cutler, Roger Heinen Jr., and M. Donald MacLaren. Bedford, MA: Digital Press, 1982; 269 pages, 39 by 58 cm, hardcover, ISBN 0-932376-19-3, $24.

Exploring the Worlds of Computers, Donald D. Spencer. Ormond Beach, FL: Camelot Publishing Co., 1982; 102 pages, 37 by 56 cm, hardcover, ISBN 0-89218-055-2, $10.95.

49 Explosive Games for the ZX81, Tim Hartnell, ed. Reston, VA: Reston Publishing Co., 1981; 140 pages, 36 by 54 cm, softcover, ISBN 0-8359-2086-0, $10.95.

Fundamentals of Microcomputer Programming, Including Pascal, Daniel R. McGlynn. New York: John Wiley & Sons, 1982; 332 pages, 35 by 54 cm, softcover, ISBN 0-471-08769-6, $14.95.

How to Write and Publish Engineering Papers and Reports, Herbert B. Michaelson. Philadelphia, PA: ISI Press, 1982; 155 pages, 37 by 55 cm, hardcover, ISBN 0-89495-016-9, $17.95.

How to Write a TRS-80 Program, Ed Faulk. Chatsworth, CA: Datamost Inc. (9748 Cozycroft Ave.), 1982; 220 pages, 32 by 49.5 cm, softcover, ISBN 0-8359-2992-2, $14.95.

Introduction to Modern Information Retrieval, Gerard Salton and Michael J. McGill. New York: McGraw-Hill, 1983; 448 pages, 41 by 57.6 cm, hardcover, ISBN 0-07-054484-0, $32.95.

Invasion of the Space Invaders, Martin Amis. London, England: Hutchison & Co. Ltd. (17-21 Conway St.), 1982; 128 pages, 50 by 70 cm, softcover, ISBN 0-09-047841-3, $9.95.

Invitation to Ada & Ada Reference Manual, Harry Katzan Jr. Princeton, NJ: Petrocelli Books, 1982; 429 pages, 43 by 62 cm, hardcover, ISBN 0-89433-132-9, $29.95.

Language Translators, John Zarella. Suisun City, CA: Microcomputer Applications (POB E), 1982; 200 pages, 36 by 54 cm, softcover, ISBN 0-935230-06-8, $12.95.

Mastering Machine Code on Your ZX81, Toni Baker. Reston, VA: Reston Publishing Co., 1981; 180 pages, 36 by 54 cm, softcover, ISBN 0-8359-4261-9, $12.95.

The Microchip: Appropriate or Inappropriate Technology? Alan Burns. New York: Halsted Press, 1981; 180 pages, 36 by 55 cm, hardcover, ISBN 0-470-27206-6, $39.95.

Micro Cookbook, Volume 1: Fundamentals, Don Lancaster. Indianapolis, IN: Howard W. Sams & Co., 1982; 381 pages, 32 by 51 cm, softcover, ISBN 0-672-21828-3, $15.95.

Microprocessor Data Book, S. A. Money. New York: McGraw-Hill, 1982; 264 pages, 51 by 66 cm, hardcover, ISBN 0-07-042706-2, $38.

Microprocessor Operating Systems, volume II, John Zarella, ed. Suisun City, CA: Microcomputer Applications (POB E), 1982; 158 pages, 36 by 54 cm, softcover, ISBN 0-935230-04-1, $12.95.

101 Pocket Computer Programming Tips & Tricks, Jim Cole. Woodsboro, MD: Arcsoft Publishers, 1981; 128 pages, 33 by 51 cm, soft-

cover, ISBN 0-86668-004-7, $7.95.

Osborne CP/M User Guide, 2nd edition, Thom Hogan. Berkeley, CA: Osborne/McGraw-Hill, 1982; 280 pages, 39 by 55 cm, softcover, ISBN 0-931988-82-9, $15.95.

PATCA, Directory of Consultants, San Jose, CA: PATCA (Professional and Technical Consultants Association, Suite 3, 1190 Lincoln Ave.), 1982; 110 pages, 33 by 51 cm, softcover, ISBN 0-939-840-01-4, $5.

The PET Index, Michael A. F. Ryan. Aldershot, Hampshire, England: Gower Publishing Ltd. (Gower House, Croft Rd.), 1982; 194 pages, 49.6 by 70 cm, softcover, ISBN 0-566-03426-3, $12.50.

The Power of Supercalc, Robert E. Williams and Bruce J. Taylor. Englewood Cliffs, NJ: Prentice-Hall, 1982; 110 pages, 50 by 64.6 cm, softcover, ISBN 0-13-687301-4, $9.95.

The Power of Visicalc, Robert E. Williams and Bruce J. Taylor. Englewood Cliffs, NJ: Prentice-Hall, 1981; 88 pages, 50 by 64.6 cm, softcover, ISBN 0-13-687418-5, $9.95.

The Power of Visicalc, Real Estate, Patricia J. Hughes and Kaz Ochi. Englewood Cliffs, NJ: Prentice-Hall, 1981; 166 pages, 50.6 by 65 cm, softcover, ISBN 0-13-687350-2, $14.95.

The Power of Visiplot-Visicalc-Visifile, Patricia J. Hughes and Kaz Ochi. Englewood Cliffs, NJ: Prentice-Hall, 1981; 154 pages, 50.6 by 65 cm, softcover, ISBN 0-13-687368-5, $14.95.

Programming Concepts with the Ada Language, Roy S. Freedman. Princeton, NJ: Petrocelli Brooks, 1982; 162 pages, 33 by 49 cm, softcover, ISBN 0-89433-190-6, $12.

Programming the 6809, Rodnay Zaks and William Labiak. Berkeley, CA: Sybex, 1982; 362 pages, 35 by 54 cm, softcover, ISBN 0-89588-078-4, $14.95.

Programming Microcomputers with Pascal, M. D. Beer. New York: Van Nostrand Reinhold, 1982; 256 pages, 36 by 56 cm, softcover, ISBN 0-442-21368-9, $13.95.

Software Manual Production Simplified, Richard Zaneski. Princeton, NJ: Petrocelli Books, 1982; 190 pages, 33 by 51 cm, hardcover, ISBN 0-89433-180-9, $20.

So You Are Thinking About a Small Business Computer, R. G. Canning and N. C. Leeper. Englewood Cliffs, NJ: Prentice-Hall, 1982; 203 pages, 51 by 66 cm, softcover, ISBN 0-13-823617-8, $10.95.

SPPC Manual, A Statistical Package for the Pocket Calculator, Walter W. Hudson. Tallahassee, FL: Walmyr Publishing Co. (POB 3554, Leon Station), 1982; 330 pages, 36 by 54 cm, softcover, ISBN 0-942390-01-6, $14.95.

Using Computers in Mathematics, Gerald H. Elgarten, Alfred S. Posamentier, and Stephen E. Moresh. Reading, MA: Addison-Wesley, 1983; 575 pages, 52 by 57 cm, hardcover, ISBN 0-201-10450-4, $18.60.

Z8000 Handbook, Martin L. Moore. Englewood Cliffs, NJ: Prentice-Hall, 1982; 398 pages, 41 by 55 cm, softcover, ISBN 0-13-983866-X, $14.95.

The ZX81 Pocket Book, Trevor Toms. Reston, VA: Reston Publishing Co., 1981; 128 pages, 36 by 54 cm, softcover, ISBN 0-8359-9524-0, $10.95. ■

This is a list of books received at BYTE Publications during this past month. Although the list is not meant to be exhaustive, its purpose is to acquaint BYTE readers with recently published titles in computer science and related fields. We regret that we cannot review or comment on all the books we receive; instead, this list is meant to be a monthly acknowledgment of these books and the publishers who sent them.

BYTE's Bits

Computers Sparkle in Pearl City

A new pearl was added to the Pearl of New Jersey's string of casinos, hotels, and visitor attractions late last month. The grand opening of Ocean One, a three-level shopping, restaurant, entertainment, and exhibition hall resembling a 900-foot ocean-liner, was held at the end of March.

The highlight of Ocean One is Computerama 21, a year-round computer show featuring products from more than 30 computer manufacturers. Printers, software, and accessories will be on display, and a staff of trained technical personnel are on hand to answer questions.

Computerama is open 7 days a week, 14 hours a day. It's located on Arkansas Avenue, near the boardwalk. ■

Software Received

Apple

Accounts Payable, an accounting package. This module will maintain accounts-payable records and link with other State of the Art accounting packages. For the Apple III; floppy disk, $595. State of the Art, 3183-A Airway Ave., Costa Mesa, CA 92626.

A. E., an arcade-type game. The robots are running amuck, and you must destroy them or force them away from the earth. For the Apple II; floppy disk, $34.95. Broderbund Software Inc., 1938 Fourth St., San Rafael, CA 94901.

Air Navigation Trainer, a flight-simulation program. Pilots can watch a simulation of their flying techniques using navigation aids and making course corrections. For the Apple II and III; floppy disk, $40. Space-Time Associates, 20-39 Country Club Dr., Manchester, NH 03102.

Apple II Business Graphics, a utility package that performs data analyses and transforms numerical data into simple illustrations. For the Apple II; floppy disk, $175. Apple Computer Inc., 20525 Mariani Ave., Cupertino, CA 95014.

Bank Street Writer, a home-oriented word-processing system. This package includes all essential word-processing functions and features an interactive tutorial program on the disk. For the Apple II; floppy disk, $69.95. Broderbund Software Inc. (see address above).

BASIC Compiler+, a utility program to convert Apple*soft* BASIC programs into machine-language files. True integer arithmetic, array vectors, and optimal memory utilization are provided. For the Apple II; floppy disk, $99.95. Hayden Software Co., 600 Suffolk St., Lowell, MA 01853.

Bellhop, an arcade-type game. The object of this game is to pick up one piece of luggage at a time and deliver it to the correct suite until all seven pieces are delivered. Your tips depend on speed. For the Apple II; floppy disk, $34.95. Hayden Software Co. (see address above).

Black Jack Strategy, a program that allows you to test and analyze various strategies of playing blackjack. You set up the bets and the game-playing simulation to develop a winning strategy. For the Apple II; floppy disk, $69.95. Soft Images, 200 Route 17, Mahwah, NJ 07430.

Black/Kayles, an educational game. Play with a friend or against the computer to fill in the puzzle. The game helps students develop their mathematical strategies. For the Apple II Plus; floppy disk, $25. Island Software, Department B, POB 300, Lake Grove, NY 11755.

Championship Golf, a golf-simulation game for one to four players. Each hole is displayed from two angles. Players have a choice of 20 clubs. For the Apple II; floppy disk, $24.95. Hayden Software Co. (see address above).

Crime Stopper, an adventure-type game. You assume the role of a detective who must overcome many obstacles to locate a kidnapped heiress. For the Apple II; floppy disk, $34.95. Hayden Software Co. (see address above).

Crystal Caverns, an adventure-type game. Without a map, you must hunt for treasure in the caves beneath an old mansion. For the Apple II; floppy disk, $34.95. Hayden Software Co. (see address above).

Datafax, an unconstructed database-management system that uses keywords to organize non-numeric information. You can categorize and cross-reference information. For the Apple II and III; floppy disk, $199 and $249, respectively. Link Systems, 1640 19th St., Santa Monica, CA 90404.

Data Plotting Software for Micros, data-analysis tools. This collection of 21 data-plotting programs will help you analyze data and produce a variety of charts. For the Apple II; floppy disk, $19.95. Kern Publications, 190 Duck Hill Rd., POB 1029, Duxbury, MA 02332.

dBRx, a package of routines to expand the functional capabilities of Ashton-Tate's dBASE II. New functions include sine, cosine, logarithm, exponentiation, and square root. For the Apple II; floppy disk, $150. Gryphon Microproducts, POB 6543, Silver Spring, MD 20906.

Evolution, an adventure-type game. Work your way up the evolutionary ladder from amoeba to human while avoiding various predators. For the Apple II; floppy disk, $39.95. Sydney Development Corp., 600-1385 West 8th Ave., Vancouver, British Columbia V6H 3V9, Canada.

Final Conflict, a simulation game. You must program an army of robots to invade and destroy the enemy's central controller. Requires game paddle. For the Apple II; floppy disk, $34.95. Hayden Software Co. (see address above).

Financial Planning for Multiplan, a set of 17 templates to use with the Multiplan electronic-spreadsheet system. For the Apple II; floppy disk, $69.95. Howard W. Sams & Co. Inc., 4300 West 62nd St., POB 7092, Indianapolis, IN 46206.

Financial Planning for Visicalc, a set of 17 templates for use with the Visicalc electronic-spreadsheet system. For the Apple II; floppy disk, $69.95. Howard W. Sams & Co. Inc. (see address above).

Flip Out, an arcade-type strategy game. You are given 10 marbles. You must drop your marbles into the flip-out course in such a way that all your marbles exit before your opponent's. For the Apple II; floppy disk, $29.95. Sirius Software Inc., 10364 Rockingham Dr., Sacramento, CA 95827.

Foreign Language Series, a French or Spanish vocabulary drill package. Students can respond to quizzes by answering in either English or a foreign language. Special drills can be created. For the Apple II Plus; floppy disk, $80. Island Software (see address above).

General Ledger, an accounting package. This module will maintain a general ledger with simplified journal entry and audit trails, and will link with other State of the Art accounting packages. For the Apple III; floppy disk, $595. State of the Art (see address above).

Jigsaw, a set of four picture puzzles to assemble. Each puzzle has 24 pieces that you assemble on the screen. The set increases in difficulty. For the Apple II Plus; floppy disk, $25. Island Software (see address above).

Know Your Apple, an educational program that uses high-resolution pictures to demonstrate how the Apple computer works. For the Apple II; floppy disk, $34.95. Muse Software, 347 North Charles St., Baltimore, MD 21201.

Magic Mailer, a mailing-list management system. This program can merge a form-letter file with a data file or keyboard input to create customized form letters. For the Apple II Plus; floppy disk, $69.95. Artsci Inc., 5547 Satsuma Ave., North Hollywood, CA 91601.

Magic Window Diablo, a printer-driver program for the Diablo series of printers that uses the Magic Window word-processing system. For

the Apple II; floppy disk, $19.95. Artsci Inc. (see address above).

Magic Window NEC, a printer-driver program for the NEC Spinwriter that uses the Magic Window word-processing system. For the Apple II; floppy disk, $19.95. Artsci Inc. (see address above).

Magic Window II, a word-processing system. This improved version of the Magic Window system features a 70-column uppercase and lowercase display, 160-character line length, and hard-disk support. For the Apple II; floppy disk, $149.95. Artsci Inc. (see address above).

Magic Words, a spelling-checker system. This program features a 14,000-word dictionary that can be customized. It works with any Apple-compatible word-processing program that uses standard Apple DOS. For the Apple II; floppy disk, $69.95. Artsci Inc. (see address above).

Microbe: The Anatomical Adventure, an adventure game based on medical facts. You command a miniature submarine through your patient's body, fighting off deadly organisms as you go. For the Apple II; floppy disk, $44.95. Synergistic Software, Suite 201, 830 North Riverside Dr., Renton, WA 98055.

Micro Mother Goose, a set of games and animated stories. Designed for children aged 3 to 9 years, this package provides three games and nine animated comics with traditional music. For the Apple II; floppy disk, $39.95. Software Productions Inc., 2357 Southway Dr., POB 21341, Columbus, OH 43221.

Modula-2, a general-purpose programming language designed for systems implementation. Written by Niklaus Wirth, the author of Pascal, Modula-2 is based in part on Pascal and features modules and separate compilation. For the Apple II and III; floppy disk, $550. Volition Systems, POB 1236, Del Mar, CA 92014.

Paint Master, a design utility program that allows you to draw or paint high-resolution pictures on the screen, fill in colored sections, and save the drawings on disk. For the Apple II Plus; floppy disk, $34.95. Avant-Garde Creations, POB 30160, Eugene, OR 97403.

Pandemonium, a challenging word game that contains a built-in dictionary. See how many words you can spell from the letters in a 5 by 5 grid. For one or more players. For the Apple II; floppy disk, $39.95. Soft Images (see address above).

The Prime Plotter, a statistical-analysis and graphics development package. Using menu-driven commands, you can create a variety of charts and have them printed or drawn by a plotter. For the Apple II Plus; floppy disk, $239.95. Primesoft Corp., POB 40, Cabin John, MD 20818.

Puss **in Boot,** an educational program to teach positional concepts to children from preschool through the primary grades. Graphics appear at random to demonstrate In, Out, Left, Right, On, Off, Over, Under, and more. For the Apple II Plus; floppy disk, $25. Island Software (see address above).

Repton, an arcade-type game. You control the Star Fighter *Armageddon*. Your mission is to save Repton from the Quarriors. You have a laser gun, radar screen, and energy shields. For the Apple II; floppy disk, $39.95. Sirius Software Inc. (see address above).

Roadsearch, a computerized road atlas. This database of 406 cities and road junctions in the U.S. and Canada allows you to enter a starting point and a destination. You receive a detailed route plan for your next trip by car and save time, money, and gas. For the Apple II Plus; floppy disk, $34.95. Columbia Software, POB 2235, Columbia, MD 21045.

Sea Dragon, an arcade-type game. You must navigate the nuclear submarine *Sea Dragon* through a sea filled with deadly obstacles. For the Apple II; floppy disk, $34.95. Adventure International, POB 3435, Longwood, FL 32750.

Senior Analyst, a modeling program that allows financial planners to analyze and review data. Create models from a common database within the program, or combine many models into one. For the Apple II; floppy disk, $225. Apple Computer Inc. (see address above).

U.S. Cities, an educational program. Students learn to use a map of the United States. Coordinate locations of major cities are shown on high-resolution displays. For the Apple II Plus; floppy disk, $25. Island Software (see address above).

Wavy Navy, an arcade-type game. You pilot a PT boat in 30-foot waves while surrounded by enemy planes, helicopters, mines, and missiles. For one to four players. For the Apple II; floppy disk, $34.95. Sirius Software Inc. (see address above).

Atari

Bulldog Pinball, an arcade-type game. This computer version of a pinball game lets you score points, use flippers, and control ball speed. It features graphics and sound. For the Atari 400/800; cassette, $29.95. Hayden Software Co., 600 Suffolk St., Lowell, MA 01853.

Castle Wolfenstein, an adventure-type game. You have been captured by Nazis and taken to Castle Wolfenstein for interrogation. You must find the secret war plans and escape. For the Atari 400/800; floppy disk, $29.95. Muse Software, 347 North Charles St., Balimore, MD 21201.

Dragonfire, a video game. Help the prince reclaim the king's treasures. Cross bridges and dodge dragon fire in the quest. For the Atari Video Computer System; cartridge, $32.95. Imagic, 1875 Dobbin Dr., San Jose, CA 95133.

River Raid, an arcade-type game. You are piloting a B-1 strato-wing assault jet. Your mission is to seek and destroy enemy targets on a dangerous river course. For the Atari Video Computer System; cartridge, $31.95. Activision Inc., Drawer #7286, Mountain View, CA 94042.

Sea Dragon, an arcade-type game (see description under Apple). For the Atari 400/800; floppy disk, $34.95. Adventure International, POB 3435, Longwood, FL 32750.

Serpentine, an arcade-type game. You control three blue serpents. Your object is to destroy the hostile orange serpents and create more blue ones. For the Atari 400/800; floppy disk, $34.95. Broderbund Software Inc., 1938 Fourth St., San Rafael, CA 94901.

Speed Track, a simulation game. Place your bets, watch six horses race toward the finish line, and collect your winnings. For up to eight players. For the Atari 400/800; cassette, $19.95. Brenner, POB 459, Plainview, NY 11803.

Strätos, an arcade-type game. One or two players can defend a futuristic city from attack by alien spacecraft. For the Atari 400/800; floppy disk, $34.95. Adventure International (see address above).

Wayout, an arcade-type game. You have a choice of 26 three-dimensional mazes to explore. Look for the fireflies, but beware of the Cleptangle. Wayout glasses and compass included. For the Atari 400/800; floppy disk, $39.95. Sirius Software, 10364 Rockingham Dr., Sacramento, CA 95827.

Commodore

AC Network Analysis, a program to analyze an AC network with both passive components and transistors. Results are in decibel magnitude, return loss, and phase. For the Commodore 64, PET, and VIC-20; cassette, $25. R. K. Altenbach, 31 Garner Rd., Stow, MA 01775.

Beginners Assembly Language Programming, a book and software combination that teaches the basics of assembly-language programming. For the Commodore VIC-20; cassette. Price not available. Honeyfold Software Ltd., Standfast House, Bath Place, High St., Barnet, London, England.

Conquer, a medieval strategy game. The object of this game is to conquer as many countries as possible. For 1 to 15 players. For the Commodore VIC-20; floppy disk or cassette, $16.95. Computer Knowledge, 100 Grove St., Worcester, MA 01605.

The Dungeon, an arcade-type game. Escape an ever-expanding dungeon while meeting monsters, thieves, trap doors, secret keys, coffins, gold, swords, and much more. For the Commodore VIC-20; cassette, $15. Softwar III, 1307 Douglas Dr., Sterling, IL 61081.

Vanilla PILOT, an implementation of the PILOT language. This interpreter-based package features turtle graphics and enhanced editing commands. For the Commodore 64 and VIC-20; floppy disk, $29.95. Tamarack Software, Water St., Darby, MT 59829.

CP/M

Compress, a data-compression program for CP/M files. Storage requirements can be reduced 30 to 40 percent. It is based on a logarithmic relation between relative-letter frequency and bit length. For CP/M-based systems; floppy disk, $59.95. Digital Marketing Inc., 2670 Cherry Lane, Walnut Creek, CA 94596.

DES-Crypt Version 1.0, an implementation of the National Bureau of Standards' Data Encryption Standard (DES). This menu-driven package encrypts and decrypts your files. For CP/M-based systems; floppy disk, $149. Trigram Systems, 3 Bayard Rd. #66, Pittsburgh, PA 15213.

Disk Inspector, a full-screen editor for CP/M-based files. It displays selected sectors in both ASCII and hexadecimal formats. Make changes and rewrite the sector by moving the cursor. For CP/M-based systems; floppy disk, $29.95. Overbeek Enterprises, POB 726, Elgin, IL 60120.

Peachtext Word Processor, a full-featured word-processing package. It provides menu selection for functions, help display, print formatting, and self-teaching lessons. For CP/M-based systems; floppy disk, $500. Peachtree Software Inc., Suite 1300, 3445 Peachtree Rd. NE, Atlanta, GA 30326.

Solomon Series Software, an integrated accounting system that includes general ledger, accounts receivable and payable, invoicing, payroll, address and job-cost management. For CP/M-based systems; floppy disk, $3495. Computech Group Inc., Main Line Industrial Park, Lee Blvd., Frazer, PA 19355.

Spelling Proofreader, a spelling-checker package. Based on the *Random House Dictionary*, this program works with the Peachtext word-processing system to check the spelling of your documents. For CP/M-based systems; floppy disk, $300. Peachtree Software Inc. (see address above).

Y-Wing II, an arcade-type game. Stormslayer has enslaved all creatures under the sea. Your mission is to fly your Y-Wing fighter through the Stygian Sea and slay the

sea giant himself. For CP/M-based systems; floppy disk, $21.50. Evryware, POB 60802, Sunnyvale, CA 94088.

Heath/Zenith

Empire, a simulated war game. Your army is fighting the computer's army. As the forces move over a grid of unknown territory, your task is to contact and destroy the enemy. For the Heathkit H-11; 8-inch floppy disk, $40. Northwest Software, 15343 Southeast 43 Place, Bellevue, WA 98006.

Extended Tiny BASIC Compiler, a BASIC compiler program. Convert your BASIC programs into fast machine language. Requires HDOS 1.6. For Heath/Zenith computers; floppy disk, $31.95. O'Connor Software, 191 Oakridge Dr., Lower Burrell, PA 15068.

Y-Wing II, an arcade-type game (see description under CP/M). For Heath HDOS-based systems; floppy disk, $21.50. Evryware, POB 60802, Sunnyvale, CA 94088.

IBM Personal Computer

Air Traffic Controller, a simulation game. You must direct air traffic. Several options allow you to tailor the game to your preferences: successfully land planes or cause crashes for a high score. For the IBM Personal Computer; floppy disk, $29.95. Avant-Garde Creations, POB 30160, Eugene, OR 97403.

Data Plotting Software for Micros, a data-analysis program (see description under Apple). For the IBM Personal Computer; floppy disk, $19.95. Kern Publications, 190 Duck Hill Rd., POB 1029, Duxbury, MA 02332.

Deadline, an interactive program in which you are a detective who must solve a murder within 12 game hours. The program gives you all the clues you need. For the IBM Personal Computer; 5¼- and 8-inch floppy-disk formats, $49.95 and $59.95, respectively. For information, contact Infocom, 55 Wheeler St., Cambridge, MA 02138.

Federation, an arcade-type game. You command a Federation fleet. Your mission is to wipe out invading Drorn Drones. For the IBM Personal Computer; floppy disk, $29.95. Avant-Garde Creations (see address above).

Financial Planning for Multiplan (see description under Apple). For the IBM Personal Computer; floppy disk, $79.95. Howard W. Sams & Co. Inc., 4300 West 62nd St., POB 7092, Indianapolis, IN 46206.

Financial Planning for Supercalc, a set of 17 templates for use with the Supercalc electronic-spreadsheet system. For the IBM Personal Computer; floppy disk, $79.95. Howard W. Sams & Co. Inc. (see address above).

Financial Planning for Visicalc (see description under Apple). For the IBM Personal Computer; floppy disk, $79.95. Howard W. Sams & Co. Inc. (see address above).

Label Kit PC Disk Organizer, a user-friendly system that prints labels of your alphabetically arranged files. Kit includes a program disk, 300 pin-feed labels, and instructions. For the IBM Personal Computer; floppy disk, $59.95. PC Goodie Co., Suite 10, 15445 Ventura Blvd., Sherman Oaks, CA 91413.

Lazermaze, an arcade-type game. In the Arena Grid of Justice, your laser will reflect off many obstacles. A keen eye and trigger finger mean victory. For the IBM Personal Computer; floppy disk, $29.95. Avant-Garde Creations (see address above).

Name & Address List Management System, a simple database-management program designed to maintain lists of names and addresses. You can print listings and mailing labels according to several options. For the IBM

Personal Computer; floppy disk, $29.95. M & J Automation, POB 205, Plainsboro, NJ 08536.

Starcross, an adventure-type game. You must explore an alien starship and solve the complex and puzzling alien mysteries. For the IBM Personal Computer; floppy disk, $39.95. Infocom (see address above).

Terran Jeopardy, an arcade-type game. Pit your strategic skills against the Black Nebula Horde. Terra's fate is in your hands as you defend your base from alien attack. For the IBM Personal Computer; floppy disk, $29.95. Avant-Garde Creations (see address above).

Zork I: The Great Underground Empire, an adventure-type game. Strive to discover the Twenty Treasures of Zork and escape with them and your life. The game features a Save option for continued play. For the IBM Personal Computer; 5¼- and 8-inch floppy-disk formats, $39.95 and $49.95, respectively. Infocom (see address above).

Zork II: The Wizard of Frobozz, an adventure-type game. A continuation in the series, this game takes you deeper into the subterranean realm where you meet the powerful Wizard. For the IBM Personal Computer; 5¼- and 8-inch floppy-disk formats, $39.95 and $49.95, respectively. Infocom (see address above).

Zork III: The Dungeon Master, an adventure-type game. This is the final test in the series. You must fight the Dungeon Master himself. For the IBM Personal Computer; 5¼- and 8-inch floppy-disk formats, $39.95 and $49.95, respectively. Infocom (see address above).

Texas Instruments

Data Rescue, an arcade-type game. See if you can recover the stolen data-bank models and return them to earth. For the TI-99/4A; cassette, $9.95. Kuhl Software, 412 15th Ave. SW, Rochester, MN 55901.

The Dungeon, an arcade-type game (see description under Commodore). For the TI-99/4A; cassette, $15. Softwar III, 1307 Douglas Dr., Sterling, IL 61081.

TRS-80

Alphabet Soup, a competitive spelling game with nine skill levels. Once the program generates 5 to 14 letters, you have 200 seconds to spell as many words as you can. For the TRS-80 Color Computer; cassette, $14.95. Creative Technical Consultants, 16-8 Sangre de Cristo, POB 652, Cedar Crest, NM 87008.

Cyberchess System Program, a chess-tutorial program. This chess-analysis system will play games according to your level of expertise, set up classic games, and rate a player's ability. For the TRS-80 Models I and III; floppy disk, $29.95. I.J.G. Inc., 1953 West 11th St., Upland, CA 91786.

ZX80/ZX81

Bon Mot, an educational game that teaches vocabulary and spelling skills. Up to 6 players can choose from 11 different anagram games. For the ZX80/ZX81; cassette, $9.99. Luther A. Gotwald Jr., POB 404, Davidsville, PA 15928.

Musical Scales, a program to convert any series of notes from one musical scale to another. Scales included are Ionian, Dorian, Phrygian, Lydian, Mixolydian, Aeolian, Locrian, and harmonic minor. For the Timex/Sinclair 1000 and ZX81; cassette, $14.95. Rave Records, 1005 Mechanic St., Decorah, IA 52101.

Schedi-Mort, an amortization-scheduler program. You can compute complete schedules of payments, principal, interest, and remaining balance on any loans. For the Timex/Sinclair 1000 and ZX81; cassette, $20. E. Arthur Brown Co., 1702 Oak Knoll Dr., Alexandria, MN 56308.

Other Computers

Dragonfire, a video game (see description under Atari). For the Mattel Intellivision; cartridge, $39.95. Imagic, 1875 Dobbin Dr., San Jose, CA 95133.

Empire, a simulated war game (see description under Heath/Zenith). For the Digital Equipment Corporation LSI-11, 8-inch floppy disk, $40. Northwest Software, 15343 Southeast 43 Place, Bellevue, WA 98006.

Recipe Organizer, a program that stores and retrieves up to 200 recipes on one disk. For the Intertec Superbrain; floppy disk, $29.95. The Office Partner Inc., 6736 Brookcrest Dr., Charlotte, NC 28210. ■

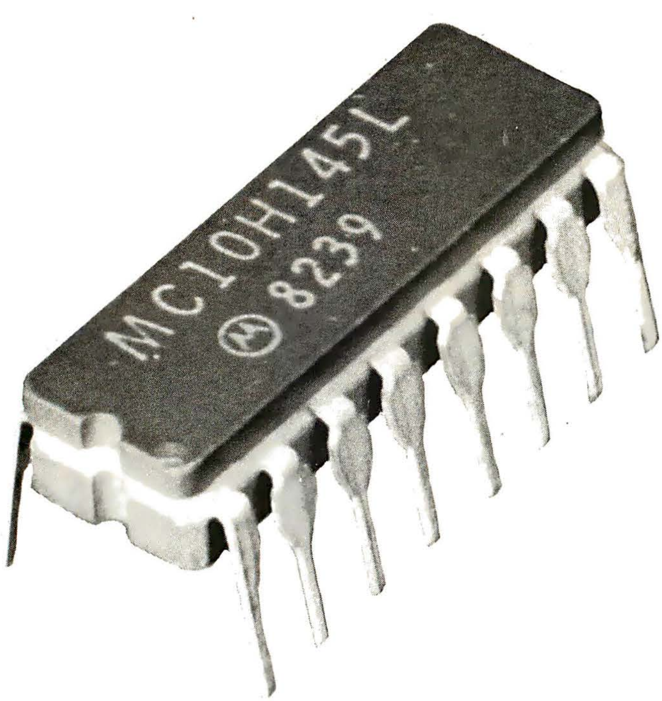
This is a list of software packages that have been received by BYTE Publications during the past month. The list is correct to the best of our knowledge, but it is not meant to be a full description of the product or the forms in which the product is available. In particular, some packages may be sold for several machines or in both cassette and floppy-disk format; the product listed here is the version received by BYTE Publications.

This is an all-inclusive list that makes no comment on the quality or usefulness of the software listed. We regret that we cannot review every software package we receive. Instead, this list is meant to be a monthly acknowledgment of these packages and the companies that sent them. All software received is considered to be on loan to BYTE and is returned to the manufacturer after a set period of time. Companies sending software packages should be sure to include the list price of the packages and (where appropriate) the alternate forms in which they are available.

See other ad on page 178.

What's New?

NEW CHIPS



RAM Has 3-Nanosecond Access Time

Motorola's 64-bit MC10H145 bipolar ECL RAM (random-access read/write memory) can be used in any memory storage system requiring high-speed access times. This device, a member of the MECL 10KH family, has a 3-ns (nanosecond) address access time (typical) with 6 ns maximum. It's organized as a 16 by 4 memory array and engineered with Motorola's MOSAIC (Motorola oxide self-aligned implanted circuit) oxide-isolated process, which achieves a purported smaller device geometry, improved bandwidth, and reduced parasitic capacitances. It's completely compatible with the Motorola MECL 10K family and offers an improved noise margin (150 millivolts) and voltage consumption. The memory cell array features a write and data input buffer, an address buffer and decoder, data output buffers, and a chip select.

Prototype quantities of the MC10H145 are available in ceramic and plastic DIPs (dual-inline packages). In 100-unit lots, these versions cost $10.65 and $9.25 each, respectively. Contact Motorola Semiconductor Products Inc., 5005 East MacDowell Rd., Phoenix, AZ 85008, (602) 962-2202.

Circle 550 on inquiry card.

High-Speed Math Chip

Oki Semiconductor's general-purpose 8-bit MSM6203 mathematics circuit is said to be fast enough for radar data correlation and industrial process-control systems. It is built with silicon-gate CMOS (complementary metal-oxide semiconductor) technology and has eight bidirectional I/O pins. It readily connects to such 8-bit microprocessors as Oki's 80C85A. The MSM6203 can perform 8-by 8-bit multiplication or 16- by 8-bit division operations in 3.3 microseconds. Power consumption is 6.5 millwatts per MHz during arithmetic operation, and the maximum operating frequency is 4 MHz (50% duty cycle). It's housed in an 18-pin plastic DIP (dual-inline package).

The MSM6203 costs $7.50 each, in 100-piece quantities. Contact Oki Semiconductor Inc., Suite 401, 1333 Lawrence Expressway, Santa Clara, CA 95051, (408) 984-4842.

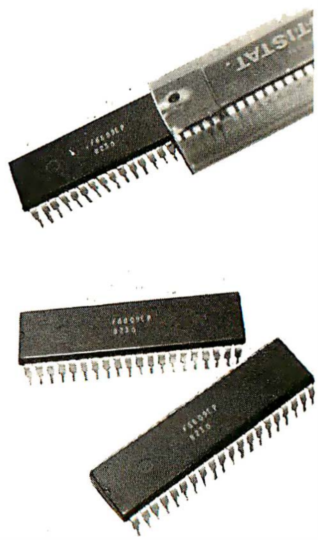
Circle 551 on inquiry card.

Speedy PROM

The 6353-2 is a 4K-byte nickel chromium PROM (programmable read-only memory) from Monolithic Memories. This chip, organized as 1024 words of 4 bits each, features an address access time of 50 ns (nanoseconds) worst case; 35 ns (typical). Its power consumption is 140 mA (milliamperes), and output leakage current is 40 μA (microamperes). According to the company, the 6353-2 can be used as a logic element because of its speed. Other applications include program or microcode storage, lookup tables, and character generators. The 6353-2 PROM is housed in an 18-pin 0.3-inch-wide ceramic package.

In lots ranging from 100 to 999, the 6353-2 costs $5.25 each. Monolithic Memories Inc., 1165 East Arques Ave., Sunnyvale, CA 94086, (408) 739-3535.

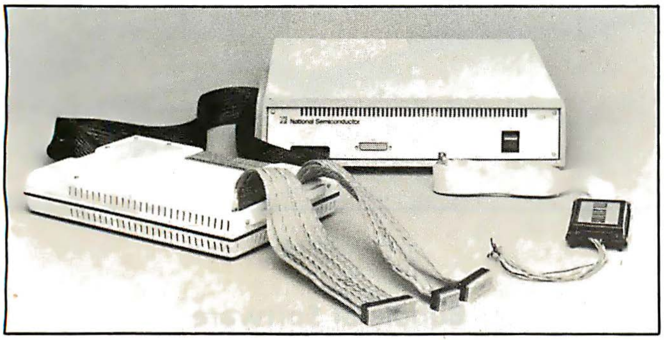
Circle 552 on inquiry card.



New Member of F6800 Family

Fairchild has added the F6809E to its 8-bit F6800 microprocessor family. This high-performance chip features 16-bit registers, dual 8-bit data paths, 59 basic instructions, the ability to recognize 1464 different variations of instructions and addressing modes, and external clock inputs that permit synchronization with peripherals, systems, or other microprocessors. The F6809E is compatible at the hardware and software levels with the F6800 family.

The F6809E microprocessor is available in three speeds: 1, 1.5, and 2 MHz. Quantities can be ordered through local sales offices or franchised distributors. For further details, contact Product Marketing, Fairchild Microprocessor Division, 3420 Central Expressway, Santa Clara, CA 95051, (408) 773-2102.
Circle 553 on inquiry card.



In-System Emulator

The NS-ISE-16 is the vanguard of National Semiconductor's series of In-System Emulators (ISE) for its 16/32-bit NS16000 microprocessor family. A multihost emulator family, the ISE/16 line lets users test and debug both hardware and software on their own 16000-family-based designs. The NS-ISE-16 provides real-time emulation of the NS16032 processor, the NS16201 TCU (timing-control unit), and the NS16082 MMU (memory-management unit). The package has three basic components: an emulation support box, an emulation pod, and a TTL (transistor-transistor logic) status pod. Also provided is the IDBG16 software debugging program, resident on the host computer system. (The IDBG16 is a superset of the NS16000 cross-software debugger, DGB16.)

The NS-ISE-16 currently communicates with a Digital Equipment Corporation VAX/11 host system. Its two RS-232C ports permit transparent mode communication with the host computer. This means that one port is connected to the VAX while the other connects with the user's terminal, permitting direct communication between the ISE and the VAX for faster response. The user's terminal functions as a command console.

The NS-ISE-16 is supplied with an IEEE-488 GPIB po t that will allow it to communicate with future host systems. Other standard features include up to 30K bytes of memory-mapping space, write protect/detect of 2K-byte blocks, and program-flow trace of up to 256 nonsequential fetches. This device is presently specified for operation at speeds of up to 6 MHz, with future upgrades planned to operate at 10 MHz.

The NS-ISE-16 costs $7500, including the interactive debugger program. Contact National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051, (408) 721-5000.
Circle 554 on inquiry card.

SYSTEMS

Complete Color Graphics System

The Executive Presentation System (EPS) from Intelligent Systems Corporation is said to provide all the hardware and software you need to prepare presentation-quality color graphic visuals. With EPS, you can create overhead projector transparencies, 35 mm slides, and paper prints and plots. EPS software includes CP/M, Microsoft BASIC, and a graphics language that uses such English-statement commands as pie, bar, and line. EPS is device-independent, which lets you use a variety of output peripherals, including color plotters, camera systems, and ink-jet printers. This system is built around the Intecolor 8001R color graphics terminal and the Intecolor 7000 computer.

The Intecolor 8001R features individual dot addressability, 96K bytes of RAM (random-access read/write memory) with red/green/blue readable bit map, a 4K-byte graphics command processor in ROM (read-only memory) with 20 functions, 4K bytes of command software in ROM to handle routines, and an 8K-byte RAM-based low-resolution memory plane for alphanumerics and graphics, with 96 uppercase and lowercase ASCII characters. Its hardware includes two RS-232C ports, one 8-bit parallel printer port, and a 177-key ASCII keyboard with 28 function keys. The Intecolor 7000 offers 128K bytes of RAM, a scrolling text editor, and dual 8-inch floppy-disk drives with 2.4 megabytes of data space and full-track disk buffer for fast throughput.

An 8-pen color plotter, a color camera system, and a color ink-jet printer are available as options. Prices begin at $18,000, which includes an output option. For details, contact Intelligent Systems Corp., 225 Technology Park/Atlanta, Norcross, GA 30092, (404) 449-5961.
Circle 555 on inquiry card.

Eagles Are IBM PC-Compatible

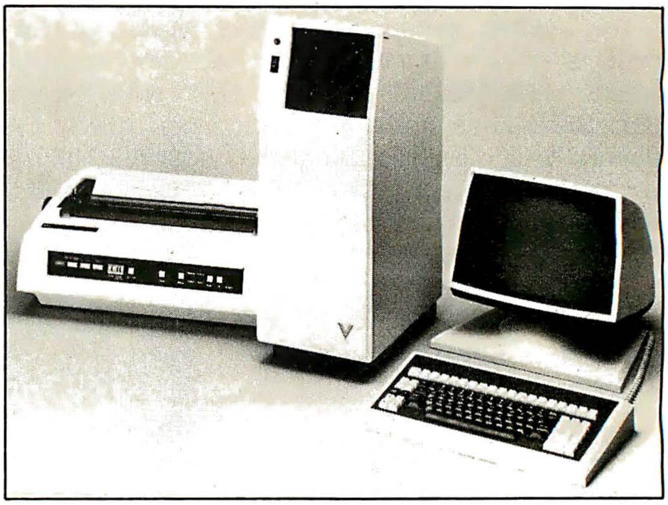
The Eagle 1600 Series of 16-bit computers is compatible with the IBM Personal Computer. According to the company, this series combines all the features of the PC at up to four times the operating speed. The 1600 computers are fully upgradable and come with networking capabilities and word-processing and financial planning software.

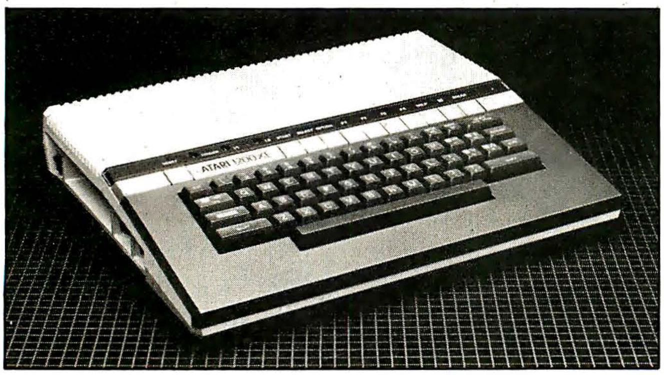
The basic system, the Model 1630, has 128K bytes of RAM (random-access read/write memory), 1

megabyte of 5¼-inch floppy-disk storage, 12.5 megabytes of hard-disk storage, a detachable 105-key keyboard with 24 user-definable keys, and a separate monitor and 8086 microprocessor, which operates at 8 MHz. Its internal memory is expandable to 512K bytes, and up to eight PC plug-compatible boards can be added for peripherals. Additional software available from Eagle includes general accounting, medical and dental practice management, and CPA accounting.

The Model 1630 costs $6995. Contact Eagle Computer Inc., Building C, 983 University Ave., Los Gatos, CA 95030, (408) 395-5005.

Circle 556 on inquiry card.





Atari 1200XL

The Atari 1200XL home computer comes with 64K bytes of RAM (random-access read/write memory), 12 user-programmable function keys, and built-in diagnostics. Its keyboard permits shifting into an integral European character set that includes special currency and character symbols. A Help key is standard as are one-touch cursor controls, 256 available colors for a monitor, and a speaker with 4 voices and a 3½-octave range. The 1200XL is compatible with Atari peripherals and software products.

Options for the 1200XL include a cassette memory system, an 80-column printer, and a 40-column printer/plotter. The memory system, the Model 1010 Program Recorder, uses standard audio cassettes and features two channels for both a program and sound effects. The Model 1025 printer prints dot-matrix characters at 40 cps (characters per second) and accepts single-sheet, fan-fold, and rolled paper. The Model 1020 Color Printer/Plotter produces four-color text, complex charts, and graphs to any set of X,Y coordinates. Prices range from $99.95 to $549. The 1200XL costs less than $1000. Full details are available from Atari Inc., 1265 Borregas Ave., POB 427, Sunnyvale, CA 94086.

Circle 557 on inquiry card.

Bundle of Software Comes with Business System

The Voyager 4000 series of small business computers comes with the CP/M operating system and word processing, spreadsheet with graphics, database management, mailing list, payroll, Telex, and time management software. The basic Voyager has RS-232C and RS-422A ports, dual 5¼-inch double-sided double-density floppy-disk drives (1.2 megabytes of storage), and an 8085 central processor that addresses 64K bytes of RAM (random-access read/write memory). The central processor is upgradable to 8085/8088-based 8- and 16-bit coprocessor operation, addressing 1000K bytes of RAM. Up to 20 megabytes of plug-in hard-disk storage is available. The series also features an adjustable 12-inch nonglare video monitor with dedicated memory and an 8 by 12 matrix on a 10 by 14 grid with a choice of three colors. The computer's detachable keyboard has 100 five-function keys and a 10-key numeric pad.

The Voyager 4000 costs $4995, including the software. Dealer and OEM (original equipment manufacturer) discounts are available. Contact Voyager Systems Inc., 2192 Anchor Court, Newbury Park, CA 91320, (213) 991-9028.

Circle 558 on inquiry card.

Multiuser Telesystem Runs Unix III

A Motorola MC68000-based computer running the Unix III operating system is being marketed by Televideo Systems Inc. The Telesystem II supports up to 16 users and offers interface flexibility by means of 15 serial ports, one RS-422A port, a Centronics-compatible parallel port, and bus expansion capabilities. Standard features include 512K bytes of RAM (random-access read/write memory) and an 8-inch 40-

or 80-megabyte Winchester hard-disk drive backed up by a 17.5-megabyte streaming cartridge tape. RAM memory can be expanded to 1 megabyte in 256K-byte increments, and an additional 40- or 80-megabyte drive can be attached for a total storage capacity of 160 megabytes. The operating speed is 8 MHz, and the MC68000 is complemented with an MMU (memory-management unit) chip. Software available includes COBOL, Pascal, C, and FORTRAN-77.

The Telesystem II costs less than $14,000, which includes 40 megabytes of disk storage, the backup tape drive, Unix III, and two Televideo displays. Further details are available from Televideo Systems Inc., 1170 Morse Ave., Sunnyvale, CA 94086, (408) 745-7760.

Circle 559 on inquiry card.



Dual Processors Provide Flexibility

The Micro 16S personal business computer from Fujitsu Ltd. gives you integrated 8- and 16-bit processing power flexibility. The Micro 16S uses the Zilog Z80 and Intel's 16-bit 8086 for its main processors. The Z80 runs the CP/M 2.2 operating system, while the 8086 supports up to 1 megabyte of memory.

Mass storage is supplied by dual 5¼-inch floppy-disk drives, each capable of handling more than 312K bytes of formatted data. User memory is provided by 125K bytes of parity-checking RAM (random-access read/write memory), expandable to 1 megabyte. This system has high-resolution color graphics capabilities that are backed by more than 50K bytes of support RAM. Its dedicated display processor generates high-resolution (640 by 200) color graphics. Other standard features are parallel and serial output ports and a typewriter-style detachable keyboard with a separate numeric keypad and 10 programmable function keys.

The Micro 16S comes with the CP/M-86 operating system, a word processor, an electronic spreadsheet, and a color monitor. Options include a 10-megabyte 5¼-inch Winchester-disk drive, a link to Corvus Systems' Omninet network, and Concurrent CP/M-86, which lets the Micro 16S run four jobs simultaneously with each task using up to 250K bytes of memory. Its base price is $3995. For full details, contact Fujitsu Ltd., Professional Microsystems Division, 2840 San Tomas Expressway, Santa Clara, CA 95051, (408) 980-0755.

Circle 560 on inquiry card.

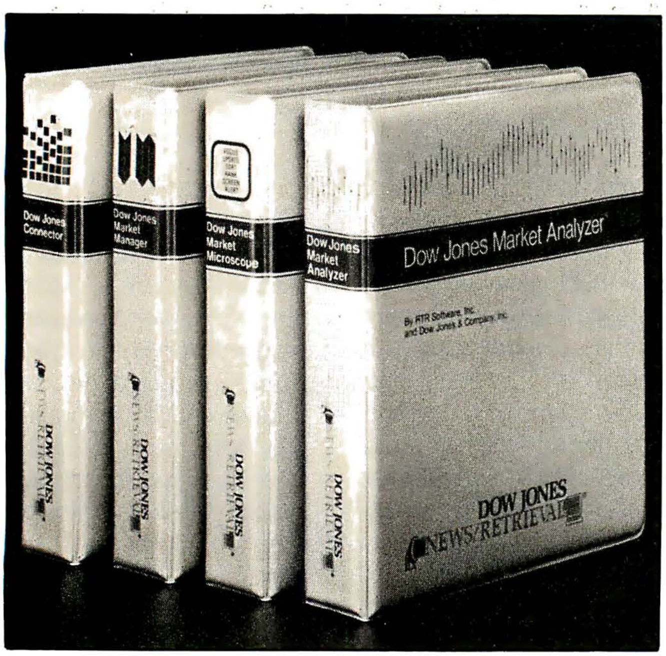
SOFTWARE

Software Line for Lisa Unveiled

Open Systems will distribute Xenix-based software products for Apple Computer's recently announced Lisa computer. This line, targeted at the small-business market, will include Science Management Corporation's (SMC's) Business BASIC interpreter, seven interactive accounting applications packages, and a report writer. The accounting packages include order processing, general ledger, accounts receivable with billing and sales analysis, payroll, and job cost. The report writer, to be marketed under the name The Team Manager, will link the accounting applications to a comprehensive data dictionary, which will allow creation of simple or complex reports from all files within the accounting system. It will also permit reformatting of data from the accounting applications for use by word processing, spreadsheet, and other productivity applications available under Xenix.

Open Systems will directly license the Xenix-based software to Apple dealers. In addition, it will provide all packaging, training, and support. For further details, contact Open Systems Inc., 430 Oak Grove, Minneapolis, MN 55403, (612) 870-3515.

Circle 561 on inquiry card.



Dow Jones Markets Software

Dow Jones & Company offers software programs designed to meet the business and investment needs of personal computer users. Dow Jones software runs on such systems as the Apple II and the IBM Personal Computer. Customer and dealer support includes a one-year warranty and a toll-free customer service department.

The Dow Jones Market Analyzer automatically collects, stores, and updates stock market data that can be used to construct charts for technical analysis. The Market Microscope sorts and ranks companies and industries by 68 financial indicators. For automatic updates and monitoring of investment portfolios, the Market Manager is offered. Also available is the Dow Jones Connector, which provides users of most microcomputers with access to news, information, and data contained in the Dow Jones News/Retrieval database.

Prices range from $95 to $700. For full hardware details or purchasing information, contact Dow Jones & Co. Inc., POB 300, Princeton, NJ 08540, (800) 257-5114; in New Jersey (609) 452-1511.
Circle 562 on inquiry card.

Smart Terminal Program Housed in ROM

The Colorcom/E from Spectrum Projects is a smart terminal program for the Radio Shack Color Computer. Colorcom/E, housed in a ROM (read-only memory) cartridge, provides you with online and offline scrolling, offline printing of data, full- and half-duplex operation, and the ability to receive and send cassette files. It will support any serial printer, and it permits easy editing before data is printed or written to cassette.

A word mode that eliminates word wrap is offered as an option. Colorcom/E costs $49.95 and is available from Spectrum Projects, 93-15 86th Dr., Woodhaven, NY 11421, (212) 441-2807.
Circle 563 on inquiry card.

Graphics System for dBASE II

Fox & Geller's dGraph lets you produce high-quality charts from any Ashton-Tate dBASE II database. According to the manufacturer, all you have to do is enter the data or the name of the dBASE II database you wish to chart and dGraph will do the rest. A chart-description procedure lets you create bar, pie, line, and pie-bar charts that include such information as the percent of total based on summing or counting. Other possible uses include summing, counting, and averaging of data fields and automatic selection of data based on ranges and on matched values. dGraph can function as a stand-alone system, and it supports a variety of printers and plotters, including Epson MX-70/80/100, Okidata Microline, and Xerox/Diablo 1750.

The dGraph system runs on CP/M-, CP/M-86-, or MS-DOS-based computers with 64K bytes of memory. A video terminal with clear screen and cursor-addressing and 240K bytes of disk capacity are required. The suggested retail price is $295. For further details, contact Fox & Geller Inc., 604 Market, Elmwood Park, NJ 07407, (201) 794-8883.
Circle 564 on inquiry card.

Financial Forecasting Tool

Ashton-Tate's Bottom Line Strategist is an econometric forecasting tool. Developed to serve Fortune 1000 forecasting needs, this program generates bottom-line answers for future business ventures without programming, formulas, or complex spreadsheets. It provides complete, sophisticated models that assist executives in analyzing and tracking business scenarios. The Strategist uses direct user input of business assumptions and displays 11 different financial and marketing forecasts. Key considerations include how profitable a business will be, how much money is being risked, and when break-even points will be established.

The Bottom Line Strategist, designed for the IBM Personal Computer and CP/M-based systems, is available for $400 through Ashton-Tate dealers and distributors. Contact Ashton-Tate, 10150 West Jefferson Blvd., Culver City, CA 90230, (213) 204-5570.
Circle 565 on inquiry card.

Database Program for Nonprogrammers

Infostar is a database-management system that doesn't force you to learn a programming language. Produced by Micropro International, this business-applications development package provides onscreen English-language menus that guide you through each step of data-entry form design and report generation. For data entry, a cursor is used to draw forms on the screen. Generating custom applications is said to be four times faster than with other programs because you do not have to write and debug code.

Infostar can generate a preformatted quick report in approximately 60 seconds and has the ability to incorporate data from multiple files. It provides up to nine control breaks, arithmetic calculations within reports, and four levels of help menus. It can sort a file of up to 32 key fields at speeds approaching 560 records per minute, and its report writing and editing feature lets you move data fields, change headings, and insert dollar signs and decimal points. Able to work with dot-matrix or letter-quality printers, Infostar's print features include boldface and underlining of selected data fields. Other specifications include variable-length records and Wordstar compatibility.

Infostar runs on 48K-byte CP/M 2.2-based systems. Dual floppy-disk drives or a single floppy disk with a hard disk is recommended. With a training guide, Infostar costs $495. It's available from Micropro International Corp., 33 San Pablo Ave., San Rafael, CA 94903, (415) 499-1200.

Circle 566 on inquiry card.

Xenix Now Standard on TRS-80 Model 16

Radio Shack has announced that it will use Microsoft's multiuser, multitasking Xenix operating system as the standard DOS on its TRS-80 Model 16. A Model 16 equipped with Xenix can be expanded to accommodate three users, with all users running programs or sharing the same program, data, or peripherals.

Xenix features tree-structured directories, device-independent I/O, chaining of program input and output, and foreground and background execution. It requires 256K bytes of memory and a hard-disk drive. Xenix can also run on TRS-80 Model IIs outfitted with a hard disk and a Model 16 upgrade kit. All applications software currently offered by Radio Shack for the Model 16 can be moved to the Xenix system. Radio Shack will supply Xenix at no cost to Model 16 owners and include it in all new Model 16 production.

In a related development, Radio Shack also announced that it intends to introduce several multiuser application packages for Xenix-equipped Model 16s. Future plans call for several interactive accounting programs, a high-capacity inventory control system, versions of Microsoft's BASIC and Multiplan spreadsheet, and a Xenix development system that includes the C language.

For complete details, contact your local Radio Shack Computer Center, selected Radio Shack stores, and participating dealers. Radio Shack 1800 One Tandy Center, Fort Worth, TX 76102.

Circle 567 on inquiry card.

Appointments and Records Filed in Shoebox

Shoebox 2.0, an appointment manager and expense recording system from Techland Systems, can track tasks and appointments for any number of executives, limited only by storage capacity. It offers such features as a schedule-handler for tasks that are not appointments, expense recording keyed to particular appointments and categories, reminders for recurring schedule items, and the ability to produce printouts of schedules and expense reports. Using a minimum number of keystrokes, you can review past appointments or reminders involving a given subject or person. Shoebox has the ability to remind you of events up to six months ahead of time, and its multiuser option offers password-protection and a coordinator mode that allows nonsensitive data to be manipulated. Programming knowledge is not required because most Shoebox commands are single keystrokes.

Shoebox 2.0 runs on 50K-byte MS-DOS-based systems. A cursor-addressable terminal and one or more 160K-byte disk drives are required. An 80-character-per-line printer is recommended. Shoebox costs $195 and is available from Techland Systems Inc., 39 Carwall Ave., Mount Vernon, NY 10552, (914) 699-8467.

Circle 568 on inquiry card.

L. A. W. S. Support for Law Offices

L. A. W. S. (Litigation support, Accounting, Word processing System) software for law offices is available from Legal Systems Development. Litigation support modules range from a database that stores, manipulates, and retrieves depositions, transcripts, and evidence to a trial preparation program that provides a variety of summary reports. Accounting packages include accounts receivable and payable, billing, and payroll. Lexisoft's Spellbinder is available through Legal Systems Development. This word processor features letter-quality printer support, simple cursor moves, office and data management abilities, and an optional spelling checker. Other modules in the L. A. W. S. product line include a docket-con-

trol system and communications software.

The manufacturer recommends a computer system with 10 megabytes of disk storage, 64K bytes of RAM (random-access read/write memory), CP/M, a printer, and a terminal. Prices for individual modules range from $100 to $2495. The complete L. A. W .S. product line can be purchased for $5295. For full details, contact Legal Systems Development, 460 Main St., Placerville, CA 95667, (916) 626-3351.

Circle 569 on inquiry card.

PERIPHERALS



Matrix Printers from GE

The GE 3010 and 3014 are the latest additions to the General Electric GE 3000 series of dot-matrix printers. These microprocessor-based printers are plug-to-plug compatible with such microcomputers as Apple, IBM, and Televideo. They can print up to four copies bidirectionally at 160 cps (characters per second). Each 136-column printer is supplied with a 2K-byte print buffer, a 9-wire printhead for continuous underscoring and lowercase descenders, and selectable print densities and paper widths. Both machines print 6 or 8 lines per vertical inch.

The GE 3010 uses a 4-pin tractor for paper feeding, while the 3014 has a tractor and a friction cut-sheet roller arrangement. The 3014 also features a high-resolution print mode that produces overlapping dots for near-letter-quality printing at 40 cps and a horizontally enhanced 80-cps memo mode. A carbon-film ribbon is being developed for the 3014. Volume pricing ranges from $850 to $1150, depending upon model and quantity. Additional information is available from General Electric Co., Data Communication Products Department, Waynesboro, VA 22980, (800) 368-3182; in Virginia, (703) 949-1183.

Circle 570 on inquiry card.



Graphos: Desktop Graphics Terminal

Graphos, a desktop color graphics terminal that can display and manipulate 16 windows, is produced by Ithaca Intersystems. It features resolution of 640 by 480 pixels, two-dimensional segment transformations, high-level primitives, a Motorola MC68000-based device-independent graphics subsystem, multiple fonts, and individual scroll, pan, zoom, and graphics overlay for each window. Input support includes tablets, joysticks, and track balls. Standard alphanumeric support includes character and background color, insert and delete line, and VT-100 compatibility. Three I/O function modules can be incorporated into Graphos, providing a means for such interfaces as RS-232C, RS-422A, and 8- or 16-bit parallel.

The concept behind Graphos is known as Shiftable Cell. The Shiftable Cell, which combines alphanumeric and bit-mapping architecture, dynamically assigns cells to the 16 on-screen windows. It permits text and graphics scrolling under any fixed window and independent manipulation of any window. Segments are retained in the terminal's memory, enabling them to be rotated, recalled, or shifted without retransmission from the host computer.

A 9-slot card cage is available as an option. Graphos is priced at less than $8000. For further details, contact Ithaca Intersystems Inc., 1650 Hanshaw Rd., POB 91, Ithaca, NY 14850, (800) 847-2088; in New York, (607) 257-0190.

Circle 571 on inquiry card.

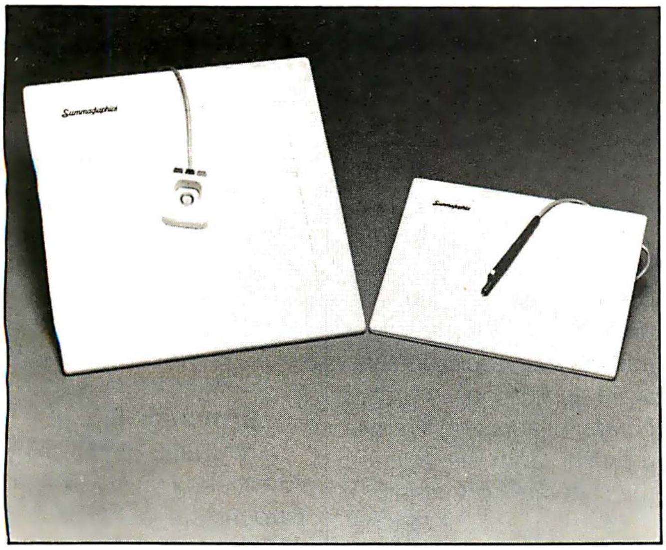
Disk Drive for Atari

The Percom Data AT-88 disk-drive system is compatible with Atari 400/800 computers. This single-density drive offers 88K bytes of formatted storage and features Atari plug compat-

ibility and an integral power supply. The AT-88 can use Atari operating system software without modification.

The AT-88 is shipped with the OSA/Plus operating system. It costs $488. For further information, contact Percom Data Co. Inc., 11220 Pagemill Rd., Dallas, TX 75243, (214) 340-7081.

Circle 572 on inquiry card.

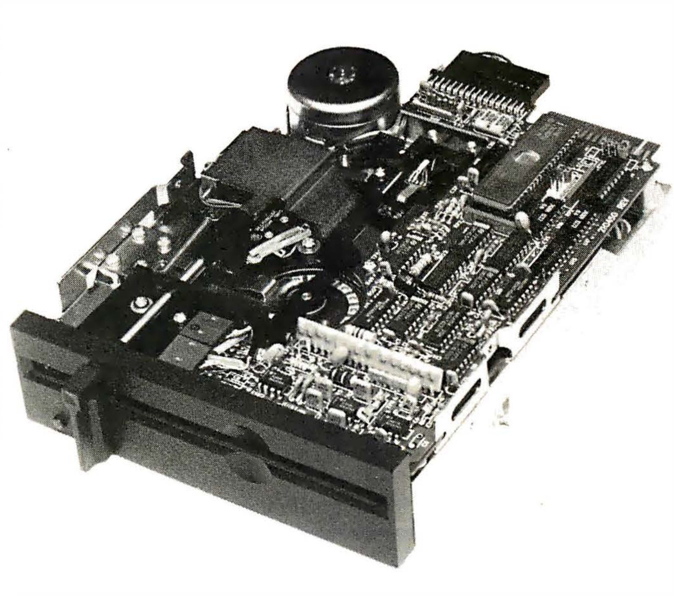


Compact Digitizers for OEM Market

Summagraphics has announced a family of compact, ergonometrically designed digitizers for the OEM (original equipment manufacturer) graphics systems market. The MM series will perform all cursor steering, menu picking, and graphics digitizing tasks. The digitizers can provide absolute and delta coordinate output and can automatically scale output both horizontally and vertically to match video-display resolution and orientation. Standard features include resolution of up to 500 lines per inch, single printed-circuit grid electronics, and built-in diagnostic modes to check electronics, communications, tablet, and stylus or cursor. A three-button cursor that can be used either as a mouse or as a digitizer cursor is supplied with this system. The stylus is equipped with a pen-tip switch and a user-assignable barrel activation button.

Interface options include either RS-232C or TTL (transistor-transistor logic) ports. The MM 960 digitizer has a 6- by 9-inch (152- by 228-mm) active area that provides 3000 by 4500 points of resolution. The MM 1200's active area measures 12 by 12 inches and offers 6000 by 6000 points of resolution. For detailed price and product information, contact Summagraphics Corp., 35 Brentwood Ave., POB 781, Fairfield, CT 06430, (203) 384-1344.

Circle 573 on inquiry card.



Half-Height Drives Handle Full Load

The storage capacity and performance of the Tandon TM55 Thinline family of half-height $5\frac{1}{4}$-inch floppy-disk drives are said to be equivalent to that of Tandon's full-sized drives. TM55 Thinline drives are $1\frac{5}{8}$ inches tall, $5\frac{3}{4}$ inches wide, and 8 inches long. They weigh 3 pounds. Standard features include maximum data storage of up to 1 megabyte, a 3-millisecond track-to-track access time, and a transfer rate of 250,000 bytes per second. An on-board microprocessor controls spindle speed, centers the media, positions the head for minimum hysteresis, and switches the write current for optimum recording quality. TM55 drives use IBM-formatted $5\frac{1}{4}$-inch floppy disks.

Two models are offered. The Thinline TM55-2, a double-sided 48-tpi (track-per-inch) drive, has a storage capacity of half a megabyte. The TM55-4 is a double-sided 96-tpi drive with 1 megabyte of storage. Prices begin at less than $200. Complete technical specifications are available from Tandon Corp., 20320 Prairie St., Chatsworth, CA 91311, (213) 993-6644.

Circle 574 on inquiry card.



Pint-Size Modem Fits Anywhere

Novation is marketing a 300-bit-per-second direct-connect automatic ans-

wer/originate modem that's almost one-fifth the size of conventional units. The J-Cat measures 5 by 1.9 by 1.3 inches, small enough to fit almost anywhere. It plugs into any modular RJ11C telephone jack and has the ability to automatically switch into answer or originate modes. J-Cat comes with an audio beep that sounds for busy signals, dial tones, and when a carrier is detected. Built-in features include LED (light-emitting diode) status displays, a disconnect/test key, a connect/break key, and self-test. J-Cat is RS-232C-compatible.

The suggested retail price for the J-Cat modem is $149. Address inquiries to Novation Inc., 18664 Oxnard St., Tarzana, CA 91356, (800) 423-5419; in California, (213) 996-5060.
Circle 575 on inquiry card.

PUBLICATIONS



Jameco Issues Catalog

Jameco Electronics has produced a 64-page illustrated catalog listing more than 2000 electronic products ranging from integrated circuits to power supplies. For a copy, contact Jameco Electronics, 1355 Shoreway Rd., Belmont, CA 94002, (415) 592-8097.
Circle 576 on inquiry card.

Software Guide

The Online Micro-Software Guide and Directory, 1983-84, is available from Online Inc., publisher of Database magazine. Edited by Helen A. Gordon, this guide contains full-page descriptions of software packages, resource information, an annotated bibliography, and listings of resources. To assist readers in locating programs for specific needs, four indices are provided: applications, software, producer, and distributor. Also included are nontechnical articles that address such topics as software applications in a corporate headquarters environment and the role of the software consultant.

Each copy of the Online Micro-Software Guide and Directory comes with an up-to-the-minute addendum that includes new benchmarks and less familiar programs. Single copies cost $40. Four or more copies are $30 each, including the annual supplements. Two annual supplements cost $30 each. Contact Online Inc., 11 Tannery Lane, Weston, CT 06883, (203) 227-8466.
Circle 577 on inquiry card.

Guide Aids Standards Developers

A FORTRAN coding guide that assists software departments in formulating standards has been produced by Associated Technology. This 46-page reference work is said to provide software managers, designers, and quality-assurance teams a methodology made up of a set of company standards and examples. The publisher asserts that these features ensure the construction of top-down programs that are structured, testable, and easily maintainable.

The FORTRAN guide costs $20. It's available from Associated Technology, Route 2, Box 448, Estill Springs, TN 37330.
Circle 578 on inquiry card.

Armchair BASIC

Armchair BASIC by Annie and David Fox is an introductory book on the BASIC programming language from Osborne/McGraw-Hill. It's written for computer neophytes who do not have access to microcomputers but who want to be familiar with programming concepts. This 180-page book presents programming fundamentals that are applicable to any computer that runs BASIC, such as the Apple or Commodore PET. Topics covered include the working parts of a computer, variables, data inputs, if . . . then statements, controlled loops, random numbers, and subroutines.

Armchair BASIC is available in paperback for $11.95. Contact Osborne/McGraw-Hill, 630 Bancroft Way, Berkeley, CA 94710, (415) 548-2805.
Circle 579 on inquiry card.

MISCELLANEOUS



Robot Recalls Its Actions

RB5X, an intelligent robot, detects and responds to objects in its path. Manufactured by RB Robot Corporation, RB5X has 8K bytes of memory, programs, and tactile sensors. The company asserts that once RB5X achieves a successful random response, it remembers its actions and repeats the correct response when confronted with the same situation again.

For program entry and data transfers, RB5X is supplied with an RS-232C port, making it compatible with such microcomputers as the Apple, Radio Shack TRS-80, and IBM Personal Computer. This port, for example, lets you transfer RB5X's memory to your computer, where you can study and alter its patterns and programs. RB5X is equipped with a circuit that automatically charges its batteries. Other standard features include a sonar sensor and a pulsating light. It has an aluminum body with polycarbonate dome and measures 13 by 24 inches. RB5X weighs 10 pounds and uses two rechargeable 6-volt gelled electrolyte batteries (supplied).

Options include 16K bytes of additional memory, data telemetry, and a mechanical arm. A voice-recognition system and a speech synthesizer are under development. The basic RB5X is $1495. Address all inquiries to RB Robot Corp., Suite 201, 14618 West Sixth Ave., Golden, CO 80401, (303) 279-5525.

Circle 580 on inquiry card.

Data Encryption Board

The Encryptor from Jones Futurex is a high-speed data encryption/decryption plug-in board. Practical applications include protecting financial statistics, market strategies, and technical and personal records. It has a transfer rate of 1.1 megabits per second and offers programmed I/O operation for key, data, commands, and states. The Encryptor is said to be able to encrypt or decrypt 8 bytes of data in less than 50 microseconds. No cables are required. The Encryptor provides supporting software for CP/M, MP/M, and Oasis operating systems and works with S-100, Apple, and IBM Personal Computers.

The Encryptor, model number ENC 300, uses the Western Digital Data Encryption/Decryption VLSI (very large-scale integration) device, as certified by the National Bureau of Standards. It costs $299.95 and is available from Jones Futurex Inc., Suite G, 9700 Fair Oaks Blvd., Fair Oaks, CA 95628, (916) 966-6836.

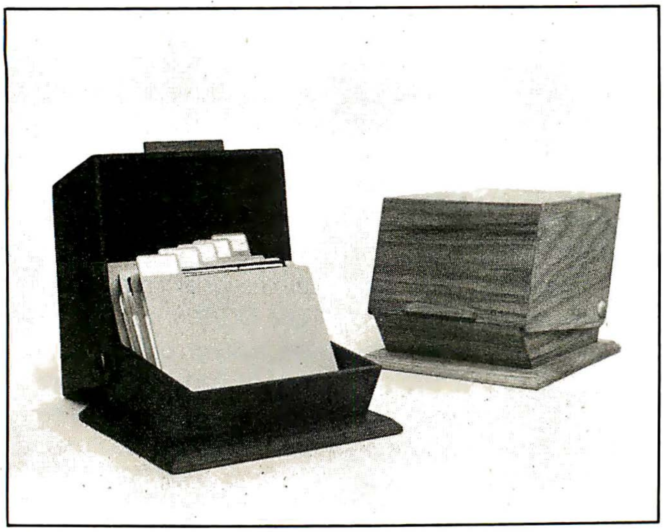
Circle 581 on inquiry card.

Intelligent Clocking Machine

Digitech's DC-999 is an intelligent clocking machine that can be controlled by any computer through an RS-232C port. It's suitable for applications involving time recording and card identification, such as security access and professional time tracking. The DC-999 responds to a set system of commands, and it can be reprogrammed for different applications. Standard features include a built-in microprocessor and memory and the ability to handle all front-end processing independently or to work as a stand-alone terminal. It's able to collect, check, edit, compute, store, and transfer data to a host computer. Data is collected through an optical card reader or through keyboard entry. The DC-999 has LED (light-emitting diode) displays for verifying data entry and a buzzer alarm that alerts the key operator of misuse or tampering.

A 15-column printer and a magnetic tape drive are offered as backup storage options. A 12-digit version with programmable digit length for job-costing and a keyboard option for entering external data relating to an incoming card number are also available. The suggested price is $1500; dealer inquiries are invited. Contact Digitech PTE Ltd., 303 Pearls Center, 100 Eu Tong Sen St., Singapore 0105, Republic of Singapore; tel: 2237740; Telex: RS28171 DGTECH. In the U.S., contact Hiram H. Samuel, Onondaga International, (315) 471-1251.

Circle 582 on inquiry card.

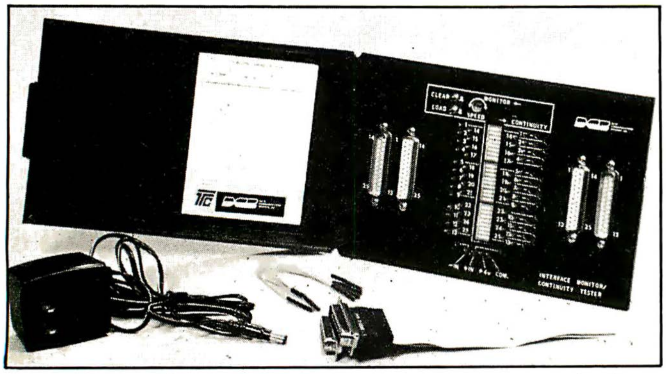


Hardwood Disk Storage Box

Systems Integration's Disk Niche is a solid hardwood storage box for 5¼-inch floppy disks. It provides a dust-proof, static-free environment for as many as 50 floppy disks and has 5 movable, tabbed dividers to aid organization.

The Disk Niche is available in walnut, cherry, or oak, with a hand-rubbed oil finish. It costs $49.95, plus $3 postage and handling. Contact Systems Integration, 1519 North Nevada Ave., Colorado Springs, CO 80907, (303) 635-4477.

Circle 583 on inquiry card.



Cable Tester Doubles As Breakout Box

The CT-1 Cable Tester and Breakout Box lets your technicians test RS-232C cables on-site. Made by Data Communications Brokers, the CT-1 checks for cable continuity and indicates leads that are tied together or crossed over. A speed adjustment for setting the rate for cable tester scans and an LED (light-emitting diode) for each of the RS-232C's 25 connections are provided. The CT-1 can be placed into an RS-232C link and used as a breakout box by flipping a switch.

The CT-1 comes with jumpers, a short extension cable, rechargeable batteries, and a battery charger. It costs $255 and can be purchased directly from Data Communications Brokers, 3000 Research Rd., POB 3658, Champaign, IL 61820, (800) 637-1127; in Illinois, (217) 352-3207.

Circle 585 on inquiry card.

Compact Disk Has Large Disk Abilities

The CFD (compact floppy disk) is a 3-inch floppy disk from Maxell Corporation of America. The CFD's rotation speed, data transfer rate, recording capacity per track, and other technical specifications are identical to those of 5¼-inch floppy disks. The CFD has a high-recording-density magnetic coating with the same capacity as that of a standard disk, which lets you transfer all the data from a 5¼-inch disk to it. The magnetic coating features a hardened plastic center for improved reliability.

The CFD, which was released late last month, is designed to work with such 3-inch disk drives as the one manufactured by Hitachi. Each CFD costs approximately $6.50. Further information is available from Maxell Corporation of America, Computer Products Division, 60 Oxford Dr., Moonachie, NJ 07074.

Circle 584 on inquiry card.

Slot-Independent Bubble Memory for the Apple II

Ap-Bub, a slot-independent 128K-byte nonvolatile bubble-memory module for the Apple II, is marketed by MPC Peripherals Corporation. Standard features include disk-emulation software for DOS 3.3 and a boot PROM (programmable read-only memory) that permits the user to boot directly from the module. Ap-Bub is said to be able to execute DOS read and write commands at speeds three times faster than the standard floppy-disk drive. Its data reliability is purported to be 1000 times greater than that of tapes and disks.

Ap-Bub has an $875 suggested retail price. For more information, contact MPC Peripherals Corp., 9424 Chesapeake Dr., San Diego, CA 92123, (619) 278-0630.

Circle 586 on inquiry card.

Where Do New Products Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. The information is printed more or less as a *first-in first-out queue*, subject to occasional priority modifications. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

Circle 114 on inquiry card.

DISK DRIVE For APPLE!!

→ metal cabinet ☆ ☆
→ 35 track $279.95
→ w/cable

Computer Games:
APPLE & ATARI (specify)

Choplifter
Frogger → **$24.95ea.**

Apple Panic
Crossfire
Raster Blaster → **$21.95ea.**

SUPER 3.5amp POWER SUPPLY
for APPLE → $95.00 ☆

Diskette Storage BOX

5¼in. 5/ $2.50ea. $10.00 : 8in. 5/ $3.50 $15.00

Bare Bones APPLE II EURO

=48K RAM=

w/o Keyboard

w/o Pwr. Supply

$399.

Microswitch Keyboard	Power Supply w/ Purchase	APPLE Reference Manl.
$ 75.00	$ 89.00	$18.00

☆SPECIALS☆

3inch Mini FAN → $8.95
2111 → $2.45
8155 → $11.50
ER2501 → $4.95
AY5 1013A → $2.95
8202 → $29.95
6522 → $5.25
8255 → $4.50
8748-8 → $31.00
MC6800 → $7.75
MC6802 → $14.95
MC6850 → $4.50
MC6821 → $4.95
6331 → $1.25

4116-2 → 8/9.95
2716(5v) → 3.25ea
2732(5v) → 5.25ea
2532(5v) → 8.75ea.
Z80 A CPU → 5.25ea.

I.C. Master (2vol.)
$49.95

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50 - 99	- 4.00	500 - 999	- 11.00	for
100 - 240	- 8.00	1000 - UP	- Call	catalog

MONITORS ☆ ☆

ZENITH # ZVM-121

12in. 15MHz./GREEN Phos
→ $99.00☆

BMC # BM-1200SU

12in. 18 MHz./GREEN Phos.
Non-Glare Screen
→ $118.00☆

BMC # BM1401RGB

13in. "RGB" COLOR
with Apple interface!!
→ $425.00☆

Diskette SALE!!

"Wabash"

call for Qty. Price

	5¼	8inch
SS/SD soft	18.50	21.50
SS/DD	27.40	30.40
DS/SD	ø	34.90
DS/DD	32.40	37.40

REAL-TIME CLOCK CALENDAR (MSM 5832)
$6.25 / $1.25 xtal.

Syntron II Computer
★ 48K RAM
★ Runs Apple Software

$699.00

74LS00	.24
74LS02	.24
74LS03	.24
74LS04	.24
74LS05	.24
74LS06	.30
74LS08	.28
74LS10	.24
74LS11	.33
74LS12	.33
74LS13	.45
74LS14	.89
74LS20	.24
74LS21	.24
74LS26	.30
74LS27	.28
74LS28	.32
74LS30	.24
74LS32	.32
74LS37	.50
74LS38	.32
74LS42	.50
74LS48	.70
74LS51	.24
74LS55	.35
74LS74	.35
74LS75	.48
74LS83	.70
74LS86	.38
74LS90	.60
74LS91	.85
74LS92	.65
74LS93	.60
74LS95	.80
74LS107	.38
74LS109	.38
74LS112	.40
74LS113	.40
74LS114	.45
74LS122	.40
74LS123	.85
74LS125	.90
74LS126	.85
74LS132	.70
74LS136	.50
74LS138	.65
74LS139	.65
74LS145	1.10
74LS151	.70
74LS153	.70
74LS157	.70
74LS158	.70
74LS161	.85
74LS162	.85
74LS163	.85
74LS164	.85
74LS165	.85
74LS169	1.55
74LS170	1.55
74LS174	.85
74LS175	.85
74LS190	.90
74LS191	.90
74LS221	1.10
74LS240	.95
74LS241	.95
74LS244	.85
74LS245	1.65
74LS248	1.00
74LS249	.90
74LS251	1.20
74LS253	.80
74LS257	.80
74LS258	.80
74LS259	1.25
74LS260	.60
74LS273	1.50
74LS275	3.00
74LS279	.50
74LS283	.75
74LS373	.90
74LS374	1.50
74LS377	1.40

COMPONENTS

7400 SERIES

7400	.18	7454	.19
7402	.18	7470	.30
7404	.18	7472	.25
7405	.21	7474	.30
7406	.23	7475	.40
7409	.18	7476	.30
7410	.18	7480	.55
7411	.22	7481	1.00
7412	.28	7489	3.00
7413	.32	7490	.30
7414	.45	7491	.35
7416	.24	7492	.45
7417	.24	7494	.60
7420	.18	7495	.50
7421	.30	74100	.90
7425	.25	74107	.25
7427	.25	74122	.40
7430	.18	74125	.40
7432	.25	74144	2.50
7438	.25	74145	.50
7440	.18	74148	1.00
7441	.45	74154	1.00
7443	.60	74157	.45
7444	.60	74160	.60
7445	.60	74161	.60
7447	.60	74166	.90
7448	.60	74174	.80
7450	.18	74181	1.80
7451	.18	74390	1.00
7453	.19		

74S SERIES

74S00	35
74S02	38
74S03	38
74S04	45
74S05	65
74S08	40
74S10	55
74S15	55
74S20	55
74S22	75
74S30	35
74S37	1 25
74S51	60
74S65	95
74S74	55
74S85	2 00
74S86	1 10
74S112	1 45
74S132	1 10
74S138	95
74S140	1 25
74S158	1 25
74S174	95
74S175	95
74S181	4 00
74S182	2 75
74S188	3 50
74S240	3 50
74S244	3 50
74S471	9 50
74S472	15 00

STATIC RAMS

2111	2 85	8/2 50ea
2112	2 85	8/2 50ea
2114	2 00	8/14 00
2114L 200NS	2 25	4/2 00ea
HM6116 150NS	8 25	

DYNAMIC RAMS

4027	2 00	8/1 75ea
4116 200ns	1 50	
4164 200ns	7.95	

MISC

8T26	1 20
8T28	1 20
8038	2 75
8080A	3 75
8155	10 50
8255	4.50
MC1330	1 45
MC1350	1 10
MC1358	1 35
MC1458	55
LM380	1.10
LM386	1.40
LM565	95
LM741	25
LM1310	2.90

EPROMS

1702	4 25	8/3 95 ea
2708	3 25	8/2 99 ea
2716(5V)	395	8/3 65 ea
TMS2716	8 95	8/8 00ea
2732(5V)	8 95	8/7 75 ea
TMS2532	11 50	8/10 25ea

VOLTAGE REGULATORS

7805, 7806, 7808, 7812, 7818, 7905, 7908, 7912, 7918 — 85

MORE MISC

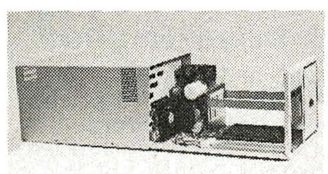
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8216	1 80
1103A	95
N82S185	8 95
AY5 1013A	3 00
1488	95
1489	95
MC6802	9 95
MC6821P	4 95
MC6850P	3 25

CPU S

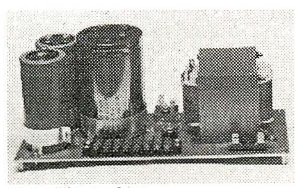
Z80	8 50
Z80A	6 00
Z80A PIO	6 00
6502	6 00
6502A	12 00
8085A	8 50
MC6800	7 75

SUNNY LOW LOW COST

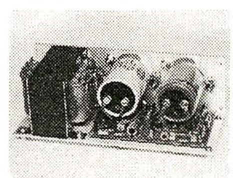
POWER SUPPLIES
(LINEAR & SWITCHING) FOR S-100, DISK DRIVES



No. 806 & No. 516 Mainframes



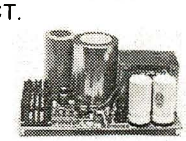
Kit 1, 2 & 3 for S-100



R_2, R_3 for 2 Drives (Floppy & Hard)

S-100 & DISK POWER SUPPLIES: OPEN FRAME, ASSY. & TESTED, 6 OUTPUTS, ADJU. & FUSES PROTECT.

ITEM		+5V OVP	−5V	+24V(OR +12V)	+8V	±16V	SIZE W x D x H	PRICE
S_3	12 SLOT & 2 FLOPPY (1 Floppy & 1 Hard Disk)	5A	1A	5-7A PEAK	13A	3A	10" x 6" x 5"	102.95
S_4	6 SLOT & 2 FLOPPY	4A	1A	4-5A PEAK	8A	3A	8⅜" x 5" x 4¾"	92.95



S_3, S_4 for S-100 & 2 Drives

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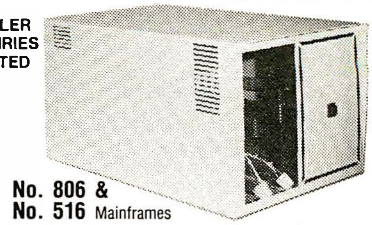
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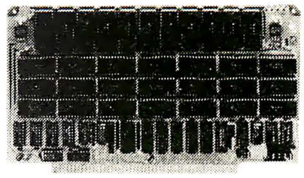
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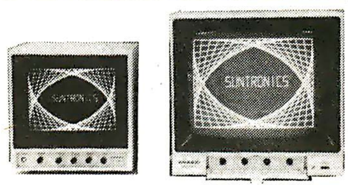
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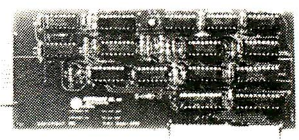
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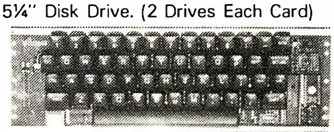
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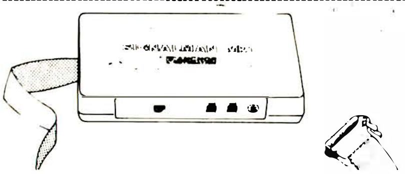
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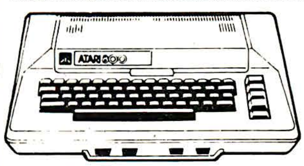
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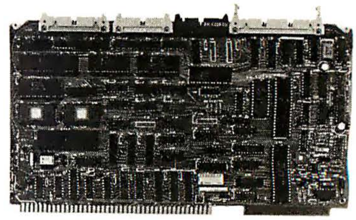
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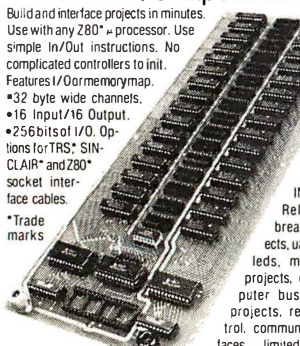
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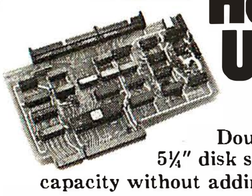
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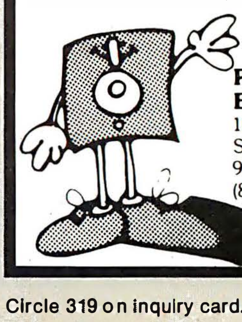
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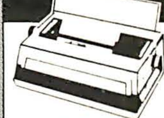
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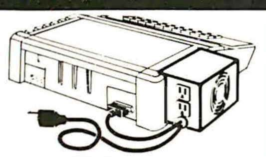
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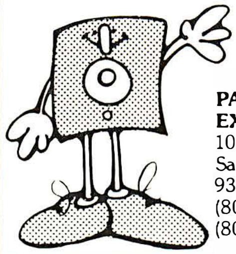
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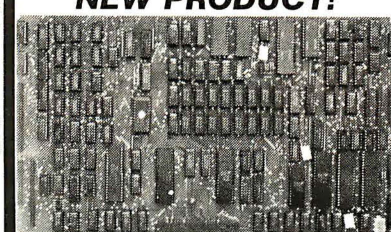
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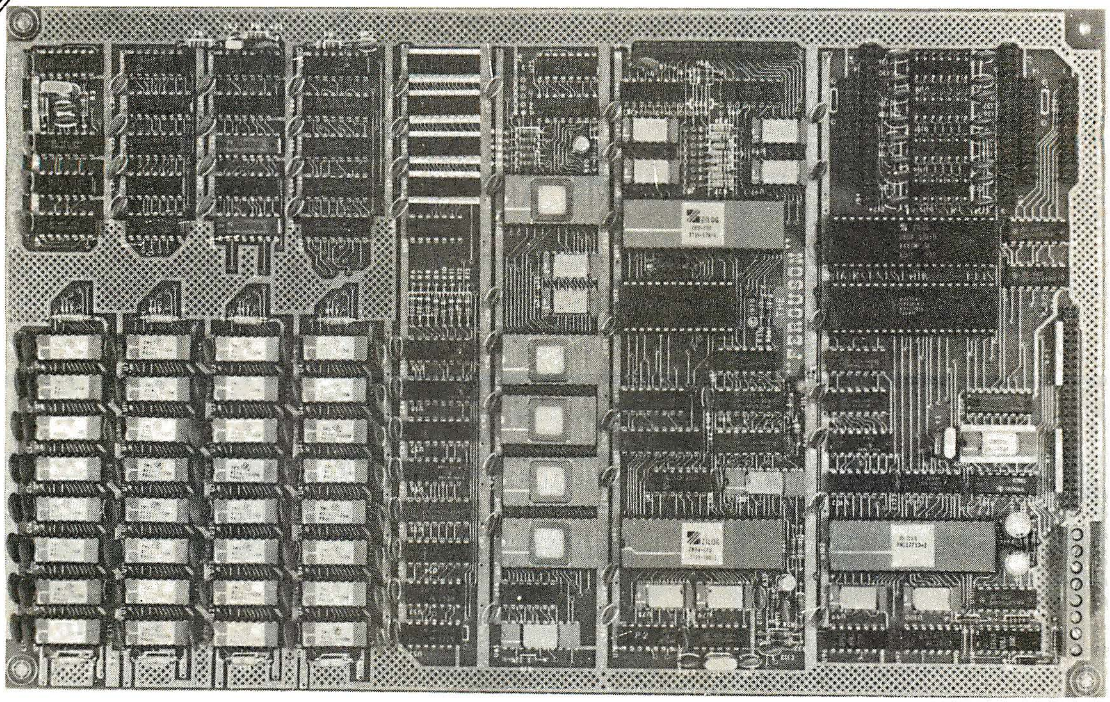
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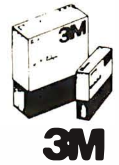
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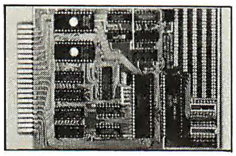
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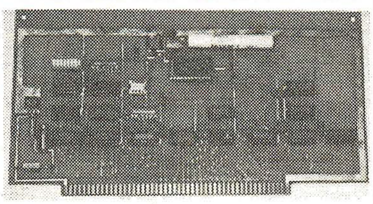
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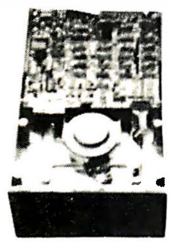
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Sincerely,

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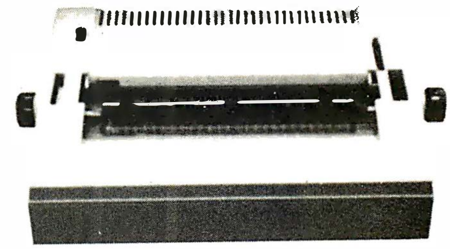
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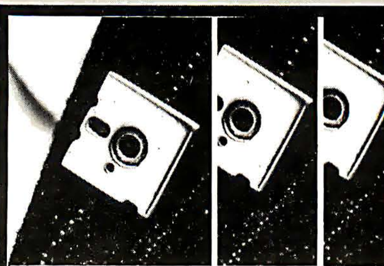
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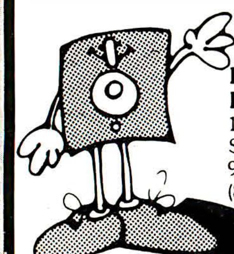
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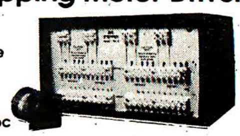
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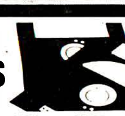
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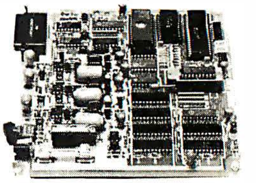
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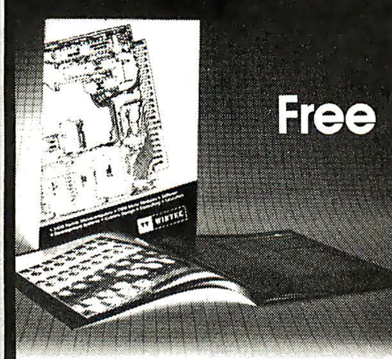
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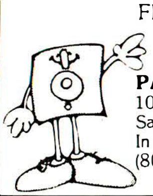
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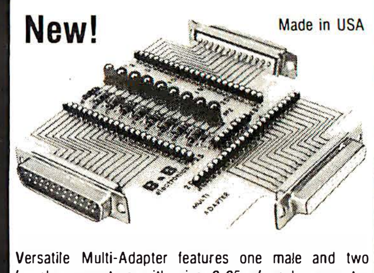
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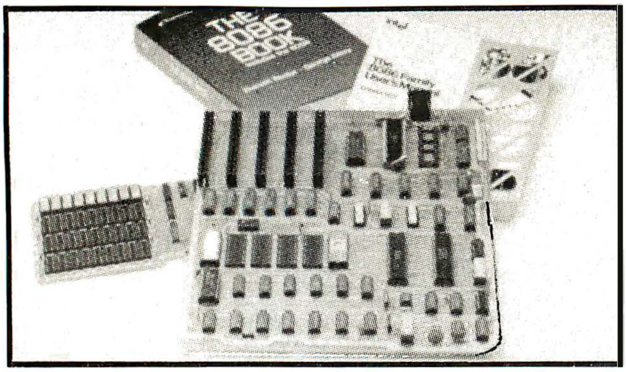
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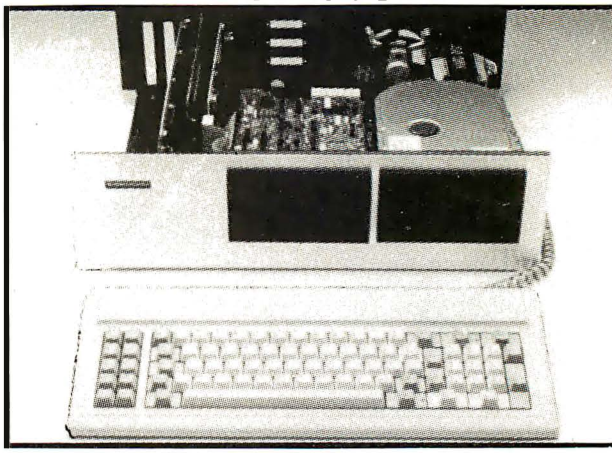
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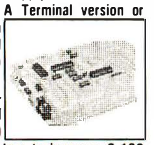
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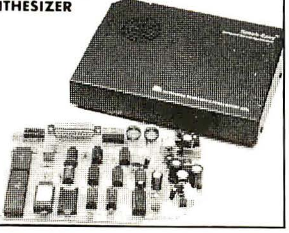
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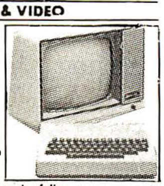


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SMARTERM 80 ☐ 299.95 + 3.00 p&i. Display format: specify either 80 by 24 or 40 by 16...128 ASCII characters (u&l case)...8 baud rates: 110 to 19,200...line output: RS232/C or 20 ma current loop...video output: 1V P/P...editing features: insert/delete line, insert/delete character, forward/back tab...line or page transmit...page print function...cursor positioning: up, down, right, left, plus absolute cursor positioning with read back... visual attributes: underline, blink, reverse video, half intensity & blank...graphics: 12,000 pixel resolution block plus line graphics...on-screen parity indicator... parity: off, even or odd...stop bits: 110 baud 2, all others 1...printer output...60 or 50 Hz vertical refresh...blinking block cursor...2k on-board RAM... ASCII encoded keyboard: 56 keys, 128 characters... 4k on-board ROM...complete with power supply & cabinet.

☐ SMARTERM VIDEO BOARD: 199.95 + 3.00 p&i
☐ ZENITH VIDEO MONITOR (green phosphor): 149.95 + 6.00 p&i ☐ RF MODULATOR (kit only): 8.95 + 1.00 p&i ☐ 3-ft. cable with DB 25 connectors: 14.95 + 2.00 p&i

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HI-RES 12" GREEN SCREEN - Zenith

15 MHz bandwith 700 lines/inch, P31 green phosphor, switchable 40 or 80 columns, small, light-weight & portable.

VDM-201201 *List price $189.95* ________ **$115.95**

HI-RES GREEN MONITORS - NEC

20 MHz bandwidth, P31 phosphor ultra-high resolution video monitor, high quality, extremely reliable.

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18 MHz high resolution RGB color monitors fully compatible with Apple II and IBM PC, unlimited colors available.

VDC-821210 *RGBvision I, 380 lines* ________ **$389.95**
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Reasonably priced color video monitors.

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Single board, standard size S-100 computer system, 4 MHz Z-80A, single or double density disk controller for 5¼" or 8" drives. 64K RAM, extended addressing, up to 4K of EPROM, 2 serial & 2 parallel I/O ports, real time interrupt clock, CP/M compatible.

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Disk Sub-Systems - Jade

Handsome metal cabinet with proportionally balanced air flow system, rugged dual drive power supply, power cable kit, power switch, line cord, fuse holder, cooling fan, never-mar rubber feet, all necessary hardware to mount 2-8" disk drives, power supply, and fan, does not include signal cable.

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END-000421 *Cabinet kit* ________ **$199.95**
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Handsome vertical cabinet with scratch resistant baked enamel finish, proportionally balanced air flowsystem, quiet cooling fan, rugged dual drive power supply, power cables, power switch, line cord, fuse holder, cooling fan, all necessary hardware to mount 2-8" slimline disk drives, does not include signal cable.

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END-000820 *Bare cabinet* ________ **$59.95**
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Dual 8" Slimline Sub-Systems

END-000823 *Kit w/2 TM848-1* ________ **$919.95**
END-000824 *A & T w/2 TM848-1* ________ **$949.95**
END-000833 *Kit w/2 TM848-2* ________ **$1149.95**
END-000834 *A & T w/2 TM848-2* ________ **$1179.95**

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Tandon TM100-1 *single-sided double-density 48 TPI*
MSM-551001 ________ $219.95 ea 2 for **$199.95 ea**

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MSM-104550 ________ $349.95 ea 2 for **$329.95 ea**

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MSM-104650 ________ $399.95 ea 2 for **$379.95 ea**

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MSM-551002 ________ $294.95 ea 2 for **$269.95 ea**

Shugart SA450 *double-sided double-density 35 track*
MSM-104500 ________ $349.95 ea 2 for **$329.95 ea**

Tandon TM100-3 *single-sided double-density 96 TPI*
MSM-551003 ________ $294.95 ea 2 for **$269.95 ea**

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MSM-551004 ________ $394.95 ea 2 for **$374.95 ea**

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END-000216 *Single cab w/power supply* ________ **$69.95**
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PB-1 - SSM Microcomputer

2708, 2716 EPROM board with on-board programmer.

MEM-99510K *Kit with manual* ________ **$154.95**
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Microline 84 *132/232 column, Hi-speed 200 CPS, full dot graphics built in, plus all the features of the 83A.*

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New 40 CPS daisy wheel printer with full 15" carriage, uses standard Diablo print wheels and ribbons, both parallel and serial interfaces included.

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Silent, simple, and on sale - a better motherboard

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MBS-121A *A & T* ________ **$109.95**

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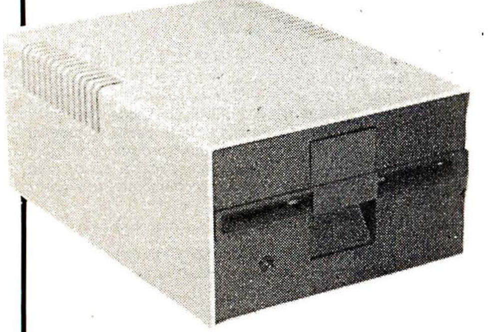
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Expand your Apple II to 64K, use as language card, full 1 year warranty. Why spend $175.00 ?

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Two computers in one, Z-80 & 6502, more than doubles the power and potential of your Apple, includes Z-80 CPU card CP/M 2.2 and complete manual set, Pascal compatible, utilities are menu-driven, one year warranty.

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80 column x 24 line video card for Apple II, addressable 25th status line, normal/inverse or high/low video, 128 ASCII characters, upper and lower case, 7 x 9 dot matrix with true descenders, standard Data Media terminal control codes, CP/M Pascal & Fortran compatible, 50/60 Hz, 40/80 column selection from keyboard.

IOV-2500A	*ALS Smarterm II*	**$169.95**

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CPX-62810A	*A.L.S. CP/M Card*	**$349.95**

2 MEGABYTES for Apple II

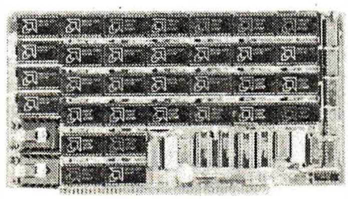
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MEM-99152K	*Kit less RAM*	**$99.95**
MEM-32152K	*32K kit*	**$199.95**
MEM-56152K	*56K kit*	**$289.95**
MEM-64152K	*64K kit*	**$299.95**
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256 RAMDISK - SD Systems

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MEM-65256A	*256K A & T*	**$774.95**
SFC-55009000F	*RAMDISK sftwr CP/M 2.2*	**$44.95**
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IEEE S-100, supports front panels, bank select, fail-safe refresh 4MHz, extended addressing, list price $575.00 - less than half price!!!

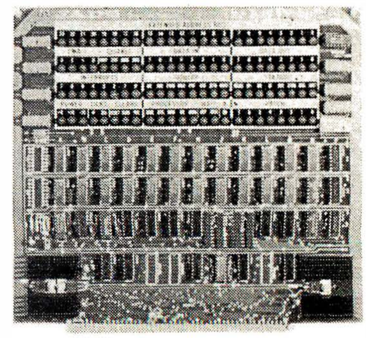
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Ultra-high-resolution 512 x 480, 256 color or black & white S-100 video board

IOV-1500A	*A & T*	**$799.95**



S-100 I/O BOARDS

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Inexpensive S-100 Diagnostic Analyzer

So your computer is down. And you don't have an oscilloscope. And you don't have a front panel... You're not alone - most computers have their occasional bad days. But without diagnostic equipment such as an oscilloscope (expensive!) or a front panel (expensive!), it can be very difficult to pinpoint the problem. Even if you have an extender board with a superfast logic probe, you can't see more than one signal at a time. You're stuck, right?

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TSX-200B	*Bare board*	**$59.95**
TSX-200K	*Kit*	**129.95**
TSX-200A	*A & T*	**$159.95**

I/O-4 - SSM Microcomputer

2 serial I/O ports plus 2 parallel I/O ports.

IOI-1010B	*Bare board w/manual*	**$35.95**
IOI-1010K	*Kit with Manual*	**$179.95**
IOI-1010A	*A & T*	**$249.95**

I/O-5 - SSM Microcomputer

Two serial & 3 parallel I/O ports, 110-19.2K Baud

IOI-1015A	*A & T*	**$289.95**

INTERFACER 4 - CompuPro

3 serial, 1 parallel, 1 Centronics parallel.

IOI-1840A	*A & T*	**$314.95**
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SBC-200 - SD Systems
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CPC-30200A *A & T* ______ **$329.95**

THE BIG Z - Jade
2 or 4 MHz switchable Z-80 CPU board with serial I/O, accomodates 2708, 2716, or 2732 EPROM, baud rates from 75 to 9600.
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CPU-30201A *A & T with Manual* ______ **$199.95**

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2 or 4 MHz Z-80 CPU with serial I/O port & on board monitor PROM, front panel compatible.
CPU-30400A *A & T with PROM* ______ **$289.95**

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2/4 MHz Z80A CPU, 24 bit addressing.
CPU-30500A *2/4 MHz A & T* ______ **$279.95**
CPU-30500C *3/6 MHz CSC* ______ **$374.95**

8085/8088 - CompuPro
Both 8 & 16 bit CPUs, standard 8 bit S-100 bus, up to 8 MHz, accesses 16 Megabytes of memory.
CPU-20510A *6 MHz A & T* ______ **$398.95**
CPU-20510C *6/8 MHz CSC* ______ **$497.95**

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MSF-201120 ______ *$274.95 ea* 2 for **$249.95 ea**

Shugart SA810 *half-size single-sided double-density*
MSF-108100 ______ $424.95 ea 2 for **$394.95 ea**

Shugart SA860 *half-size double-sided double-density*
MSF-108600 ______ $574.95 ea 2 for **$549.95 ea**

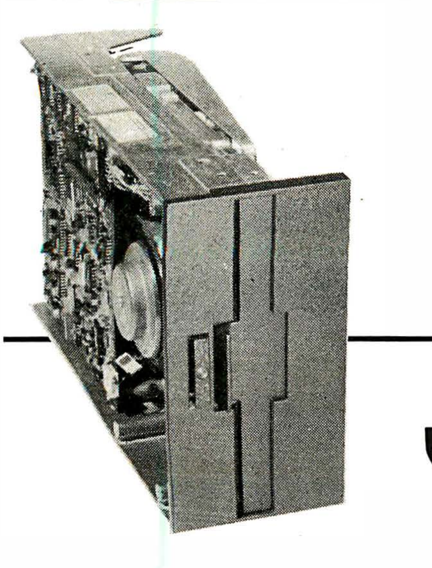
Shugart SA801R *single-sided double-density*
MSF-10801R ______ $394.95 ea 2 for **$389.95 ea**

Shugart SA851R *double-sided double-density*
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Tandon TM848-1 *single-sided double-den thin-line*
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Tandon TM848-2 *double-sided double-den thin-line*
MSF-558482 ______ $494.95 ea 2 for **$484.95 ea**

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IOM-5630A *300 baud for IBM PC* ______ *$269.95*
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1200 and 300 baud, all the features of the standard Smartmodem plus 1200 baud, 212 compatible, full or half duplex.
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SMARTMODEM - Hayes
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IOM-2010A *Micromodem II w/Term prgm* ______ **$329.95**
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IOM-1100A *Micromodem 100* ______ **$368.95**

1200 BAUD SMART CAT - Novaton
103/212 Smart Cat & 103 Smart Cat, 1200 & 300 baud, built-in dialer, auto re-dial if busy, auto answer/disconnect, direct connect, LED readout displays mode, analog/digital loop-back self tests, usable with multi-line phones.
IOM-5241A *300 baud 103 Smart Cat* ______ **$229.95**
IOM-5251A *1200 baud 212/103 Smart Cat* ______ **$549.95**
IOM-5261A *300 baud 103 J-Cat* ______ **$129.95**

J-CAT™ MODEM - Novation
1/5 the size of ordinary modems, Bell 103, manual or auto-answer, automatic answer/originate, direct conect, built-in self-test, two LED's and audio "beeps" provide complete status information.
IOM-5261A *Novation* ______ **$149.95**

S-100 DISK CONTROLLERS

DISK 1 - CompuPro
8" or 5¼" DMA disk controller, single or double density, single or double sided, 10 MHz.
IOD-1810A *A & T* ______ **$449.95**
IOD-1810C *CSC* ______ **$554.95**

VERSAFLOPPY II - SD Systems
Double density disk controller for any combination of 5¼" and 8" single or double sided, analog phase-locked loop data separator, vectored interrupts, CP/M 2.2 & Oasis compatible, control/diagnostic software PROM included.
IOD-1160A *A & T with PROM* ______ **$359.95**
SFC-55009047F *CP/M 3.0 with VF II* ______ **$99.95**

2242 DISK CONTROLLER - C.C.S.
5¼" or 8" double density disk controller with on-board boot loader ROM, free CP/M 2.2 & manual set.
IOD-1300A *A & T with CP/M 2.2* ______ **$399.95**

DOUBLE D - Jade
High reliablity double density disk controller with on-board Z-80A, auxiliary printer port, IEEE S-100, can function in multi-user interrupt driven bus.
IOD-1200B *Bare board & hdwr man* ______ **$59.95**
IOD-1200K *Kit w/hdwr & sftwr man* ______ **$299.95**
IOD-1200A *A & T w/hdwr & sftwr man* ______ **$325.95**
SFC-59002001f *CP/M 2.2 with Double D* ______ **$99.95**

NEW! CP/M PLUS 3.0

CP/M 3.0 is Digital Research's latest version of the industry standard disk operating system. It features many performance improvements such as intelligent record buffering, improved directory handling, "HELP" facility, time/date stamping of files and many more improvements. AND A TREMENDOUS INCREASE IN SPEED !!!, it is fully CP/M 2.2 compatible and requires no changes to your existing application software. Available only to Versafloppy II owners with SBC-200 CPU's

- ***CP/M 2.2 compatible***
- ***Easily customized***
- ***Easier to learn and use***
- ***High performance file system***
- ***Automatic disk log-in of removable media***
- ***Support for 1 to 16 banks of RAM***
- ***Supports up to 16 drives of 512 Megabytes each***
- ***Up to ten times faster than CP/M 2.2***
- ***Console I/O re-direction***
- ***Easy to use system utilities with HELP facility***
- ***Power batch facility***
- ***Designed for application programmers***
- ***Resident system extensions***

SFC-55009057F *CP/M 3.0 8" with manuals* ______ **$200.00**
SFC-55009057M *CP/M 3.0 Manual* ______ **$30.00**

THREE BOARD SET — SD Systems

FREE CP/M 3.0

Save $800.00

S-100 board set with 4 MHz Z-80A, 64K of RAM expandable to 256K, serial and parallel I/O ports, double-density disk controller for 5¼" and 8" disk drives, new and improved CP/M 3.0 manual set, system monitor, control and diagnostic software. Includes SD Systems SBC-200, 64K ExpandoRAM III, Versafloppy II, and FREE CP/M 3.0 - all boards are assembled & tested.

* **64K Board Set with FREE CP/M 3.0** ______ **$1195.00**
256K Board Set with FREE CP/M 3.0 ______ **$1395.00**

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SCOTCH	744D-0	744D-10	744D-16	26.50
MEMOREX	3481	3483	3485	26.50
VERBATIM	525-01	525-10	NA	26.50
MAXELL	MD1	MH1-10	MH1-16	29.85
DYSAN	104/1D	107/1D	NA	45.00

Double Side Double Density

SCOTCH	745-0	745-10	745-16	42.50
VERBATIM	550-01	550-10	NA	42.50
MAXELL	MD2-D	MH2-10D	MH2-16D	45.00
DYSAN	104/2D	107/2D	NA	49.50
DYSAN 96	204/2D	NA	NA	59.50

EIGHT INCH DISKETTES

Single Side Single Density

SCOTCH	740-0	29.50
MEMOREX	3060	29.50
DYSAN	3740/1	39.50

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SCOTCH	740-32	29.50

Single Side Double Density

SCOTCH	741-0	39.00
MEMOREX	3090	35.00
DYSAN	3740/D	57.50

Double side Double Density

SCOTCH	743-0	47.50
MEMOREX	3114	39.50
DYSAN	3740/2D	65.00

Scotch Head Cleaning Kits 5¼ & 8" $24.95
Plastic Library Cases 5¼ & 8" 2.95
Diskette Flip Tubs fifty diskettes 5¼"
Diskette Flip Tubs fifty diskettes 8"

Microswitch ASCII KEYBOARD $79



Each keyboard contains 81 high reliability Hall Effect keys. Outputs seven bit parallel ASCII MIC-81SD5 3 Lbs.



HITEK KEYBOARD $24.95

This Hitek keyboard is the same unit used by Lear Siegler in their middle line CRT terminals. The keyboard features 58 unencoded metal on metal contacts (HIK-58). Matching numeric cluster with 15 keys is available for $9.95 (HIK-15). Buy both of these units for only $29.90 and save $5.00 (HIK-5815)

MEMORY

16K DYNAMIC **1.95** 4116 150ns.	2732 EPROM **4.95** 450ns.
64K DYNAMIC **6.95** 4164 150ns.	16K STATIC **4.95** 6116 200ns.



2764 EPROM SALE $9.95

DYNAMIC MEMORY

		1-31	32+	100+
4027 4K dynamic 250ns	ICM-4027250	1.99	1.85	1.75
4116 150ns. 16K	ICM-4116150	1.95	1.85	1.75
4116 200ns. 16K	ICM-4116200	1.75	1.65	1.50
4164 150ns. 64K 128 refresh	ICM-4164150	6.95	6.50	5.90
41256 150ns. 256K	ICM-41256150	Available March83		

STATIC MEMORY

21L02 200ns. 1K static	ICM-21L02200	1.49	1.29	1.15
21L02 450ns. 1K static	ICM-21L02450	1.29	1.15	99
2112 450ns. 2K static	ICM-2112450	2.99	2.85	2.75
2114 300ns 1K x 4	ICM-2114300	1.95	1.85	1.75
4044TMS 450ns. 4K x 1	ICM-4044450	3.49	3.25	2.99
5257 300ns. 4K x 1	ICM-5257300	2.50	2.25	1.99
6116 P4 200ns. 2K x 8	ICM-6116200	4.95	4.80	4.65
6116 P3 150ns. 2K x 8	ICM-6116150	5.95	5.75	5.60
6167/2167 100ns 16K x 1 (20pin)	ICM-6167100	8.95	8.50	7.90

EPROMS

2708 450ns. 1K x 8	ICE-2708	4.95	4.75	4.55
2716 450ns. 2K x 8	ICE-2716	4.95	4.75	4.55
2716TMS 450ns. Tri-voltage	ICE-2716TMS	7.95	7.65	7.25
2732 450ns. 4K x 8	ICE-2732	4.95	4.75	4.55
2732 350ns. 4K x 8	ICE-2732350	8.50	8.00	7.60
2532 450ns. 4K x 8	ICE-2532	10.50	9.90	9.5[illegible]
2764 350ns. 8K x 8	ICE-2764	10.95	10.50	9.95
27128 350ns. 16K x 8	ICE-27128	Available March83		

CONNECTORS



S-100 Gold $2.95

DB25P



$2.50

GOLD EDGE CONNECTORS

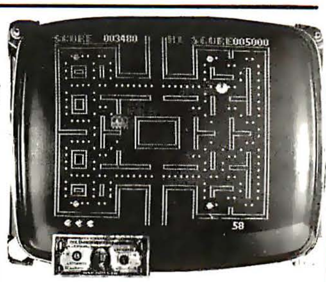
S-100 .125" centers	each	10+
Imsai solder .250" row	$2.95	$2.50
Imsai wire wrap (TI)	3.95	3.50
Sullins Hi-Rel. .250"	4.50	4.00
Sullins Hi-Rel. W/W	5.35	4.90
Sullins / Altair .140"	4.95	4.50
.156" Centers (standard)		
22/44 Kim Eyelet	2.50	2.15
36/72 Digital Group S/T	5.95	5.50
36/72 Digital Group W/W	6.60	6.15
43/86 Motorola 6800 S/T	6.60	6.15
43/86 Moto. 6800 W/W	7.00	6.85

INTEGRATED CIRCUIT SOCKETS

	Low Profile each	Low Profile 100+	Wire Wrap each	Wire Wrap 100+
8 pin	$.10	$.09	$.46	$.41
14 pin	.10	.09	.45	.41
16 pin	.12	.11	.50	.45
18 pin	.15	.13	.68	.61
24 pin	.26	.24	.94	.87
40 pin	.42	.40	1.60	1.47

"D" Type	each	10-24	25+
DE9P male	$1.60	$1.40	$1.30
DE9S female	2.25	2.00	1.90
DE hood	1.50	1.35	1.20
DA15P male	2.35	2.15	2.00
DA15S female	3.25	3.10	2.90
DA hood 2/P	1.60	1.35	1.30
DB25P male	2.50	2.35	2.25
DB25S female	3.35	3.15	3.05
DB hood 2/P	1.35	1.15	1.05
DC37P male	4.20	4.00	3.70
DC37S female	6.00	5.75	5.50
DC hood 2/P	2.25	2.00	1.75
DD50P male	5.50	5.10	4.75
DD50S female	9.40	8.60	8.00
DD50 hood 2/P	2.60	2.40	2.10
CENTRONICS			
57-30360	7.95	6.75	5.75
RIBBON CABLE CONNECTORS			
17/34 5" disk	4.85	4.15	3.95
20/40 TRS-80	5.65	5.05	4.70
25/50 8" disk	5.90	5.15	4.90

23" COMPOSITE MONITOR $159



Ideal monitor for classroom demonstrations.

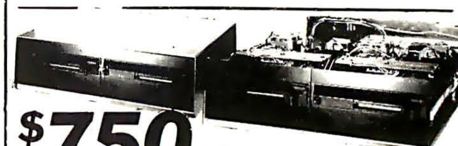
Ever try gathering a classroom of students around a 12" monitor? Here is your opportunity to purchase a 23" high resolution monitor at a reasonable price.
These units accept standard composit video signals generated by most personal computers including the Apple and IBM. Attach it your computer and in second you are shooting down Klingons in wide screen video.
MOT-BW23 35 Lbs. Monitors are open frame and for safety should be enclosed. Wood grained enclosure for above $35.00 additional CAL-ENC23 15 Lbs.



Eight Inch Single Sided

	One	Two	Ten
SHUGART SA801R	$395	385	375
SIEMENS FDD100-8	259	259	225
TANDON 848-1 SLIMLINE	379	369	359
Eight Inch Double Sided			
SHUGART SA851R	525	495	475
QUME DATA TRACK 8	525	495	475
MITSUBISHI M2894-63	485	475	469
OLIVETTI 802/851	369	359	349
TANDON 848-2 SLIMLINE	495	485	475
SHUGART 860 THINLINE	569	549	539
Five Inch Single Sided			
SHUGART SA400	215	209	199
TANDON TM 100-1	209	199	195
Five Inch Double Sided			
SHUGART SA450	349	329	315
TANDON TM 100-2	295	269	259
TANDON 96TPI TM100-4	369	355	350
OLIVETTI 502 ⅔ height	239	225	215
Three Inch Rigid Floppy			
HITACHI-AMDEK	call for pricing		
Five Inch Winchesters			
SEAGATE 506 6 Megabyte	759	725	695
SEAGATE 512 12 Megabyte	995	960	960
TANDON 603SE 14 Megabyte	995	960	895
WESTERN DYNAX removable	995	960	950

Upon request, all drives are supplied with power connectors and manual



$750 *Eight Inch Subsystem*

Two Siemens FDD100-8 disk drives with power supply, 4" exhaust fan complete with all necessary power cables.

Same as above but with:

Shugart 801R	MSD2801	$1195	Olivetti 802	CAL2802	$1250
Shugart 851R	MSD2851	1450	Qume DT8	MSD8DT	1450

ECLIPSE 100 $695



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Suitable for hospital and industrial applications. Constructed from 304 brushed stainless steel. Modualar 500 watt toroid power supply provides +8 volts at 30 Amps and ±16 volts at 4 Amps. Supplied with standard 18 slot Faraday mother board. Auxilary switched AC receptacles. The Eclipse 100 can be either table or rack mounted. Provisions for internally mounting a ten megabyte Winchester disk drive.
The Eclipse 100 is the perfect mainframe to fill the void left by the now defunct TEI Corporation. EPS-100 50 lbs.

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SN7401N	14	.19	SN7473N	14	.35	**SN74157N**	16	.59
SN7402N	14	.25	SN7474N	14	.35	SN74160N	16	.69
SN7403N	14	.25	SN7475N	16	.45	SN74161N	16	.69
SN7404N	14	.25	SN7476N	16	.35	SN74162N	16	.69
SN7405N	14	.25	SN7479N	14	4.95	SN74163N	16	.69
SN7406N	14	.29	SN7480N	14	.69	SN74164N	14	.69
SN7407N	14	.29	SN7482N	14	1.19	SN74165N	16	.69
SN7408N	14	.25	SN7483N	16	.59	SN74166N	16	.89
SN7409N	14	.25	SN7485N	16	.59	SN74167N	16	2.79
SN7410N	14	.25	SN7486N	14	.35	SN74170N	16	1.29
SN7411N	14	.25	SN7489N	16	2.25	SN74172N	24	4.95
SN7412N	14	.35	SN7490N	14	.39	SN74173N	16	.69
SN7413N	14	.35	SN7491N	14	.59	SN74174N	16	.69
SN7414N	14	.49	SN7492N	14	.39	SN74175N	16	.69
SN7416N	14	.25	SN7493N	14	.39	SN74176N	14	.69
SN7417N	14	.25	SN7494N	14	.69	SN74177N	14	.69
SN7420N	14	.19	SN7495N	14	.49	SN74179N	16	1.49
SN7421N	14	.35	SN7496N	16	.49	SN74180N	14	.69
SN7422N	14	.45	SN7497N	16	2.75	SN74181N	24	1.95
SN7423N	16	.59	SN74100N	24	1.49	SN74182N	16	.89
SN7425N	14	.29	SN74104N	14	.89	SN74184N	16	1.95
SN7426N	14	.29	SN74105N	14	.89	SN74185N	16	1.95
SN7427N	14	.25	**SN74107N**	14	.29	SN74190N	16	.69
SN7428N	14	.49	**SN74109N**	16	.39	SN74191N	16	.69
SN7430N	14	.25	SN74116N	24	1.49	SN74192N	16	.69
SN7432N	14	.29	SN74121N	14	.39	SN74193N	16	.69
SN7437N	14	.25	SN74122N	14	.55	SN74194N	16	.69
SN7438N	14	.29	SN74123N	16	.49	SN74195N	16	.69
SN7439N	14	.59	SN74125N	14	.45	SN74196N	14	.89
SN7440N	14	.19	SN74126N	14	.45	SN74197N	14	.89
SN7441N	16	.89	SN74132N	14	.49	SN74198N	24	1.19
SN7442N	16	.45	SN74136N	14	.69	SN74199N	24	1.19
SN7443N	16	.99	SN74141N	16	.69	SN74221N	16	1.19
SN7444N	16	.99	SN74142N	16	2.95	SN74251N	16	.79
SN7445N	16	.69	SN74143N	24	2.95	SN74276N	20	1.95
SN7446N	16	.69	SN74144N	24	2.95	SN74279N	16	.79
SN7447N	16	.69	SN74145N	16	.59	SN74283N	16	1.49
SN7448N	16	.69	SN74147N	16	1.49	SN74284N	16	2.95
SN7450N	14	.19	SN74148N	16	1.19	SN74285N	16	2.95
SN7451N	14	.19	SN74150N	24	1.19	SN74365N	16	.55
SN7453N	14	.19	SN74151N	16	.59	SN74366N	16	.55
SN7454N	14	.19	SN74152N	14	.59	SN74367N	16	.55
SN7459A	14	.25	SN74153N	16	.59	SN74368N	16	.55
SN7460N	14	.19	SN74154N	24	1.25	SN74390N	16	1.49
SN7470N	14	.29	SN74155N	16	.59	SN74393N	14	1.49

74LS

74LS00	14	.25	74LS92	14	.55	74LS192	16	.79
74LS01	14	.25	74LS93	14	.55	74LS193	16	.79
74LS02	14	.25	74LS95	14	.79	74LS194	16	.69
74LS03	14	.25	74LS96	16	.89	74LS195	16	.69
74LS04	14	.29	74LS107	14	.39	74LS197	14	.79
74LS05	14	.29	74LS109	16	.39	74LS221	16	.89
74LS08	14	.29	74LS112	16	.39	74LS240	20	1.09
74LS09	14	.29	74LS113	14	.39	74LS241	20	1.09
74LS10	14	.29	74LS114	14	.39	74LS242	14	1.09
74LS11	14	.35	74LS122	14	.49	74LS243	14	1.09
74LS12	14	.35	74LS123	16	.79	74LS244	20	1.09
74LS13	14	.39	74LS125	14	.49	74LS245	20	1.49
74LS14	14	.59	74LS126	14	.49	74LS247	16	1.09
74LS15	14	.35	74LS132	14	.59	74LS248	16	1.09
74LS20	14	.29	74LS133	16	.59	74LS249	16	1.09
74LS21	14	.29	74LS136	14	.39	74LS251	16	.59
74LS22	14	.29	74LS138	16	.59	74LS253	16	.59
74LS26	14	.29	74LS139	16	.59	74LS257	16	.59
74LS27	14	.29	74LS151	16	.59	74LS258	16	.59
74LS28	14	.35	74LS153	16	.59	74LS260	14	.59
74LS30	14	.29	74LS154	24	.99	74LS266	14	.69
74LS32	14	.35	74LS155	16	.69	74LS273	20	1.49
74LS33	14	.55	74LS156	16	.69	74LS279	16	.49
74LS37	14	.35	74LS157	16	.69	74LS283	16	.69
74LS38	14	.35	74LS158	16	.59	74LS290	14	.89
74LS40	14	.29	74LS160	16	.69	74LS293	14	.79
74LS42	16	.55	74LS161	16	.69	74LS298	16	.89
74LS47	16	.75	74LS162	16	.69	74LS352	16	1.29
74LS48	16	.75	74LS163	16	.69	74LS353	16	1.29
74LS49	14	.75	74LS164	14	.69	74LS365	16	.49
74LS51	14	.25	74LS165	16	1.19	74LS366	16	.49
74LS54	14	.25	74LS168	16	1.19	74LS367	16	.49
74LS55	14	.29	74LS169	16	1.19	74LS368	16	.49
74LS73	14	.39	74LS170	16	1.49	74LS373	20	1.29
74LS74	14	.39	74LS173	16	.69	74LS374	20	1.29
74LS75	16	.39	74LS174	16	.59	74LS375	16	.69
74LS76	16	.39	74LS175	16	.59	74LS385	14	.45
74LS78	14	.39	74LS181	24	2.49	74LS393	14	1.19
74LS83	16	.65	74LS190	16	.89	74LS399	16	1.49
74LS85	16	.69	74LS191	16	.89	74LS670	16	1.49
74LS86	14	.39				81LS95	20	1.49
74LS90	14	.55				81LS97	20	1.49

74S/PROMS*

74S00	14	.35	74S124	16	2.95	74S243	14	2.49
74S02	14	.35	74S133	16	.45	74S244	20	2.49
74S03	14	.35	74S134	16	.50	74S251	16	1.19
74S04	14	.45	74S135	16	.69	74S253	16	1.19
74S05	14	.45	74S136	14	1.39	74S257	16	1.19
74S08	14	.39	74S138	16	.89	74S258	16	1.19
74S09	14	.39	74S139	16	.89	74S260	14	.79
74S10	14	.35	74S140	14	.55	74S280	14	1.95
74S11	14	.35	74S151	16	.99	74S287*	16	1.95
74S15	14	.35	74S153	16	.99	74S288*	16	1.95
74S20	14	.35	74S157	16	.99	74S373	20	2.49
74S22	14	.35	74S158	16	.99	74S374	20	2.49
74S30	14	.35	74S160	16	2.49	74S387*	16	1.95
74S32	14	.45	74S174	16	.99	74S471*	20	5.95
74S38	14	.89	74S175	16	.99	74S472*	20	4.95
74S40	14	.39	74S188*	16	1.49	74S473*	20	4.95
74S51	14	.35	74S194	16	1.49	74S474*	24	4.95
74S64	14	.39	74S195	16	1.49	74S475*	24	4.95
74S65	14	.39	74S196	14	1.49	74S570*	16	2.95
74S74	14	.55	74S240	20	2.25	74S571*	16	2.95
74S86	14	.55	74S241	20	2.25	74S572*	18	4.95
74S112	16	.55	74S242	14	2.49	74S573*	18	4.95
74S113	14	.55				74S940	20	2.49
74S114	14	.55				74S941	20	2.49

CA—LINEAR

CA3010H		.99	CA3060N	16	3.25	CA3089N	16	1.69
CA3013H		2.15	CA3080E	8	.89	CA3096N	16	1.19
CA3023H		3.25	CA3081N	16	1.49	CA3130E	8	1.49
CA3035H		5.95	CA3082N	16	1.49	CA3140E	8	.99
CA3039H		1.35	CA3083N	16	1.49	CA3160H		1.95
CA3046N	14	.89	CA3086N	14	.69	CA3401N	14	.59
CA3059N	14	3.25				CA3600N	14	3.95

CD—CMOS

CD4000	14	.29	CD4040	16	.79	CD4098	16	1.95
CD4001	14	.29	CD4041	14	.79	CD4506	16	1.19
CD4002	14	.29	CD4042	16	.69	CD4507	14	.39
CD4006	14	.89	CD4043	16	.79	CD4508	24	3.95
CD4007	14	.29	CD4044	16	.79	CD4510	16	.89
CD4009	16	.39	CD4046	16	.89	CD4511	16	.89
CD4010	16	.39	CD4047	14	.89	CD4512	16	.89
CD4011	14	.29	CD4048	16	.39	CD4514	24	1.79
CD4012	14	.15	**CD4049**	16	.39	CD4515	24	1.79
CD4013	14	.39	CD4050	16	.39	CD4516	16	.99
CD4014	16	.79	CD4051	16	.79	CD4518	16	.99
CD4015	16	.39	CD4052	16	.79	CD4519	16	.39
CD4016	14	.39	CD4053	16	.79	CD4520	16	.79
CD4017	16	.75	CD4056	16	2.95	CD4526	16	1.19
CD4018	16	.79	CD4059	24	7.95	CD4528	16	1.19
CD4019	16	.39	CD4060	16	.89	CD4529	16	1.19
CD4020	16	.75	CD4066	14	.39	CD4543	16	1.19
CD4021	16	.79	CD4068	14	.39	CD4552	14	6.95
CD4022	16	.79	CD4069	14	.29	CD4566	16	1.39
CD4023	14	.29	CD4070	14	.39	CD4583	16	2.49
CD4024	14	.69	CD4071	14	.29	CD4584	14	.59
CD4025	14	.23	CD4072	14	.29	CD4723	16	1.19
CD4026	16	2.49	CD4073	14	.29	CD4724	16	1.19
CD4027	16	.45	CD4075	14	.29	MC14409	16	13.95
CD4028	16	.69	CD4076	16	.79	MC14410	16	13.95
CD4029	16	.79	CD4078	14	.49	MC14411	24	11.95
CD4030	14	.39	**CD4081**	14	.29	MC14412	16	13.95
CD4034	24	1.95	CD4082	14	.29	MC14419	16	7.95
CD4035	16	.89	CD4093	14	.49	MC14433	24	13.95
						MC14538	16	1.19
						MC14541	14	1.19

(More in Catalog)

MICROPROCESSOR COMPONENTS

MICROPROCESSOR CHIPS

Part No.	**Pins	Function	Price
CDP1802	40	CPU	$9.95
2650	40	MPU	14.95
IDM2901ADC	40	CPU—4-bit slice (Com. Temp. Gr.)	19.95
MCS6502	40	MPU w/Clock (65K bytes mem.)	9.95
MC6802CP	40	MPU w/Clock and RAM	7.95
INS8035N-6	40	MPU—8-bit (6MHz)	5.95
INS8039N-6	40	CPU-Sgl. chip 8-bit (128 bts. Ram)	5.95
INS8040N-6	40	CPU (256 bytes RAM)	5.95
INS8070N	40	CPU (64 bytes RAM)	11.95
INS8073N	40	CPU w/Basic Micro Interpreter	14.95
P8085A	40	CPU	5.95

Z80, Z80A, Z80B, Z8000 SERIES

Part No.	**Pins	Function	Price
Z80	40	CPU (MK3880N)(780C) 2MHz	$4.95
Z80-CTC	28	Counter Timer Circuit	5.95
Z80-DART	40	Dual Asynchronous Rec./Trans.	11.95
Z80-DMA	40	Direct Memory Access Circuit	15.95
Z80-P10	40	Parallel I/O Interface Controller	5.95
Z80-S10/0	40	Serial I/O (TxCB and RxCB Bonded)	15.95
Z80-S10/1	40	Serial I/O (Lacks DTRB)	15.95
Z80-S10/2	40	Serial I/O (Lacks SYNCB)	15.95
Z80-S10/9	40	Serial I/O	15.95
Z80A	40	CPU (MK3880N-4)(780C-1) 4MHz	5.95
Z80A-CTC	28	Counter Timer Circuit	5.95
Z80A-DART	40	Dual Asynchronous Rec./Trans.	11.95
Z80A-DMA	40	Direct Memory Access Circuit	17.95
Z80A-P10	40	Parallel I/O Interface Controller	5.95
Z80A-S10/0	40	Serial I/O (TxCB and RxCB bonded)	16.95
Z80A-S10/1	40	Serial I/O (Lacks DTRB)	16.95
Z80A-S10/2	40	Serial I/O (Lacks SYNCB)	16.95
Z80A-S10/9	40	Serial I/O	16.95
Z80B	40	CPU (MK3880N-6) 6MHz	11.95
Z80B-CTC	28	Counter Timer Circuit	13.95
Z80B-P10	40	Parallel I/O Interface Controller	13.95
Z8001	48	CPU Segmented	51.95
Z8002	40	CPU Non-Segmented	55.95
Z8030	40	Serial Comm. Controller	44.95
Z8036	40	Counter/Timer & Parallel I/O Unit	29.95

6800/68000 SERIES

Part No.	**Pins	Function	Price
MC6800	40	MPU	4.95
MC6802CP	40	MPU with clock and RAM	7.95
MC6810API	24	128x8 Static RAM	3.95
MC6821	40	Peripheral Inter. Adapt (MC6820)	4.95
MC6828	24	Priority Interrupt Controller	15.95
MC6830L8	24	1024x8-bit ROM (MC68A30-8)	10.95
MC6850	24	Asynchronous Comm. Adapter	4.95
MC6852	24	Synchronous Serial Data Adapter	5.75
MC6860	24	0-600bps Digital MODEM	9.95
MC6862	24	2400bps Modulator	12.95
MC6880A	16	Quad 3-state bus. trans. (MC8T26)	2.25
MC68000L8	64	MPU 16-Bit (8MHz)	69.95
MC68488P	40	General Purpose Int. Adapter	8.95
MC68652P2	40	Multi. Protocol Comm. Controller	24.95
MC68661PB	28	Enhanced Prog. Comm. Int.	8.95

8080A SERIES

Part No.	**Pins	Function	Price
INS8080A	40	CPU	3.95
TMS5501	40	Synchronous Data Interface (SIRC)	14.95
INS8154	40	128 Byte RAM 16-Bit I/O	13.95
INS82C06	20	Octal D Flip Flop Tri-State (74C374)	2.49
DP8212	24	8-bit Input/Output (74S412)	2.25
DP8214	24	Priority Interrupt Control	3.95
DP8216	16	Bi-Directional Bus Driver	2.25
DP8224	16	Clock Generator/Driver	2.25
DP8226	16	Bus Driver	2.25
DP8228	28	System Cont./Bus Driver (74S428)	3.49
DP8238	28	System Controller (74S438)	4.49
INS8243	24	I/O Expander for 48 Series	5.95
INS8245	18	16-Key Keyboard Encoder (74C922)	4.49
INS8246	20	20-Key Keyboard Encoder (74C923)	4.95
INS8247	28	Display Controller (74C911)	8.95
INS8248	28	Display Controller (74C912)	8.95
INS8250N	40	Asyn. Comm. Element (INS8250)	10.95
DP8251	28	Prog. Comm. I/O (USART)	4.49
DP8253	24	Prog. Interval Timer	6.95
DP8255	40	Prog. Peripheral I/O (PPI)	4.49
DP8257	40	Prog. DMA Control	7.95
DP8259	28	Prog. Interrupt Control	6.95
DP8275	40	Prog. CRT Controller	29.95
DP8279	40	Prog. Keyboard/Display Interface	6.95
DP8303	20	8-Bit Tri-State Bi-Directional Trans.	3.95
DP8304	20	8-bit Bi-Directional Receiver	2.49
DP8307	20	8-bit Bi-Directional Receiver	2.49
DP8308	20	8-bit Bi-Directional Receiver	2.49
DP8310	20	Octal Latched Peripheral Driver	4.95
DP8311	20	Octal Latched Peripheral Driver	4.95

MICROPROCESSOR MANUALS & DATA BOOKS

M-Z80	User Manual	7.50
M-CDP1802	User Manual	7.50
M-2650	User Manual	5.00
10400	1982 Intel Data Book (1405 pg.)	14.95
30001	1981 Nat. CMOS Book (628 pg.)	6.95
30002	1980 Nat. Interface Book (640 pg.)	6.95
30003	1982 Nat. Linear Book (1952 pg.)	11.95
30005	1981 Nat. TTL Book (624 pg.)	9.95
30008	1980 Nat. Memory Data Book (464 pg.)	6.95
30011	1980 Nat. Linear Applications (736 pg.)	15.95
30013	1983 Zilog Data Book (641 pg.)	7.95
205610	1981 Intel Peripheral Design (828 pg.)	9.95

DYNAMIC RAMS

Part No.	**Pins			Price
1103	18	1024x1	(300ns)	.99
4027	16	**4096x1**	**(250ns)**	**2.49**
4116N-2	16	16,384x1	(150ns)	1.89 - 8/14.95
4116N-3	16	16,384x1	(200ns)	1.69 - 8/12.95
4116N-4	16	16,384x1	(250ns)	1.49 - 8/10.95
4164N-150	16	65,536x1	(150ns)	7.95 - 8/59.95
4164N-200	16	65,536x1	(200ns)	7.49 - 8/54.95
MM5261	18	1024x1	(300ns)	.49 - 8/1.95
MM5262	22	**2048x1**	**(365ns)**	**.49 — 8/1.95**
MM5270	18	4096x1	(250ns) MK4096	4.95
MM5280	22	4096x1	(200ns) 2107	3.95
MM5290-2	16	16,384x1	(150ns)	1.89 - 8/14.95
MM5290-3	16	16,384x1	(200ns)	1.69 - 8/12.95
MM5290-4	16	16,384x1	(250ns)	1.49 - 8/10.95
MM5298-3	16	8192x1	(200ns)	1.69

STATIC RAMS

1101	16	256x1	(650ns)	1.49
2101	22	256x4	(450ns) 8101	2.49
2102	16	1024x1	(350ns)	.89
21L02	16	1024x1	(450ns) L.P.	1.49
2111	18	256x4	(450ns) 8111	2.95
2112	16	256x4	(450ns) MOS	2.95
2114	18	1024x4	(450ns)	1.95 - 8/13.95
2114L	18	1024x4	(450ns) L.P.	2.25 - 8/15.95
2114-2	18	1024x4	(200ns)	2.25 - 8/15.95
2114L-2	18	1024x4	(200ns) L.P.	2.49 - 8/17.95
2141-3	18	4096x1	(150ns)	3.95
2147	18	4096x1	(70ns)	4.95
2148	18	1024x4	(70ns)	8.95
TMS4044	18	4096x1	(450ns)	3.95
TMS4045	18	1024x4	(450ns)	3.95
5101	22	256x4	(450ns) CMOS	4.95
MM5257	18	4096x1	(450ns) 4044	4.95
HM6116P-3	24	2048x8	(150ns) CMOS	7.95
HM6116-4	24	2048x8	(200ns) CMOS	6.95
HM6116LP-4	24	2048x8	(200ns) L.P. CMOS	7.95
7489	16	16x4	(50ns) 3101	2.25
74C920	22	256x4	(250ns) CMOS (6551)	3.95
74C921	18	256x4	(250ns) CMOS	3.95
74C929	16	1024x1	(250ns) CMOS (6501)	3.95
74C930	18	1024x1	(250ns) CMOS (6518)	3.95
74S189	16	16x4	(35ns) 93405	1.95
74S200	16	256x1	(80ns) 93410	3.95
74S206	16	256x1	(60ns) 93411	3.95
74S289	16	16x4	(35ns) 3101	2.25
82S10	16	1024x1	(50ns) O.C. (93415)	3.95
82S25	16	16x4	(50ns) O.C. (74S289)	2.25

EPROMS

1702A	24	256x8	(1us)	4.95
2708	24	1024x8	(450ns)	3.95
2708-5	24	1024x8	(550ns) SM00246	2.95
TMS2516	24	2048x8	(450ns) 2716	6.95
TMS2532	24	4096x8	(450ns) NMC2532	9.95
TMS2564	28	8192x8	(450ns)	19.95
TMS2716	24	2048x8	(450ns) 3 voltage	7.95
2716	24	2048x8	(450ns)	4.95
2716-1	24	2048x8	(350ns)	6.95
2732	24	4096x8	(450ns)	9.95
27580	24	1024x8	(450ns) single +5V	2.95
MM2764	28	8192x8	(450ns)	16.95
MM2764-3	28	8192x8	(300ns)	19.95

PROMS

74S188	16	32x8	PROM O.C. (6330-1)	1.49
74S287	16	256x4	PROM T.S. (6301-1)	1.95
74S288	16	32x8	PROM T.S. (6331-1)	1.95
74S387	16	256x4	PROM O.C. (6300-1)	1.95
74S471	20	256x8	PROM T.S. (6309-1)	5.95
74S472	20	512x8	PROM T.S. (6349-1)	4.95
74S473	20	512x8	PROM O.C. (6348)	4.95
74S474	24	512x8	PROM T.S. (DM87S296N)	4.95
74S475	24	512x8	PROM O.C. (6340)	4.95
74S478	24	1024x8	PROM T.S. (TBP28S86)	8.95
74S570	16	512x4	PROM O.C. (6305)	2.95
74S571	16	512x4	PROM T.S. (6306)	2.95
74S572	18	1024x4	PROM O.C. (6352)	4.95
74S573	18	1024x4	PROM T.S. (82S137)	4.95
82S23	16	32x8	PROM O.C. (27S18)	2.95
82S115	24	512x8	PROM T.S. (27S15)	9.95
82S123	16	32x8	PROM T.S. (27S19)	2.95
82S126	16	256x4	PROM O.C. (27S20)	3.95
82S129	16	256x4	PROM T.S. (27S21)	3.95
82S130	16	512x4	PROM O.C. (27S12)	5.95
82S185	18	2048x4	PROM T.S. (TBP24S81)	9.95
DM87S180N	24	1024x8	PROM O.C. (82S180)	9.95
DM87S181N	24	1024x8	PROM T.S. (82S181)	9.95
DM87S184N	18	2048x4	PROM O.C. (82S184)	9.95
DM87S185N	18	2048x4	PROM T.S. (82S185)	9.95
DM87S190N	24	2048x4	PROM O.C. (82S190)	19.95
DM87S191N	24	2048x8	PROM T.S. (82S191)	19.95

DATA ACQUISITION

DC10		Mostek DC/DC Convert. +5V to -9V	2.95
MC3470P	18	Floppy Disk Read AMP System	4.95
MC1408L7	16	7-bit D/A Converter (DAC0807LCN)	2.49
MC1408L8	18	8-bit D/A Converter (DAC0808LCN)	2.95
ADC0804	20	8-bit A/D Converter (1 LSB)	3.49
DAC0806	16	8-bit D/A Converter (0.78% Lin.)	1.95
ADC0809	28	8-bit A/D Converter (8-Ch. Multi.)	4.49
AY-5-1013A	**40**	**30K Baud Uart (TR1602)**	**4.95**

CONNECTORS

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Part No.	Description	Price
DE9P	9 Pin Plug	$1.79
DE9S	9 Pin Socket	1.95
DA15P	15 Pin Plug	1.95
DA15S	15 Pin Socket	2.95
DB25P	**25 Pin Plug (Meets RS232)**	**2.49**
DB25S	**25 Pin Socket (Meets RS232)**	**3.25**
DB25P-831	25 Pin Right Angle Plug	4.95
DB25S-831	25 Pin Right Angle Socket	5.25
DC37P	37 Pin Plug	4.95
DC37S	37 Pin Socket	5.95
DD50P	50 Pin Plug	5.95
DD50S	50 Pin Socket	6.95

Accessories

DE-9H	Hood for DE-9 Series Connectors	$1.19
DA-15H	Hood for DA-15 Series Connectors	1.29
DB25H	Hood for DB25 Series Connectors	1.25
DC37H	Hood for DC37 Series Connectors	1.39
DD50H	Hood for DD50 Series Connectors	1.49
D20418-2	2 screws for mtg. connectors to a panel	.79

Solder Eyelet/Wire Wrap Edge Card

Part No.	Cnts.	Sp.	Description	Price
15/30SE	15/30	.156	Solder Eyelet	$1.79
18/36SE	18/36	.156	Solder Eyelet	1.95
22/44SE	22/44	.156	Solder Eyelet	2.49
22/44PC	22/44	.156	PC type (no mtg. ears)	.99
50/100SE	50/100	.125	Solder Eyelet	9.95
22/44WW	22/44	.156	Wire Wrap - Level 3	4.95
67031-5	22/44	.156	WW (Pins .0625x.03x.75)	3.95
R-681-1	50/100	.125	Wire Wrap - Level 3	7.95
R-681-2	50/100	.125	Wire Wrap - Level 1	6.95

RF Coaxial Connectors

Part No.	Description	Price
PL259	UHF Plug	$ .89
SO239	UHF Panel Receptacle	.69
PL258	UHF Straight Adapter	.89
UG175/U	UHF Reducing Adapter	.49
UG88/U	BNC Plug	1.49
UG89/U	BNC Jack	1.69
UG306/U	BNC Angle Adapter	2.49
UG260/U	BNC Plug	1.49
UG1094/U	BNC Bulkhead Receptacle	.89

IC SOCKETS

For Socket Required, See Column After The IC Part No.

LOW PROFILE (TIN) SOCKETS

	1-9	10-99	100-999
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14 pin LP	.17	.15	.14
16 pin LP	.19	.17	.16
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22 pin LP	.31	.28	.26
24 pin LP	.33	.30	.28
28 pin LP	.40	.37	.35
36 pin LP	.46	.42	.39
40 pin LP	.49	.46	.43

— Soldertail Standard Tin & Gold Also Available —

WIRE WRAP (GOLD) SOCKETS LEVEL #3

	1-9	10-99	100-999
8 pin WW	.49	.45	.42
10 pin WW	.65	.62	.59
14 pin WW	.65	.62	.59
16 pin WW	.69	.65	.61
18 pin WW	.89	.85	.79
20 pin WW	1.09	1.05	.99
22 pin WW	1.25	1.19	1.15
24 pin WW	1.29	1.23	1.18
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Digitalker™

DT1050 — Applications: Teaching aids, appliances, clocks, automotive, telecommunications, language translations, etc.

The DT1050 is a standard DIGITALKER kit encoded with 137 separate and useful words, 2 tones, and 5 different silence durations. The words and tones have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences. The "voice" output of the DT1050 is a highly intelligible male voice. Female and children's voices can be synthesized. The vocabulary is chosen so that it is applicable to many products and markets.

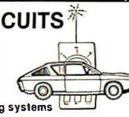
The DT1050 consists of a Speech Professor Chip, MM54104 (40-pin) and two (2) Speech ROMs MM52164SSR1 and MM52164SSR2 (24-pin) along with a Master Word list and a recommended schematic diagram on the application sheet.

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DT1057 — Expands the DT1050 vocabulary from 137 to over 260 words. Incl. 2 ROMs and specs.

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SRX1505 49.890MHz Crystal (LM1871N) ... $3.95

INTERSIL

★Evaluation Kits

Part No.	**Pins	Function	Price
7045IPI	28	CMOS Precision Timer	14.95
7045EV/Kit*	28	Stopwatch Chip, XTL	19.95
7106CPL	40	3½ Digit A/D (LCD Drive)	9.95
7106EV/Kit*	40	IC, Circuit Board, Display	34.95
7107CPL	40	3½ Digit A/D (LED Drive)	11.95
7107EV/Kit*	40	IC, Circuit Board, Display	29.95
7116CPL	40	3½ Digit A/D LCD Dis. HLD	16.95
7117CPL	40	3½ Digit A/D LED Dis. HLD	15.95
7201IUS		Low Battery Volt Indicator	2.25
7205IPG	24	CMOS LED Stopwatch/Timer	12.95
7205EV/Kit*	24	Stopwatch Chip, XTL	14.95
7206CJPE	16	Tone Generator	4.95
7206CEV/Kit*	16	Tone Generator Chip, XTL	7.95
7207AIPD	14	Oscillator Controller	5.95
7207AEV/Kit*	14	Freq. Counter Chip, XTL	7.95
7208IPI	28	Seven Decade Counter	15.95
7209IPA	8	Clock Generator	3.95
7215IPG	24	4 Func. CMOS Stopwatch CKT	13.95
7215EV/Kit*	24	4 Func. Stopwatch Chip, XTL	14.95
7216AIJI	28	8 Digit Univ. Counter C.A.	29.95
7216CIJI	28	8 Digit Freq. Counter C.A.	24.95
7216DIPI	28	8 Digit Freq. Counter C.C.	19.95
7217IJI	28	4 Digit LED Up/Down Counter C.A.	10.95
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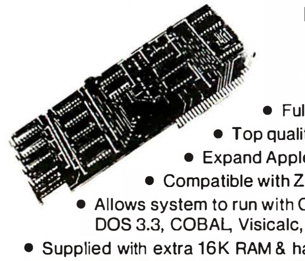
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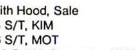
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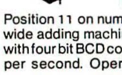
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20 pin LP	.34	.32	.30
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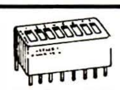
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LM320H-XX*	1.25	LM3053N	1.49
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LM324N	.95	CA3060N	3.19
LM337K	5.95	CA3062N	4.95
LM338K	6.95	LM3065N	1.49
LM339N	.95	CA3080T	1.29
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LM340H-XX*	1.25	CA3083N	1.55
LM344H	1.95	CA3086N	.80
LM348N	1.20	CA3089N	2.99
LM350K	5.60	CA3096N	3.49
LM358CN	.98	CA3097N	1.99
LM360N	1.49	CA3130T	1.30
LM372N	1.95	CA3140T	1.19
LM376N	3.75	CA3146N	2.49
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LM733N/H	.98	SN75451N	.35
LM739N	1.15	SN75452N	.49
LM741CN/H	.33	SN75453N	.49
LM741CN-14	.19	SN75454N	.49
LM747N/H	.75	SN75491N	.89
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MC1350	1.95	TL496CP	1.65
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74S00

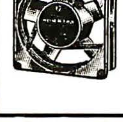
74S00	$ .39	74S124	3.69	74S244	$2.99
74S02	.43	74S133	.54	74S251	1.35
74S03	.45	74S134	.66	74S253	1.35
74S04	.52	74S135	1.15	74S257	1.29
74S05	.52	74S136	1.69	74S258	1.29
74S08	.49	74S138	1.29	74S260	.75
74S09	.49	74S139	1.29	74S280	2.79
74S10	.42	74S140	.73	74S287	2.99
74S11	.42	74S151	1.29	74S288	2.55
74S15	.42	74S153	1.29	74S373	3.10
74S20	.42	74S157	1.29	74S374	3.10
74S22	.42	74S158	1.29	74S387	2.75
74S30	.42	74S160	2.79	74S471	7.95
74S32	.48	74S174	1.49	74S472	7.95
74S38	1.19	74S175	1.49	74S473	7.95
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7404	.22	7482	.95	74165	.87
7405	.23	7483	.55	74166	1.20
7406	.35	7485	.65	74167	1.95
7407	.35	7486	.35	74170	1.69
7408	.26	7489	1.75	74172	4.75
7409	.23	7490	.39	74173	.79
7410	.22	7491	.57	74174	.89
7411	.29	7492	.45	74175	.85
7412	.29	7493	.45	74176	.75
7413	.39	7494	.69	74177	.75
7414	.59	7495	.65	74179	1.34
7416	.29	7496	.69	74180	.75
7417	.29	7497	2.90	74181	1.75
7420	.22	74100	2.90	74182	.75
7421	.35	74107	.32	74184	2.25
7422	.29	74109	.37	74185	2.25
7423	.29	74116	1.95	74186	9.95
7425	.29	74121	.29	74188	3.90
7426	.29	74122	.39	74190	1.15
7427	.25	74123	.59	74191	1.15
7429	.45	74125	.39	74192	.85
7430	.23	74126	.44	74193	.85
7432	.29	74128	.59	74194	.85
7437	.25	74132	.69	74195	.68
7438	.29	74136	.75	74196	.85
7439	.29	74139	.95	74197	.85
7440	.19	74141	.79	74198	1.39
7441	.79	74142	2.95	74199	1.39
7442	.57	74143	2.95	74221	1.19
7443	.95	74144	2.95	74251	.95
7444	.95	74145	.62	74273	1.05
7445	.79	74147	1.95	74276	1.89
7446	.79	74148	1.20	74279	.75
7447	.65	74150	1.09	74283	1.40
7448	.79	74151	.67	74284	3.90
7450	.19	74152	.67	74285	3.90
7451	.19	74153	.67	74290	1.25
7453	.19	74154	1.19	74298	.95
7454	.19	74155	.78	74365	.68
7459	.25	74156	.78	74366	.68
7460	.23	74157	.69	74367	.68
7470	.29	74158	1.65	74368	.88
7472	.29	74159	2.49	74390	1.45
7473	.34	74160	.88	74393	1.90
7474	.34			74490	1.90

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74LS01	.28	74LS114	.43	74LS247	1.10
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74LS03	.28	74LS123	1.19	74LS249	1.19
74LS04	.35	74LS124	1.35	74LS251	1.40
74LS05	.28	74LS125	.89	74LS253	1.40
74LS08	.28	74LS126	.52	74LS257	.85
74LS09	.33	74LS132	.79	74LS258	.98
74LS10	.28	74LS136	.49	74LS259	2.95
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74LS12	.33	74LS139	.85	74LS261	2.49
74LS13	.47	74LS145	1.25	74LS266	.59
74LS14	.95	74LS148	1.49	74LS273	1.75
74LS15	.33	74LS151	.79	74LS275	4.40
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74LS27	.33	74LS157	.85	74LS295	1.10
74LS28	.33	74LS158	.75	74LS298	1.19
74LS30	.26	74LS160	1.05	74LS324	1.75
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74LS33	.55	74LS162	1.05	74LS348	1.95
74LS37	.45	74LS163	1.05	74LS352	1.19
74LS38	.39	74LS164	1.19	74LS353	1.19
74LS40	.26	74LS165	.89	74LS363	1.49
74LS42	.79	74LS166	2.48	74LS365	.69
74LS47	.79	74LS168	1.15	74LS366	.69
74LS48	.95	74LS169	1.15	74LS367	.69
74LS51	.26	74LS170	1.99	74LS368	.69
74LS54	.29	74LS173	.89	74LS373	1.89
74LS55	.29	74LS174	.89	74LS374	1.89
74LS73	.45	74LS175	.89	74LS375	.69
74LS74	.42	74LS181	2.20	74LS377	1.95
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74LS83A	.79	74LS193	.98	74LS393	1.95
74LS85	1.19	74LS194	1.15	74LS395	1.70
74LS86	.45	74LS195	.95	74LS399	2.35
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74LS92	.75	74LS197	.89	74LS668	1.75
74LS93	.75	74LS221	1.15	74LS670	2.29
74LS95	.88	74LS240	1.69	81LS95	1.69
74LS96	.98	74LS242	1.69	81LS96	1.69
74LS107	.45	74LS243	1.69	81LS97	1.69
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74LS112	.43				

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4015	1.15	4052	1.10	4502	1.65
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4023	.29	4070	.49	4512	1.39
4024	.75	4071	.35	4515	2.75
4025	.25	4072	.35	4516	1.45
4027	.65	4073	.35	4518	1.39
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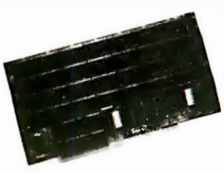
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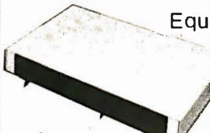
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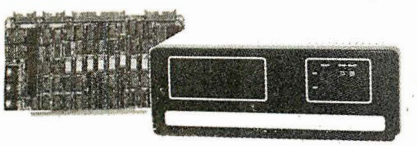


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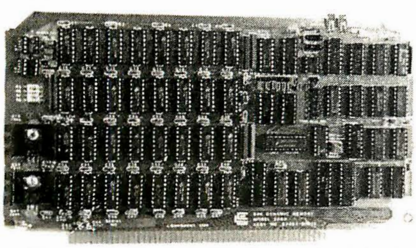
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Z80 35MB SUBSYSTEM



- Z80A 4MHz CPU
- 64K RAM
- 35 MegaByte Winchester Hard Disk Drive, Cabinet, and Power Supply
- Hard Disk Drive BIOS
- 2 RS-232 I/O Ports
- Floppy Disk Controller
- user Friendly Menu Driven CP/M 2.2™
- Drive Interface Cable.

ALL OF THIS FOR ONLY:
$4495.00 SAVE $950!!
If purchased separately: $5445.00
BPPDBSBCSYS1 (Shipped Freight Collect)

California Computer Systems
64K IEEE/S-100 DYNAMIC RAM



2 or 4MHz BANK SELECTABLE

- 2 or 4MHz operation
- Designed to IEEE proposed S-100 bus standard
- Operates with either an 8080 or Z-80 based S-100 system providing processor transparent refreshes with both
- Bank-select system allows system memory expansion
- Any 16K block can be made bank-independent
- All 64K can be made bank-enabled on and reset
- Supports DMA
- Jumper-selectable Phantom input
- Assembled & Tested
- Uses Popular 4116 RAMs

REGULAR LIST PRICE IS $375.00
$199.00
BPCCS20653 (Sh. Wt. 2 lbs.)

DUAL QUME 8" FLOPPY DRIVE, CABINET, DMA S-100 CONTROLLER, AND CP/M® FROM CompuPro

$1595.00
BPPDBGBT206SYS



YOU SAVE $1419.77!!

ABSOLUTELY THE MOST COST EFFECTIVE DISK SUBSYSTEM EVER OFFERED BY PRIORITY ONE ELECTRONICS!!

			List Price
• 2 Double sided 8" QUME DT8 disk drives			
• DMA Floppy Controller (controls up to 4 drives)	1	GBT206SP	$2325.00
• CP/M* 2.2 w/bios written for the Disk 1 Controller	1	GBT171A	$495.00
• Cabinet includes power supply & internal data cable	1	GBTCPM80	$175.00
• External data cable included	1	PGC50S60S	$ 19.77
(Shipping Charge $21.80, shipped in two boxes)			$3014.77

CABINET AND 2 QUME DT8 DOUBLE SIDED DRIVES PROVIDE 2.4 MBYTES OF MASS STORAGE!! $1295.00
(Sh. Wt. 50 lbs.) List: $2325.00 SAVE $1030.00! BPGBT206SP

CompuPro™ UN-SYSTEM 816

FOR THOSE WHO DEMAND EXCELLENCE!



Each CompuPro system contains the same nucleus of common hardware and software. This insures compatibility between systems as well as allowing you to expand as your needs grow. The following is a list of the basic hardware components as well as software.

HARDWARE:
- Desk top Enclosure 20 slots
- Floppy disk enclosure with 2 Qume DT8 drives
- DMA Floppy Controller
- 8085/8088 CPU operates 8 or 16 software
- Memory in the form of RAM 17s
- System support 1 (Clock calendar, RAM/ROM/math processor options, RS-232 Serial port, dual interrupt controllers, triple interval timers and more!)
- All internal cables

SOFTWARE:
- CP/M 2.2™ and CP/M 86™
- M Drive Software - allows the use of memory as another disk drive
- Sorcim's SUPERCALC 86™
- Ashton Tate's DBase II

DIG DEEP!! Now is the time to buy the CompuPro UN-SYSTEM 816!!
SAVE MONEY, and have an UN-SYSTEM 816 for your very own! All UN-SYSTEMS contain the very same components as the SYSTEM 816s listed in our Winter 1983 Engineering Selection Guide, but are not installed or configured. All it takes is your professional computer experience and knowledge to have the highest performing S-100 computer system on the market today. BEWARE! This is not for the novice and inexperienced user, as it requires a well-matured knowledge in system integration procedures.

So, WHY WAIT!? Don't Pass Up This Incredible Deal!!
Each component of the UN-SYSTEM 816 has been assembled and individually tested. Final installation and configuration are the sole responsibility of the purchaser.

UN-SYSTEM 816/A
ENTRY LEVEL - SINGLE USER
Disk storage 2.4 Megabytes. Expandable to 4.8 Megabytes.
Main memory: 128K - expandable to 1 Megabyte
Serial Ports: 4 / Parallel Ports: 1
Centronics/Epson ports: 1
Software: CP/M 2.2™, CP/M-86™, M-Drive, SuperCalc-86, dBase.
Component List Price: $6705.00 BPGBTUNSYSA16
OUR SALE PRICE: $4795.00 SAVE $1910.00!!

UN-SYSTEM 816/B
ENHANCED HIGH PERFORMANCE SINGLE USER SYSTEM
Disk Storage: 2.4 Megabytes. Expandable to 4.8 Megabytes.
Main memory: 256K - expandable to 1 Megabyte
Serial ports: 6
Software: CP/M 2.2™, CP/M-86™, M-Drive, SuperCalc-86™, dBase II™
Component List Price: $8497.00 BPGBTUNSYSB16
OUR SALE PRICE: $5795.00 SAVE $2702.00!!

UN-SYSTEM 816/C
HIGH PERFORMANCE MULTI-USER SYSTEM
Disk storage: 2.4 Megabytes. Expandable to 4.8 Megabytes.
Main memory: 384K - expandable to 1 Megabyte
Serial ports: 9
Software: CP/M 2.2™, CP/M-86™, MP/M 8-16™, M-Drive, SuperCalc-86™, dBase II™
Component List Price: $10,636.00 BPGBTUNSYSC16
OUR SALE PRICE: $7595.00 SAVE $3041.00!!

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ORDER TOLL FREE (800) 423-5922 - CA, AK, HI CALL (213) 709-5111
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SANYO
12" DATA DISPLAY MONITOR
24 Lines x 64 Characters



SAVE OVER 50% !!

BPSYODM2112 List Price: $160.00
SALE PRICE:
$75.00 !!
SAVE $85.00!! (Sh Wt 16 lbs.)

LOWEST COST PRINTERS AVAILABLE
$299.00 !!



COEX 80 F/T (Sh Wt 21 lbs)

- 80 cps • 10, 12 or 16.5 cpi • 3 selectable line spacing • Vertical format control • Centronics parallel or RS232 serial interface • Uses a standard Underwood spooled ribbon • Friction and tractor feed

		List Price	OUR Price
BPCOX80FT	Parallel int	$399.00	$299.00
BPCOX80FTSER	Serial int	$399.00	$299.00
BPCOXAPLINTP	Apple parallel interface w/cable		$49.95

$229.00
AXIOM AXIOM CORPORATION

SAVE $160.00!!

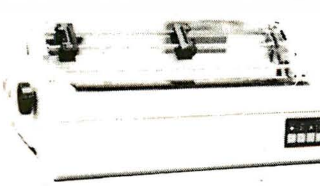


(Sh Wt 11 lbs)

- 5 x 7 Dot Matrix • Parallel Interface (Centronics) • Tractor Feed • Dot Addressable Graphics • Up to 3-Part Paper • Self Test • One Year Warranty • 30 CPS 80 Column Unidirectional • Uses Regular Paper

BPAXMGP100A Dot Matrix Printer $389.00 **$229.00**

THE COMPATIBLE P1350
TOSHIBA
100 CPS LETTER QUALITY, 200 CPS DRAFT MODE
LETTER QUALITY DOT MATRIX PRINTER!



$1895.00
BPCCCP1350 List Price: $2195.00

- Serial Interface
- Fast 200 cps draft mode
- High quality Word Processing mode for letter quality
- Full graphics capabilities (dot addressable)
- Software or switch selectable type styles
- Complete plotter capability with bidirectional tractor
- Unique 24 pin MICRO DOT matrix print head

		List Price	OUR Price
BPCCP1350T	Bidrectional tractor	$295.00	$275.00

You won't believe the print quality of the COMPATIBLE in its letter quality mode! If we didn't tell you it was dot matrix, you would have never known! (Shipping Weight 48 lbs.)

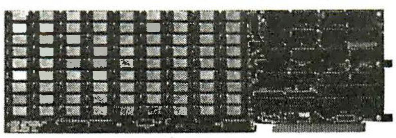
IBM® MULTICARD
Vista™ MEMORY & I/O CARD



- 64K RAM Expandable to 256K
- One RS232 Serial Port
- One Parallel Printer Port
- Real Time Clock Calendar with Battery Backup (Sh. Wt. 1 lb.)

BPVIS025665 List Price: $595.00
SALE PRICE:
$399.00

IBM® MAXICARD
Vista PERSONAL COMPUTER RAM CARD
POPULATED IN 64K, 256K, or 576K



- Runs at full speed with no wait states
- Parity can be disabled at User's option
- On board parity bit on each Byte
- Fully expanded, a full 576KB on one card
- One board fills entire primary RAM address space available
- Full Vista 120 Day Warranty

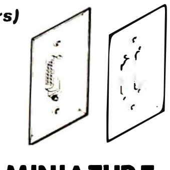
64K $199.00
BPVIS057664 List Price: $379.00
SAVE $180.00

256K $449.00
BPVIS0576256 List Price: $789.00
SAVE $340.00

576K $950.00
BPVIS0576576 List Price: $1299.00
SAVE $349.00

(IBM is a trademark of International Business Machines)

EIA/RS232 WALL PLATES
(Does not include connectors)



BPIIIWPDB251 Single punched
4/$10.00
BPIIIWPDB252 Dual Punched
4/$12.00

RS-232 "D" SUB-MINIATURE CONNECTORS



		1-9	10-24	25-99	100-UP
BPCNDDB25P	25 Pin Male	$2.75	$2.50	$2.25	$1.95
BPCNDDB25S	25 Pin Female	$4.00	$3.50	$3.25	$3.00
BPCNDDB51212	1 Pc Grey Hood	$1.65	$1.40	$1.25	$1.15
BPCNDP25H	2 Pc Grey Hood	$1.50	$1.25	$1.10	$1.00
BPCNDDB51226	2 Pc Black Hood	$1.75	$1.50	$1.35	$1.20
BPCND020418	Hardware set 2/Pr	$1.00	$ .80	$ .70	$ .60

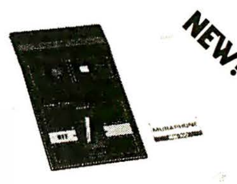
TEXAS INSTRUMENTS
16 PIN GOLD AND TIN DIP SOLDERTAIL SOCKETS



QTY	TIN BPTIS16LP	GOLD BPTIG16LP
50	$ 8.00	$ 10.00
1000	$ 60.00	$ 80.00
4500	$225.00	$315.00

DIRECT CONNECT MODEM
$79.00
0 - 300 BAUD MURA MM-100

NEW!



- 0 - 300 baud
- RS232C interface
- Full duplex
- Carrier detect indicator
- Bell 103 compatible
- Low voltage
- Originate/Answer switch selectable

		List Price	SALE
BPMURMM100	0 - 300 baud modem (Shipping Weight: 2 lbs.)	$99.95	$79.00
BPCNDRS2328F	RS232 cable		$19.95

SUPER LOW PRICES! DOUBLE DENSITY!
5¼" FLOPPY DISKETTES
LIFETIME WARRANTY!



FEATURES:
- Includes reinforcement ring
- Write protect with tabs
- 100% Surface tested
- Lifetime warranty

SALE!

SINGLE SIDED
40 TRACKS — DOUBLE DENSITY
ORDER INFORMATION:
BPULT51401 Soft Sector
BPULT51410 10 Sector
BPULT51416 16 Sector

BOX OF 10 **$25.00**
2 BOXES: **$40.00**
10 BOXES: **$180.00**

Description		Box of 10	2 Boxes	10 Boxes
BPULT52401	Soft sector, 40 track, 2 side	$35.00	$60.00	$280.00
BPULT52410	10 sector, 40 track, 2 side			
BPULT52416	16 sector, 40 track, 2 side			
BPULT51801	Soft sector, 80 track, 1 side	$30.00	$50.00	$220.00
BPULT51810	10 sector, 80 track, 1 side			
BPULT51816	16 sector, 80 track, 1 side			
BPULT52801	Soft sector, 80 track, 2 sided	$40.00	$70.00	$320.00
BPULT52810	10 sector, 80 track, 2 sided			
BPULT52816	16 Sector, 80 track, 2 sided	(Sh. Wt. 2 lbs)	(Sh. Wt. 4 lbs.)	(Sh. Wt. 20 lbs.)

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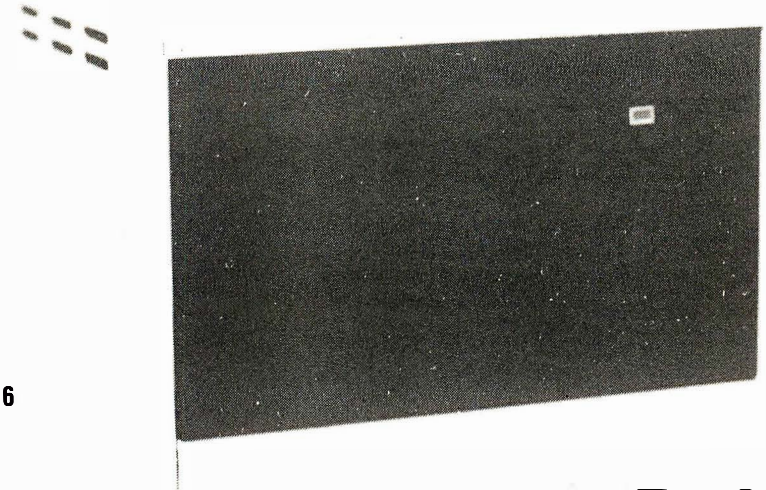
16,000,000 BYTES OF STORAGE

S-100 16MBYTE DMA HARAD DISK SUBSYSTEM

$1595.00

MORROW DESIGNS

SAVE OVER 45% !!



BPMDSDMAM16

There are price barriers to be broken, and then there are PRICE BARRIERS TO BE ***S-H-A-T-T-E-R-E-D!!*** Priority One Electronics prides itself on breaking price barriers — but never like the one you see here! We're talking about 16 ***M-E-G-A-B-Y-T-E-S*** FOR ONLY

$1595.00!!

That's the storage capacity of THIRTY TWO Shugart SA801Rs — at one tenth the price! And there can be no comparisons between the performance of this system and floppy disk drives!

PURE SPEED

That's what you get when you operate this subsystem. Imagine data access virtually without wait! By using DMA technology, the actual time required to send and retrieve data is greatly reduced. With the additional speed and high density of the 5¼" Winchester disk drive from COMPUTER MEMORIES, you will have enormous files at your own fingertips without the frustration of searching for the right floppy disk! The throughput of this subsystem is further increased by having all low level disk drive routines resident on the DMA controller, thus relieving the computer for other tasks.

COMPATIBILITY

MORROW DESIGNS engineers have invested thousands of man-hours to assure that this M16 hard disk subsystem will be compatible with almost all S-100 IEEE/696 computer systems. Each M16 hard disk subsystem is supplied with CP/M 2.2™, and MICROSOFT BASIC V5.2™. **MORROW DESIGNS** has even included an INSTALL program on 8" disk so you can easily custom configure your M16 subsystem to operate flawlessly with any system that is fully IEEE/696 compatible and has no other DMA devices on line.

EXPANDABLE

The M16 subsystem can grow with your needs. The DMA controller can operate up to four drives at one time. Just imagine — 64 MBytes on line! Also, as technologies progress, you will be prepared with a controller designed with the future in mind!

WITH CP/M 2.2™ AND MICROSOFT BASIC V5.2™!

NO KIDDING!

16,000,000 BYTES FOR

ONLY

$1595.00

SAVE $1400.00!!

KEY FEATURES:

DISK DRIVE:

- DISCUS M16. Computer Memories CMI5616, 16Mb formatted capacity
- Same physical size and mounting as the minifloppy
- Same DC voltages as the minifloppy
- Band actuator and stepper motor head positioning
- 5.0 megabit/second transfer rate
- Same track capacity as a double density 8 inch floppy
- 170 millisecond random average access time, reduceable to 95 ms via a simple software algorithm

CONTROLLER:

- Fully compatible with high speed 6MHz and 8 MHz CPUs of today and tomorrow
- DMA bus arbitration as outlined by the IEEE 696 standard
- Controls 1 to 4 soft sectored Winchester drives
- Variable sector length (256, 512, 1024, or 2048 byte sectors)
- Automatic CRC generation and checking
- Addresses 1 to 16 heads
- Addresses an infinite number of tracks
- 24-bit address burst DMA transfers
- Due to this high transferrate, a minimum CPU speed of 2.5MHz is required

DON'T WAIT!!!

WE HAVE ONLY A LIMITED QUANTITY THAT WILL BE AVAILABLE ON A FIRST COME FIRST SERVE BASIS!

AND THESE WON'T LAST LONG!

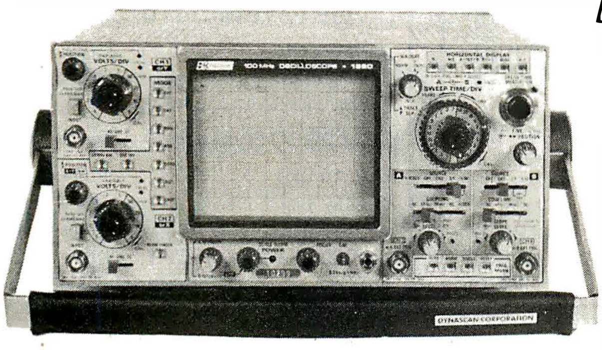
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NO ONE ELSE HAS LOWER SCOPE PRICES!

B+K PRECISION



SALE!!

2 Probes Included With Each Scope!



DIRECT FACTORY CONSUMER REBATE CERTIFICATE INCLUDED!

$75.00 REBATE!

$50.00 REBATE!

DUAL TIME BASE!
CALIBRATED DELAYED SWEEP!

- 100MHz BKP1590, 70MHz BKP1570
- 1mV/divison sensitivity
- 500 μV/division cascade sensitivity
- Four-input operation provides trigger view on 4 separate inputs
- Alternate time base operation
- 20 MHz bandwidth limiter CH1 & CH2
- Lighted function pushbuttons employing electronic switching with non-volatile RAM memory
- 8 x 10 cm internal graticule CRT
- Video sync separator standard
- Dual intensify controls
- Voltage and current probe calibrators (BKP1590 only)

B+K PRECISION

BKP1535 SPECIFICATIONS:
● 35MHz response; usable beyond 50 MHz ● 2 mV/cm vertical sensitivity ● Signal delay line for accurate view of high frequency pulse leading edge ● Alternate trigger capability ● Automatic or manual selection of CHOP AND ALTERNATE dual-trace display ● Variable hold-off for accurate pulse train display ● Video sync separators standard ● Built-in triggering filters ● PDA CRT with P31 phosphor ● 10:1/ref/direct probes included ● Differential input capability

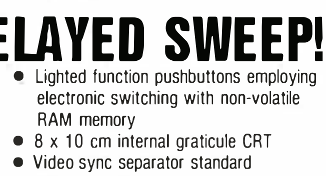
BKP1530 SPECIFICATIONS:
● Delayed sweep operation for sweep expansion up to 1000V ● 5 mV division sensitivity selectable 2 mV to 20MHz ● Variable hold-off pulse train display ● Single-sweep for nonrepetitive waveforms ● Built-in triggering filters ● Video sync separator standard ● CHOP or ALTERNATE display ● Differential input capability ● 11.7 nS rise time for short duration pulses ● Alternate trigger capability ● Front panel x-y operation ● 10:1/reference/direct probes included

100 MHz	70 MHz	35 MHz	30 MHz
8 TRACE - 4 CHANNEL	8 TRACE - 4 CHANNEL	DUAL TRACE - TRIGGERED	DUAL TRACE - DELAYED SWEEP
BPBKP1590 List Price: $1995.00	BPBKP1570 List Price: $1395.00	BPBKP1535 List Price $950.00	BPBKP1530 List Price: $875.00
$1449.00	**$995.00**	**$695.00**	**$625.00**
(Shipping Weight 18 lbs.)	(Shipping Weight 18 lbs.)	(Shipping Weight 20 lbs.)	(Shipping Weight 20 lbs.)
SAVE $546.00!!	**SAVE $400.00!!**	**SAVE $430.00!!** INCLUDING REBATE	**SAVE $301.00!!** INCLUDING REBATE

H-P QUALITY AND PERFORMANCE AT OUR *LOW* PRICES!

SERIES 10 - Programmable Calculators

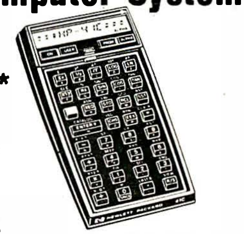
- RPN Logic
- Continuous Memory
- Convenient Design
- Automatic Turn-off Function
- LCD
- Self Diagnosis
- Rugged Construction



Part No.	Description	List Price	SALE
BP HP-10C	Scientific (Sh. Wt. 3 lbs.)	$ 70.00	$ 59.00
BP HP-11C	Advanced Scientific (3 lbs.)	$ 90.00	$ 79.00
BP HP-12C	Advanced Financial	$120.00	$ 99.00
BP HP-15C	Advanced Scientific w/matrices (3 lbs.)	$120.00	$ 99.00
BP HP-16C	For Digital Electronics and Computer Science (Sh. Wt. 3 lbs.)	$120.00	$ 99.00

HP-41C/CV - Handheld Computer System

HEWLETT PACKARD **SUPER LOW PRICES - FREE EXTRAS!***



Buy a Series 40 Computer or Peripheral and get an enhancement module FREE* — Up to a $125.00 Value! One Free Module with each Computer or Peripheral!

Buy one of these:

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BP HP82104A	Plug-in Card Reader (Sh. Wt. 5 lbs.)	$195.00	$159.00
BP HP82153A	Optical Wand (Sh. Wt. 5 lbs.)	$125.00	$ 99.00
BP HP82161A	Digital Cassette Drive (Sh. Wt. 5 lbs.)	$450.00	$349.00
BP HP82162A	Thermal Printer/Plotter (Sh. Wt. 5 lbs.)	$450.00	$349.00
BP HP82163A	Video Interface (Sh. Wt. 5 lbs.)	$225.00	$179.00

Get One of These Enhancement Modules FREE!*

BP HP82160A	HP-IL Module	$125.00	$59.00
BP HP82170A	Quad RAM	$ 75.00	$59.00
BP HP82180A	Extended Functions/Memory Module	$ 75.00	$59.00
BP HP82181A	Extended Memory Module	$ 75.00	$59.00
BP HP82182A	Time Module	$ 75.00	$59.00

*Each Computer or Peripheral is shipped with a coupon for free Enhancement Module direct from Hewlett-Packard (Offer expires 4/30/83).

HEWLETT PACKARD HP-75C Portable Computer



- Accepts 48K of applications ROM
- Touch-type typewriter-like keyboard
- Powerful BASIC Language
- Uses same peripherals as Series 40

BP HP-75C (Sh. Wt. 5 lbs.) List Price: $995.00

SALE PRICE: $849.00

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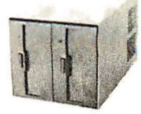
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S-100-4 MINI'S

Choose the System that fits your needs! A complete computer system ready to add on a terminal and printer. All Systems include CP/M® software and system manual set. Full six-month parts and labor warranty excluding drives which carry the full O.E.M. manufacturers warranty.

DUAL DRIVE SUBSYSTEMS





HORIZONTAL OR VERTICAL

Fully Assembled and Tested Units

w/two Shugart 801R SS/DD	$ 975.00
w/two Shugart 851R DS/DD	1225.00
w/two Siemans 120-8 SS/DD	675.00
w/two Qume DT-8 DS/DD	1250.00
w/two Tandon 848-1 SS/DD	995.00
w/two Tandon 848-2 DS/DD	1195.00
Cabinet A & T w/Power Supply and Accs.	235.00
Cabinet Top and Bottom	*Only*—69.50

California Computer Systems SPECIAL!

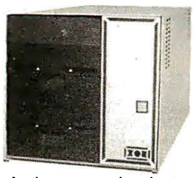
CCS SYSTEM 2410 . . $1995.00

- Includes CP/M® 2.2
- 2-Serial/1-Parallel Port
- DMA Disk Controller
- Hardware Vectored Interrupts
- 2-Real Time Clocks
- Supports CP/M®, MP/M®, OASIS

CCS 2300 System, A & T . . 1695.00

- 2810 CPU . . . . *Only*—255.00
- 2422 Disk Controller . . . . . . *Only*—330.00
- 2066 64K . . . . *Only*—360.00
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COMPLETE

- ★ with 48 TPI single sided double density 5¼" . . **$1395.00**
- ★ with 48 TPI double sided double density 5¼" . . **$1495.00**
- ★ with 96 TPI double sided double density 5¼" . . **$1650.00**

An inexpensive but powerful system featuring a 4 slot **S-100** bus chassis with the **XOR S-100** board set; 4-MHZ Z-80 CPU ★ 64K dynamic memory ★ multi-sector mixed density disk controller ★ 2-RS232 output ports in the rear for your terminal and printer ★ 3 eight-bit parallel ports on the CPU ready to add a cable and interface to your printer ★ All above systems are in stock ★ Includes CP/M® 2.2.

CP/M is a trademark of Digital Research

HARD DISK



Only $2995.00
COMPLETE

These **S-100-4** Systems may be very small in size (9"H x 9½"W x 18½"L) but look at the size of the ATASI® 5¼" Winchester hard disks we offer!

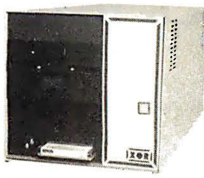
4 models to choose from

- ★ Seagate 5 Megabyte System **$2995.00**
- ★ #3020 15.6 Megabyte* System **$3495.00**
- ★ #3033 26 Megabyte* System **$3995.00**
- ★ #3046 36 Megabyte* System **$4495.00**

The above systems include a 96 TPI double sided double density 5¼" floppy as standard. The hard disk is controlled via Western Digital's controller for hard disks. Other features are the same as system at left.
*Megabyte sizes mentioned above are the available storage space after formatting.

TAPE BACKUP

WITH HARD DISK **Only $4250.00**
COMPLETE



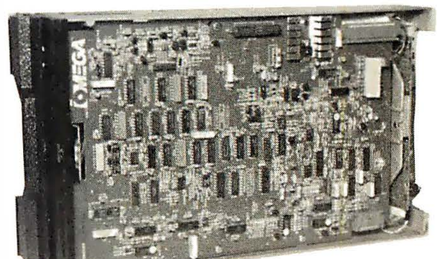
Now available through U.$ Micro Sales, the **XOR IRWIN 510 S-100-4** tape backup system with 10 megabytes of hard disk storage. Back up your hard disk on a mini-tape (we're talking 10 meg.) in less than 3½ minutes! The above system includes a 96 TPI DS/DD floppy drive and this system's modular design allows you to add a second floppy for only **$395.00**.

A MAJOR BREAKTHROUGH IN TECHNOLOGY . . .

IOMEGA™ CORP. ANNOUNCES THE ALPHA-10™



10 Megabyte Flexible Media Storage Sub-System



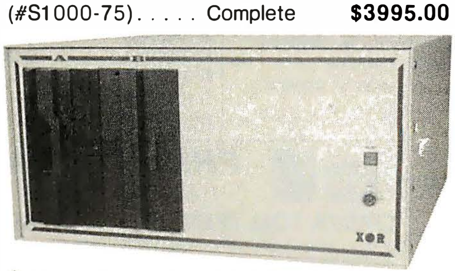
IOMEGA Technology

IOMEGA has combined the **reliability** of Winchester Technology with the **low cost removability** of flexible media recording to create a new generation of information storage technology. A unique system of media stabilization enables the flexible media to fly at close proximity to the head, resulting in high density, non-contact recording. Embedded servo and IOMEGA's Parity-Sector Error Correction further enhance the high density and data reliability achieved with the new technology. IOMEGA TECHNOLOGY is the step forward the industry has been awaiting.

Highest performance and reliability of any Removable Disk Drive. Lowest-cost 10 megabyte Disk Cartridge. More resistant to shock and vibration than any other Fixed or Removable Disk Drive. More resistant to contamination than any other Removable Disk Drive. Fastest start/stop (cartridge replacement) time of any high performance Disk Drive. Only Disk Cartridge Subsystem (drive, controller and cartridge) to dimensionally conform to the diskette standard. (size and mounting), i.e. identical size to Shugart 801/851.

Below is pictured XOR Data Science brand new S-100-12PLUS employing a fantastic 10 Meg floppy system. This new product is absolutely the greatest thing to hit the market in the last five years! Think of it, no more backup problems or head crash! 100 Meg of your data in the space the size of a shoe-box — and you can take it home with you. Call and ask for our folder before you buy your new computer system. It is definitely the best investment you can make.

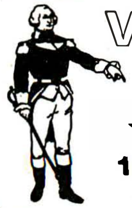
(#S1000-75) . . . . . Complete **$3995.00**



* Extra cartridges available (#M-2000-51). **$50.00**
ALPHA-10™ is a product manufactured by IOMEGA™ CORP.

IOMEGA Alpha 10

- 10 megabyte formatted capacity.
- Removable 10 megabyte flexible media cartridge.
- 1.13 megabyte/sec. data rate (instantaneous)
- 35 msec average access time.
- Low power: 35 watts including integrated controller.
- 8000 hours MTBF.
- Embedded servo for track following and track accessing.
- Parity-Sector Error Correction that insures non-recoverable data errors will be less than one in 10^{12} bits transferred to the host.
- Dimensions: Disk Drive 4.5" x 8.5" x 14.3" Cartridge ¾" x 8.23" x 11"



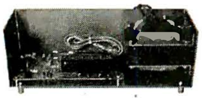
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In Ill. 1 (815) 485-4002 In Calif. 1 (714) 891-2677

TERMS: We accept VISA/MC, prepay, check or money order. Please allow personal check two weeks to clear before shipment. $5.00 handling charge on all orders under $50.00. 15% Restocking Fee. All orders shipped via U.P.S. unless otherwise specified. All UPS C.O.D. orders over $100.00 require a Cashiers Check. ★ Our products carry a full 6 months parts and labor warranty excluding drives, printers and terminals which carry the full O.E.M. factory warranty. PRICES SUBJECT TO CHANGE WITHOUT NOTICE.

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★ MADE IN U.S.A. BY AMERICANS ★

★ EAST ★ 11 Edison Drive, New Lenox, Illinois 60451
★ WEST ★ 6182 Garden Grove Blvd., Westminster, CA 92683

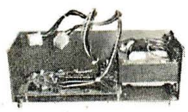
UNIVERSAL POWER SUPPLY



For Big Board, Apple or Aim 65
+5VDC @ 3 Amps
+12VDC @ .750 Amps
−12VDC @ .750Amps
−5VDC @ .500 Amps
Dimensions: 4" x 4" x 11"
$69.95

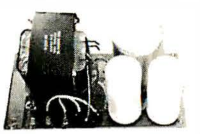
DISK DRIVE POWER SUPPLY

For 2 - 8" or 5" Drives
+ 5VDC @ 4 Amps
+24VDC @ 3 Amps
− 5VDC @ 1 Amp
AC Cables for 2 Drives **$7.50**
Dimensions: 4" x 4" x 11"



$59.95

S-100 POWER SUPPLY



+8VDC @ 30 Amps
+16VDC @ 6 Amps
−16VDC @ 6 Amps
PC Board Design
Dimensions: 5" x 6" x 11"
$89.50

TERMINALS

Televideo 910+ with green screen . . . **$575.00**
T.V. 925 . . . **739.00** T.V. 950 . . . **945.00**
Adds Viewpoint Model 3A+ **519.00**
Zenith Z-19 . . . . **740.00**

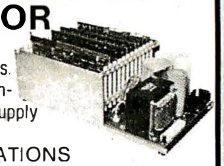
PRINTERS

Okidata 82A 80 Column **465.00**
Okidata 83A 132 Coulumn **745.00**
C-ITOH Prowriter I. **525.00**
I.D.S. Microprism Model 480 . . . . **565.00**
★★★★★★STAR MICRONICS★★★★★★
Gemini 10 Serial. . . . . **$130 OFF**
Gemini 10 Parallel. . . . . **120 OFF**
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8" DISK DRIVES

Shugart 801R . . . **$388.00ea.** Two for **$379.00ea.**
Shugart 851R . . . **535.00ea.** Two for **529.00ea.**
Qume DT-8. . . . **540.00ea.** Two for **529.00ea.**
Tandon 848-1 . . . **395.00ea.** Two for **388.00ea.**
Tandon 848-2 . . . **525.00ea.** Two for **519.00ea.**
Siemans 120-8 . . . **235.00ea.** Two for **225.00ea.**
All Shugart Drives now carry a full One year Parts and Labor Warranty!

S-100 MOD KIT
by XOR



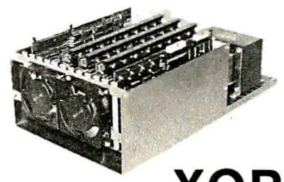
For test or systems applications. Complete **S-100** 12 Slot Mainframe with Disk Drive Power Supply for 4 Drives.

SPECIFICATIONS

Unregulated	Regulated
+8V @ 30A	+5V @ 5A
±16V @ 6A	+24V @ 3A
	−5V @ 1A

$225.00 Kit with 12 S-100 Bus Connectors
$255.00 Assem. and Tested with 12 Bus Connectors
$15.00 AC/DC Drive Cable Set for 2 Drives
Dimensions 6" x 10" x 18" — Shipping Weight 25 lbs.

Cooling Power
4 1/8"
Low Velocity Whisper® Fans
Only **$18.00** ea.
Finger Guards **$2.50** each.



XOR
S-100 MOD

CUSTOMER SERVICE HOTLINE 1 - (714) 898-5525

S-100-4



$1695.00

★ 4 Slot **S-100** Bus
★ Two Separate Power Supplys
★ **XOR S-100** Board Set
★ Inculdes CP/M® 2.2 and Manl
★ All Cables Provided
★ Dimensions only 9" x 9" x 18½"

S-100-4 System Complete with:
2-Tandon Thinline 8" (Model TM-848-1 SS/DD) Part#S-1000-40 . . . . **$1695.00**
2-Tandon Thinline 8" (Model TM-848-2 DS/DD) Part#S-1000-39 . . . . **$1950.00**

★★★SPECIAL OF THE MONTH★★★
8" Dual Drive Subsytem 1.2 Meg Includes two Siemans 120-8 SS/DD Drives, Cables, Power Supplies and Cabinet. A & T . . . . *Only*—**$675.00**

S-100-8



$1795.00

TERMINAL
★ Feather Touch Capacitance Kybrd
★ SOROC Type Screen Attribute Set
★ Half Intensity
★ 60 Key Standard ASCII
★ 8 Special Function Keys
★ 20 Screen Editing Keys

COMPUTER
★ **XOR S-100** Board set
★ Programmable Keyboard Set
★ Includes CP/M® 2.2
★ 8 Slot **S-100** Bus

S-100-8 System Complete With:
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Qume DT-8 Subsystem* (#S-1000-24) **2950.00**
Shugart SA 400 Minis (#S-1000-25) **2350.00**
Complete System, No Drives (#S-1000-21) . . **1795.00**
**Available in Horizontal or Vertical Cabinet*

S-100-12



$1350.00

★ With the **XOR S-100 MOD**
★ 12 Slot Motherboard and Card Cage
★ +8V @ 30A ★ ±16V @ 6A
★ DC Power to Run up to 4 Drives
★ **XOR S-100** Board set
★ Includes CP/M® 2.2 Software and Manual
★ All Cables Provided
★ Complete Manual Set

S-100-12 System Complete With:
2-Shugart 801R (#S-1000-30) . . . . **$ 2125.00**
2-Shugart 851R (#S-1000-31 . . . . **2425.00**
2-Qume DT-8 (#S-1000-32). **2450.00**
Complete System, no drives **1350.00**
Cabinet only - Includes Switches, Fan & AC/DC Wiring (#S-1000-28) **250.00**
Dimensions 11" x 21" x 22"
CP/M® is a trademark of Digital Research

Apple 8" Disk Controller Card **$395.00**
ZVX4 Dual Density, Single & Double Sided - Auto Boot Disk 2 + 2 Single Density Single or Dual Sided
SVA **300.00**
Complete line of add on drives for Apple
CALL TOLL FREE FOR PRICES

Ask about our Low Cost MODEM Software
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Novation - AUTOCAT Auto/Ans/Orig Direct Con. . . . **235.00**
Novation - APPLECAT 300/1200 Baud Direct Con. . . . **350.00**
PMMI - MM103 300/600 Baud (**S-100 BUS**) . . . **359.00**

SOFTWARE

BASIC 80 . . . . **$290.00**
BASIC COMPILER **320.00**
CALCSTAR. **150.00**
C BASIC **118.00**
C COMPILER **175.00**
MACRO ASSEMBLER **90.00**
MAILMERGE. **115.00**

4164 64K DYNAMIC 200 NS $5.95

TMM2016 2KX8 STATIC 200 NS $4.15

STATIC RAMS

2101	256 x 4 (450ns)	1.95
5101	256 x 4 (450ns) (cmos)	3.95
2102-1	1024 x 1 (450ns)	.89
2102L-4	1024 x 1 (450ns) (LP)	.99
2102L-2	1024 x 1 (250ns) (LP)	1.49
2111	256 x 4 (450ns)	2.49
2112	256 x 4 (450ns)	2.99
2114	1024 x 4 (450ns)	8/9.95
2114L-4	1024 x 4 (450ns) (LP)	8/12.95
2114L-3	1024 x 4 (300ns) (LP)	8/13.45
2114L-2	1024 x 4 (200ns) (LP)	8/13.95
2147	4096 x 1 (55ns)	4.95
TMS4044-4	4096 x 1 (450ns)	3.49
TMS4044-3	4096 x 1 (300ns)	3.99
TMS4044-2	4096 x 1 (200ns)	4.49
MK4118	1024 x 8 (250ns)	9.95
TMM2016-200	2048 x 8 (200ns)	4.15
TMM2016-150	2048 x 8 (150ns)	4.95
TMM2016-100	2048 x 8 (100ns)	6.15
HM6116-4	2048 x 8 (200ns) (cmos)	4.75
HM6116-3	2048 x 8 (150ns) (cmos)	4.95
HM6116-2	2048 x 8 (120ns) (cmos)	8.95
HM6116LP-4	2048 x 8 (200ns) (cmos)(LP)	5.95
HM6116LP-3	2048 x 8 (150ns) (cmos)(LP)	6.95
HM6116LP-2	2048 x 8 (120ns) (cmos)(LP)	10.95
Z-6132	4096 x 8 (300ns) (Qstat)	34.95

LP = Low Power Qstat = Quasi-Static

DYNAMIC RAMS

TMS4027	4096 x 1 (250ns)	1.99
UPD411	4096 x 1 (300ns)	3.00
MM5280	4096 x 1 (300ns)	3.00
MK4108	8192 x 1 (200ns)	1.95
MM5298	8192 x 1 (250ns)	1.85
4116-300	16384 x 1 (300ns)	8/11.75
4116-250	16384 x 1 (250ns)	8/11.95
4116-200	16384 x 1 (200ns)	8/12.95
4116-150	16384 x 1 (150ns)	8/14.95
4116-120	16384 x 1 (120ns)	8/29.95
2118	16384 x 1 (150ns) (5v)	4.95
4164-200	65536 x 1 (200ns) (5v)	5.95
4164-150	65536 x 1 (150ns) (5v)	6.95

5V = single 5 volt supply

EPROMS

1702	256 x 8 (1us)	4.50
2708	1024 x 8 (450ns)	3.95
2758	1024 x 8 (450ns) (5v)	5.95
2716	2048 x 8 (450ns) (5v)	3.95
2716-1	2048 x 8 (350ns) (5v)	5.95
TMS2516	2048 x 8 (450ns) (5v)	5.50
TMS2716	2048 x 8 (450ns)	7.95
TMS2532	4096 x 8 (450ns) (5v)	5.95
2732	4096 x 8 (450ns) (5v)	4.95
2732-250	4096 x 8 (250ns) (5v)	8.95
2732-200	4096 x 8 (200ns) (5v)	11.95
2764	8192 x 8 (450ns) (5v)	9.95
2764-250	8192 x 8 (250ns) (5v)	14.95
2764-200	8192 x 8 (200ns) (5v)	24.95
TMS2564	8192 x 8 (450ns) (5v)	17.95
MC68764	8192 x 8 (450ns) (5v)(24 pin)	39.95

5v = Single 5 Volt Supply

EPROM ERASERS

	Timer	Capacity Chip	Intensity (uW/Cm²)	
PE-14		6	5,200	83.00
PE-14T	X	6	5,200	119.00
PE-24T	X	9	6,700	175.00
PL-265T	X	20	6,700	255.00
PR-125T	X	16	15,000	349.00
PR-320	X	32	15,000	595.00

Z-80

2.5 Mhz

Z80-CPU	3.95
Z80-CTC	4.49
Z80-DART	10.95
Z80-DMA	14.95
Z80-PIO	4.49
Z80-SIO/0	16.95
Z80-SIO/1	16.95
Z80-SIO/2	16.95
Z80-SIO/9	16.95

4.0 Mhz

Z80A-CPU	4.95
Z80A-CTC	4.95
Z80A-DART	11.95
Z80A-DMA	16.95
Z80A-PIO	4.95
Z80A-SIO/0	16.95
Z80A-SIO/1	16.95
Z80A-SIO/2	16.95
Z80A-SIO/9	16.95

6.0 Mhz

Z80B-CPU	11.95
Z80B-CTC	13.95
Z80B-PIO	13.95
Z80B-DART	19.95

ZILOG

Z6132	34.95
Z8671	39.95

CRYSTALS

32.768 khz	1.95
1.0 mhz	4.95
1.8432	4.95
2.0	3.95
2.097152	3.95
2.4576	3.95
3.2768	3.95
3.579535	3.95
4.0	3.95
5.0	3.95
5.0688	3.95
5.185	3.95
5.7143	3.95
6.0	3.95
6.144	3.95
6.5536	3.95
8.0	3.95
10.738635	3.95
14.31818	3.95
15.0	3.95
16.0	3.95
17.430	3.95
18.0	3.95
18.432	3.95
20.0	3.95
22.1184	3.95
32.0	3.95

CRT CONTROLLERS

6845	14.95
68B45	35.95
HD46505SP	15.95
6847	12.25
MC1372	6.95
68047	24.95
8275	29.95
7220	99.95
CRT5027	39.95
CRT5037	49.95
TMS9918A	39.95
DP8350	49.95

KEYBOARD CHIPS

AY5-2376	11.95
AY5-3600	11.95

8000

8035	5.95
8039	6.95
INS-8060	17.95
INS-8073	24.95
8080	3.95
8085	5.95
8085A-2	11.95
8086	29.95
8087	CALL
8088	39.95
8089	89.95
8155	6.95
8155-2	7.95
8156	6.95
8185	29.95
8185-2	39.95
8741	39.95
8748	24.95
8755	24.95

8200

8202	24.95
8203	39.95
8205	3.50
8212	1.80
8214	3.85
8216	1.75
8224	2.25
8226	1.80
8228	3.49
8231	call
8237	19.95
8237-5	21.95
8238	4.49
8243	4.45
8250	10.95
8251	4.49
8253	6.95
8253-5	7.95
8255	4.49
8255-5	5.25
8257	7.95
8257-5	8.95
8259	6.90
8259-5	7.50
8271	39.95
8272	39.95
8275	29.95
8279	8.95
8279-5	10.00
8282	6.50
8283	6.50
8284	5.50
8286	6.50
8287	6.50
8288	25.00
8289	49.95

DISC CONTROLLERS

1771	16.95
1791	24.95
1793	26.95
1795	49.95
1797	49.95
2791	54.95
2793	54.95
2795	59.95
2797	59.95
6843	34.95
8272	39.95
UPD765	39.95
1691	17.95
2143	18.95

CONNECTORS

RS232 MALE	2.50
RS232 FEMALE	3.25
RS232 HOOD	1.25
S-100 ST	3.95

6800

68000	59.95
6800	3.95
6802	7.95
6808	13.90
6809E	19.95
6809	11.95
6810	2.95
6820	4.35
6821	3.25
6828	14.95
6840	12.95
6843	34.95
6844	25.95
6845	14.95
6847	11.95
6850	3.25
6852	5.75
6860	9.95
6862	11.95
6875	6.95
6880	2.25
6883	22.95
68047	24.95
68488	19.95

6800 = 1MHZ

68B00	10.95
68B02	22.25
68B09E	29.95
68B09	29.95
68B10	6.95
68B21	6.95
68B45	19.95
68B50	5.95

68B00 = 2 MHZ

6500

1 MHZ

6502	4.95
6504	6.95
6505	8.95
6507	9.95
6520	4.35
6522	7.95
6532	9.95
6545	22.50
6551	11.85

2 MHZ

6502A	6.95
6522A	9.95
6532A	11.95
6545A	27.95
6551A	11.95

3 MHZ

6502B	14.95

UARTS

AY3-1014	6.95
AY5-1013	3.95
AY3-1015	6.95
PT1472	9.95
TR1602	3.95
2350	9.95
2651	8.95
TMS6011	5.95
IM6402	7.95
IM6403	8.95
INS8250	10.95

GENERATORS

BIT-RATE

MC14411	11.95
BR1941	11.95
4702	12.95
COM5016	16.95
COM8116	10.95
MM5307	10.95

FUNCTION

MC4024	3.95
LM566	1.49
XR2206	3.75
8038	3.95

74LS00

74LS00	.24	74LS173	.69
74LS01	.25	74LS174	.55
74LS02	.25	74LS175	.55
74LS03	.25	74LS181	2.15
74LS04	.24	74LS189	8.95
74LS05	.25	74LS190	.89
74LS08	.28	74LS191	.89
74LS09	.29	74LS192	.79
74LS10	.25	74LS193	.79
74LS11	.35	74LS194	.69
74LS12	.35	74LS195	.69
74LS13	.45	74LS196	.79
74LS14	.59	74LS197	.79
74LS15	.35	74LS221	.89
74LS20	.25	74LS240	.95
74LS21	.29	74LS241	.99
74LS22	.25	74LS242	.99
74LS26	.29	74LS243	.99
74LS27	.29	74LS244	.99
74LS28	.35	74LS245	1.49
74LS30	.25	74LS247	.75
74LS32	.29	74LS248	.99
74LS33	.55	74LS249	.99
74LS37	.35	74LS251	.59
74LS38	.35	74LS253	.59
74LS40	.25	74LS257	.59
74LS42	.49	74LS258	.59
74LS47	.75	74LS259	2.75
74LS48	.75	74LS260	.59
74LS49	.75	74LS266	.55
74LS51	.25	74LS273	1.49
74LS54	.29	74LS275	3.35
74LS55	.29	74LS279	.49
74LS63	1.25	74LS280	1.98
74LS73	.39	74LS283	.69
74LS74	.35	74LS290	.89
74LS75	.39	74LS293	.89
74LS76	.39	74LS295	.99
74LS78	.49	74LS298	.89
74LS83	.60	74LS299	1.75
74LS85	.69	74LS323	3.50
74LS86	.39	74LS324	1.75
74LS90	.55	74LS352	1.29
74LS91	.89	74LS353	1.29
74LS92	.55	74LS363	1.35
74LS93	.55	74LS364	1.95
74LS95	.75	74LS365	.49
74LS96	.89	74LS366	.49
74LS107	.39	74LS367	.45
74LS109	.39	74LS368	.45
74LS112	.39	74LS373	.99
74LS113	.39	74LS374	.99
74LS114	.39	74LS377	1.39
74LS122	.45	74LS378	1.18
74LS123	.79	74LS379	1.35
74LS124	2.90	74LS385	1.90
74LS125	.49	74LS386	.45
74LS126	.49	74LS390	1.19
74LS132	.59	74LS393	1.19
74LS133	.59	74LS395	1.19
74LS136	.39	74LS399	1.49
74LS137	.99	74LS424	2.95
74LS138	.55	74LS447	.37
74LS139	.55	74LS490	1.95
74LS145	1.20	74LS624	3.99
74LS147	2.49	74LS640	2.20
74LS148	1.35	74LS645	2.20
74LS151	.55	74LS668	1.69
74LS153	.55	74LS669	1.89
74LS154	1.90	74LS670	1.49
74LS155	.69	74LS674	9.65
74LS156	.69	74LS682	3.20
74LS157	.65	74LS683	3.20
74LS158	.59	74LS684	3.20
74LS160	.69	74LS685	3.20
74LS161	.65	74LS688	2.40
74LS162	.69	74LS689	3.20
74LS163	.65	74LS783	24.95
74LS164	.69	81LS95	1.49
74LS165	.95	81LS96	1.49
74LS166	1.95	81LS97	1.49
74LS168	1.75	81LS98	1.49
74LS169	1.75	25LS2521	2.80
74LS170	1.49	25LS2569	4.25

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7400

7400	.19	74132	.45
7401	.19	74136	.50
7402	.19	74141	.65
7403	.19	74142	2.95
7404	.19	74143	2.95
7405	.25	74145	.60
7406	.29	74147	1.75
7407	.29	74148	1.20
7408	.24	74150	1.35
7409	.19	74151	.55
7410	.19	74152	.65
7411	.25	74153	.55
7412	.30	74154	1.25
7413	.35	74155	.75
7414	.49	74156	.65
7416	.25	74157	.55
7417	.25	74159	1.65
7420	.19	74160	.85
7421	.35	74161	.69
7422	.35	74162	.85
7423	.29	74163	.69
7425	.29	74164	.85
7426	.29	74165	.85
7427	.29	74166	1.00
7428	.45	74167	2.95
7430	.19	74170	1.65
7432	.29	74172	5.95
7433	.45	74173	.75
7437	.29	74174	.89
7438	.29	74175	.89
7440	.19	74176	.89
7442	.49	74177	.75
7443	.65	74178	1.15
7444	.69	74179	1.75
7445	.69	74180	.75
7446	.69	74181	2.25
7447	.69	74182	.75
7448	.69	74184	2.00
7450	.19	74185	2.00
7451	.23	74190	1.15
7453	.23	74191	1.15
7454	.23	74192	.79
7460	.23	74193	.79
7470	.35	74194	.85
7472	.29	74195	.85
7473	.34	74196	.79
7474	.33	74197	.75
7475	.45	74198	1.35
7476	.35	74199	1.35
7480	.59	74221	1.35
7481	1.10	74246	1.35
7482	.95	74247	1.25
7483	.50	74248	1.85
7485	.59	74249	1.95
7486	.35	74251	.75
7489	2.15	74259	2.25
7490	.35	74265	1.35
7491	.40	74273	1.95
7492	.50	74276	1.25
7493	.35	74279	.75
7494	.65	74283	2.00
7495	.55	74284	3.75
7496	.70	74285	3.75
7497	2.75	74290	.95
74100	1.75	74293	.75
74107	.30	74298	.85
74109	.45	74351	2.25
74110	.45	74365	.65
74111	.55	74366	.65
74116	1.55	74367	.65
74120	1.20	74368	.65
74121	.29	74376	2.20
74122	.45	74390	1.75
74123	.49	74393	1.35
74125	.45	74425	3.15
74126	.45	74426	.85
74128	.55	74490	2.55

LINEAR

LM301	.34	LM340 (see 7800)		LM566	1.49	LM1800	2.37
LM301H	.79	LM348	.99	LM567	.89	LM1812	8.25
LM307	.45	LM350K	4.95	NE570	3.95	LM1830	3.50
LM308	.69	LM350T	4.60	NE571	2.95	LM1871	5.49
LM308H	1.15	LM358	.69	NE592	2.75	LM1872	5.49
LM309H	1.95	LM359	1.79	LM709	.59	LM1877	3.25
LM309K	1.25	LM376	3.75	LM710	.75	LM1889	1.95
LM310	1.75	LM377	1.95	LM711	.79	LM1896	1.75
LM311	.64	LM378	2.50	LM723	.49	ULN2003	2.49
LM311H	.89	LM379	4.50	LM723H	.55	LM2877	2.05
LM312H	1.75	LM380	.89	LM733	.98	LM2878	2.25
LM317K	3.95	LM380N-8	1.10	LM741	.35	LM2900	.85
LM317T	1.19	LM381	1.60	LM741N-14	.35	LM2901	1.00
LM318	1.49	LM382	1.60	LM741H	.40	LM3900	.59
LM318H	1.59	LM383	1.95	LM747	.69	LM3905	1.25
LM319H	1.90	LM384	1.95	LM748	.59	LM3909	.98
LM319	1.25	LM386	.89	LM1014	1.19	LM3911	2.25
LM320(see 7900)		LM387	1.40	LM1303	1.95	LM3914	3.95
LM322	1.65	LM389	1.35	LM1310	1.49	LM3915	3.95
LM323K	4.95	LM390	1.95	MC1330	1.69	LM3916	3.95
LM324	.59	LM392	.69	MC1349	1.89	MC4024	3.95
LM329	.65	LM394H	4.60	MC1350	1.19	MC4044	4.50
LM331	3.95	LM399H	5.00	MC1358	1.69	RC4136	1.25
LM334	1.19	NE531	2.95	MC1372	6.95	RC4151	3.95
LM335	1.40	NE555	.34	LM1414	1.59	LM4250	1.75
LM336	1.75	NE556	.65	LM1458	.59	LM4500	3.25
LM337K	3.95	NE558	1.50	LM1488	.69	RC4558	.69
LM337T	1.95	NE561	24.95	LM1489	.69	LM13080	1.29
LM338K	6.95	NE564	2.95	LM1496	.85	LM13600	1.49
LM339	.99	LM565	.99	LM1558H	3.10	LM13700	1.49

H = TO-5 CAN T = TO-220 K = TO-3

RCA

CA 3023	2.75	CA 3082	1.65
CA 3039	1.29	CA 3083	1.55
CA 3046	1.25	CA 3086	.80
CA 3059	2.90	CA 3089	2.99
CA 3060	2.90	CA 3096	3.49
CA 3065	1.75	CA 3130	1.30
CA 3080	1.10	CA 3140	1.15
CA 3081	1.65	CA 3146	1.85
CA 3160	1.19		

TI

TL494	4.20	75365	1.95
TL496	1.65	75450	.59
TL497	3.25	75451	.39
75107	1.49	75452	.39
75110	1.95	75453	.39
75150	1.95	75454	.39
75154	1.95	75491	.79
75188	1.25	75492	.79
75189	1.25	75493	.89
75494	.89		

BI FET

TL071	.79	TL084	2.19
TL072	1.19	LF347	2.19
TL074	2.19	LF351	.60
TL081	.79	LF353	1.00
TL082	1.19	LF355	1.10
TL083	1.19	LF356	1.10
LF357	1.40		

CMOS

4000	.29	4527	1.95
4001	.25	4528	1.19
4002	.25	4531	.95
4006	.89	4532	1.95
4007	.29	4538	1.95
4008	.95	4539	1.95
4009	.39	4541	2.64
4010	.45	4543	1.19
4011	.25	4553	5.79
4012	.25	4555	.95
4013	.38	4556	.95
4014	.79	4581	1.95
4015	.39	4582	1.95
4016	.39	4584	.75
4017	.69	4585	.75
4018	.79	4702	12.95
4019	.39	74C00	.35
4020	.75	74C02	.35
4021	.79	74C04	.35
4022	.79	74C08	.35
4023	.29	74C10	.35
4024	.65	74C14	.59
4025	.29	74C20	.35
4026	1.65	74C30	.35
4027	.45	74C32	.39
4028	.69	74C42	1.29
4029	.79	74C48	1.99
4030	.39	74C73	.65
4034	1.95	74C74	.65
4035	.85	74C76	.80
4040	.75	74C83	1.95
4041	.75	74C85	1.95
4042	.69	74C86	.39
4043	.85	74C89	4.50
4044	.79	74C90	1.19
4046	.85	74C93	1.75
4047	.95	74C95	.99
4049	.35	74C107	.89
4050	.35	74C150	5.75
4051	.79	74C151	2.25
4053	.79	74C154	3.25
4060	.89	74C157	1.75
4066	.39	74C160	1.19
4068	.39	74C161	1.19
4069	.29	74C162	1.19
4070	.35	74C163	1.19
4071	.29	74C164	1.39
4072	.29	74C165	2.00
4073	.29	74C173	.79
4075	.29	74C174	1.19
4076	.79	74C175	1.19
4078	.29	74C192	1.49
4081	.29	74C193	1.49
4082	.29	74C195	1.39
4085	.95	74C200	5.75
4086	.95	74C221	1.75
4093	.49	74C373	2.45
4098	2.49	74C374	2.45
4099	1.95	74C901	.39
14409	12.95	74C902	.85
14410	12.95	74C903	.85
14411	11.95	74C905	10.95
14412	12.95	74C906	.95
14419	7.95	74C907	1.00
14433	4.18	74C908	2.00
4502	.95	74C909	2.75
4503	.65	74C910	9.95
4508	1.95	74C911	8.95
4510	.85	74C912	8.95
4511	.85	74C914	1.95
4512	.85	74C915	1.19
4514	1.25	74C918	2.75
4515	1.79	74C920	17.95
4516	1.55	74C921	15.95
4518	.89	74C922	4.49
4519	.39	74C923	4.95
4520	.79	74C925	5.95
4522	1.25	74C926	7.95
4526	1.25	74C928	7.95
		74C929	19.95

74S00

74S00	.32	74S163	1.95
74S02	.35	74S168	3.95
74S03	.35	74S169	3.95
74S04	.35	74S174	.95
74S05	.35	74S175	.95
74S08	.35	74S181	3.95
74S09	.40	74S182	2.95
74S10	.35	74S188	1.95
74S11	.35	74S189	6.95
74S15	.35	74S194	1.49
74S20	.35	74S195	1.49
74S22	.35	74S196	1.49
74S30	.35	74S197	1.49
74S32	.40	74S201	6.95
74S37	.88	74S225	7.95
74S38	.85	74S240	2.20
74S40	.35	74S241	2.20
74S51	.35	74S244	2.20
74S64	.40	74S251	.95
74S65	.40	74S253	.95
74S74	.50	74S257	.95
74S85	1.99	74S258	.95
74S86	.50	74S260	.79
74S112	.50	74S274	19.95
74S113	.50	74S275	19.95
74S114	.55	74S280	1.95
74S124	2.75	74S287	1.90
74S132	1.24	74S288	1.90
74S133	.45	74S289	6.89
74S134	.50	74S301	6.95
74S135	.89	74S373	2.45
74S138	.85	74S374	2.45
74S139	.85	74S381	7.95
74S140	.55	74S387	1.95
74S151	.95	74S412	2.98
74S153	.95	74S471	4.95
74S157	.95	74S472	4.95
74S158	.95	74S474	4.95
74S161	1.95	74S482	15.25
74S162	1.95	74S570	2.95
		74S571	2.95

INTERFACE

8T26	1.59
8T28	1.89
8T95	.89
8T96	.89
8T97	.89
8T98	.89
DM8131	2.95
DP8304	2.29
DS8835	1.99
DS8836	.99

MISC.

ULN2003	2.49
3242	7.95
3341	4.95
MC3470	4.95
MC3480	9.00
11C90	13.95
95H90	7.95
2513-001 UP	9.95
2513-002 LOW	9.95

VOLTAGE REGULATORS

7805T	.75	7905T	.85
7808T	.75	7908T	.85
7812T	.75	7912T	.85
7815T	.75	7915T	.85
7824T	.75	7924T	.85
7805K	1.39	7905K	1.49
7812K	1.39	7912K	1.49
7815K	1.39	7915K	1.49
7824K	1.39	7924K	1.49
78L05	.69	79L05	.79
78L12	.69	79L12	.79
78L15	.69	79L15	.79
78H05K	9.95	LM323K	4.95
78H12K	9.95	UA78S40	1.95

T = TO-220 K = TO-3
L = TO-92

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MM5369	3.95
MM5375	4.95
MM58167	8.95
MM58174	11.95
MSM5832	6.95

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ICL7103	9.50
ICL7106	9.95
ICL7107	12.95
ICL7660	2.95
ICL8038	3.95
ICM7207A	5.59
ICM7208	15.95

9000

9316	1.00
9334	2.50
9368	3.95
9401	9.95
9601	.75
9602	1.50
96S02	1.95

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XR 2206	3.75
XR 2207	3.75
XR 2208	3.75
XR 2211	5.25
XR 2240	3.25

DATA ACQUISITION

ADC0800	15.55	DAC0808	2.95
ADC0804	3.49	DAC1020	8.25
ADC0809	4.49	DAC1022	5.95
ADC0817	9.95	MC1408L6	1.95
DAC0800	4.95	MC1408L8	2.95

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AY3-8910	12.95
AY3-8912	12.95
MC3340	1.49

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CAPACITORS

TANTALUM

	6V	10V	15V	20V	25V	35V	50V
.22uf						.40	
.27						.40	
.33						.40	.45
.47				.35			.50
.68						.45	.50
1.0			.40	.40	.45	.45	
1.5				.45		.50	.60
1.8							.75
2.2		.35	.40	.45		.65	.85
2.7		.40	.45				.90
3.3		.45	.50	.55	.60	.65	.90
3.9		.45					
4.7	.45	.55		.60	.65	.85	.90
6.0			.60				
6.8			.70		.75		
8.2							1.00
10	.55	.65	.80	.85	.90	1.00	
12	.65		.85	.90			
15	.75	.85	.90				
18			1.25				
22		1.00	1.35				
27			2.25				
39		1.50					
47	1.35						
56	1.75						
100		3.25					
270	3.75						

DISC

10pf	50V	.05	470	50V	.05
22	50V	.05	560	50V	.05
25	50V	.05	680	50V	.05
27	50V	.05	820	50V	.05
33	50V	.05	.001uf	50V	.05
47	50V	.05	.0015	50V	.05
56	50V	.05	.0022	50V	.05
68	50V	.05	.005	50V	.05
82	50V	.05	.01	50V	.07
100	50V	.05	.02	50V	.07
220	50V	.05	.05	50V	.07
330	50V	.05	.1	12V	.10
			.1	50V	.12

MONOLITHIC

.1uf-mono 50V .18   .47uf-mono 50V .25

ELECTROLYTIC

RADIAL			AXIAL		
.47uf	50V	.14	1uf	50V	.14
1	25V	.14	4.7	16V	.14
2.2	35V	.15	10	16V	.14
4.7	50V	.15	10	50V	.16
10	50V	.15	22	16V	.14
47	35V	.18	47	50V	.20
100	16V	.18	100	15V	.20
220	35V	.20	100	35V	.25
470	25V	.30	150	25V	.25
2200	16V	.60	220	25V	.30
			330	16V	.40
			500	16V	.42
			1000	16V	.60
			1500	16V	.70
			6000	16V	.85

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26,000uf 30V 3.95

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P100-3	Vertical BUSS	22.95
P100-4	Single Foil Pads Per Hole	23.95

APPLE

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IBM-PR	BUSS Lines + Pads	55.00

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36/72 PIN (.1" SPACING)

P721-3	Vertical BUSS, 4.5" x 6"	13.95
P722-3	Vertical BUSS, 4.5" x 9"	14.95

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OPTO-ISOLATORS

4N26	1.00	MCA-7	1.50
4N27	1.10	MCA-255	1.75
4N28	.69	IL-1	1.25
4N33	1.75	ILA-30	1.25
4N35	1.25	ILQ-74	2.75
4N37	1.25	H11C5	1.25
MCT-2	1.00	TIL-111	1.00
MCT-6	1.50	TIL-113	1.75

DIODES

1N751	5.1 volt zener	.25
1N759	12.0 volt zener	.25
1N4148	(1N914) switching	25/1.00
1N4004	400PIV rectifier	10/1.00
KBP02	200PIV 1.5amp bridge	.45
KBP04	400PIV 1.5amp bridge	.55

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3.125" Square	14.95

SWITCHES

SPDT mini-toggle	1.25
DPDT mini-toggle	1.50
SPDT push-button	1.49

TRANSISTORS

2N918	.50	MPS3706	.15
MPS918	.25	2N3772	1.85
2N2102	.50	2N3903	.25
2N2218	.50	2N3904	.10
2N2218A	.50	2N3906	.10
2N2219	.50	2N4122	.25
2N2219A	.50	2N4123	.25
2N2222	.25	2N4249	.25
PN2222	.10	2N4304	.75
MPS2369	.25	2N4401	.25
2N2484	.25	2N4402	.25
2N2905	.50	2N4403	.25
2N2907	.25	2N4857	1.00
PN2907	.125	PN4916	.25
2N3055	.79	2N5086	.25
3055T	.69	PN5129	.25
2N3393	.30	PN5139	.25
2N3414	.25	2N5209	.25
2N3563	.40	2N6028	.35
2N3565	.40	2N6043	1.75
PN3565	.25	2N6045	1.75
MPS3638	.25	MPS-A05	.25
MPS3640	.25	MPS-A06	.25
PN3643	.25	MPS-A55	.25
PN3644	.25	TIP29	.65
MPS3704	.15	TIP31	.75
		TIP32	.79

HEAT-SINKS

TO-3 style	.95
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IC SOCKETS

	1-99	100
8 pin ST	.13	.11
14 pin ST	.15	.12
16 pin ST	.17	.08
18 pin ST	.20	.18
20 pin ST	.29	.27
22 pin ST	.30	.27
24 pin ST	.30	.27
28 pin ST	.40	.32
40 pin ST	.49	.39
64 pin ST	4.25	call
ST = SOLDERTAIL		
8 pin WW	.59	.49
14 pin WW	.69	.52
16 pin WW	.49	.49
18 pin WW	.99	.90
20 pin WW	1.09	.98
22 pin WW	1.39	1.28
24 pin WW	1.49	1.35
28 pin WW	1.69	1.49
40 pin WW	1.99	1.80
WW = WIREWRAP		
16 pin ZIF	6.75	call
24 pin ZIF	9.95	call
28 pin ZIF	10.95	call
ZIF = TEXTOOL (Zero Insertion Force)		

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MAN 74	.3"	CC	.99
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FND-507 (510)	.5"	CA	1.49

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- ★ DIMENSIONS 8⅝ x 5¹⁵⁄₁₆ x 3¹⁵⁄₁₆"
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- ★ INCLUDES MOUNTING HARDWARE AND FEET

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- ★ +5V @ 1 AMP, +12V @ 1.5 AMP
- ★ FITS STANDARD 5¼" DRIVES
- ★ PLEASE **SPECIFY** GRAY OR TAN

NOTE: Please include sufficient amount for shipping on above items.

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SA400 $189.95

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COMPONENTS

LM1488 or LM1489	.69 ea.	7805T or 7812T	.75 ea.
16 PIN LOW PROFILE ST IC SOCKETS			100/8.00
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RS232 FEMALE RIGHT ANGLE	5.25
RS232 HOOD	1.25
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S-100 WW	4.95
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44 pin WW	4.95
72 pin ST	6.95
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CONTACTS	SINGLE COLOR 1'	SINGLE COLOR 10'	COLOR CODED 1'	COLOR CODED 10'
10	.50	4.40	.83	7.30
20	.65	5.70	1.25	11.00
26	.75	6.60	1.32	11.60
34	.98	8.60	1.65	14.50
40	1.32	11.60	1.92	16.80
50	1.38	12.10	2.50	22.00

D-SUBMINIATURE

DESCRIPTION	SOLDER MALE	SOLDER FEMALE	RIGHT ANGLE SOLDER MALE	RIGHT ANGLE SOLDER FEMALE	RIBBON CABLE MALE	RIBBON CABLE FEMALE	HOODS BLACK	HOODS GREY
ORDER BY	DBxxP	DBxxS	DBxxPR	DBxxSR	IDBxxP	IDBxxS	HOOD-B	HOOD
CONTACTS 9	2.08	2.66	1.65	2.18	3.37	3.69	—	1.60
15	2.69	3.63	2.20	3.03	4.70	5.13	—	1.60
25	2.50	3.25	3.00	4.42	6.23	6.84	1.25	1.25
37	4.80	7.11	4.83	6.19	9.22	10.08	—	2.95
50	6.06	9.24	—	—	—	—	—	3.50

For order instructions see "IDC Connectors" below.

IDC CONNECTORS

DESCRIPTION	SOLDER HEADER	RIGHT ANGLE SOLDER HEADER	WW HEADER	RIGHT ANGLE WW HEADER	RIBBON HEADER SOCKET	RIBBON HEADER	RIBBON EDGE CARD
ORDER BY	IDHxxS	IDHxxSR	IDHxxW	IDHxxWR	IDSxx	IDMxx	IDExx
CONTACTS 10	.82	.85	1.86	2.05	1.15	—	2.25
20	1.29	1.35	2.98	3.28	1.86	5.50	2.36
26	1.68	1.76	3.84	4.22	2.43	6.25	2.65
34	2.20	2.31	4.50	4.45	3.15	7.00	3.25
40	2.58	2.72	5.28	4.80	3.73	7.50	3.80
50	3.24	3.39	6.63	7.30	4.65	8.50	4.74

ORDERING INSTRUCTIONS: Insert the number of contacts in the position marked "**xx**" of the "order by" part number listed. **Example:** A 10 pin right angle solder style header would be IDH**10**SR.

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From the Keyboard Co.

- ★ Brand New Rev. 7 keyboard — NOT an imitation
- ★ Special Purchase — Supply very limited
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- ★ Simple to use — Yet supports custom driver applications from ROM or Disk
- ★ Includes card, cable and user's manual
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- ★ 1 Year Warranty

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Circle 224 on inquiry card.

Unclassified Ads

WANTED: A French computer science student who has experimented both with minicomputers, Apples, TRS-80s and programming in COBOL, BASIC, ASM seeks a computer-related vacation in the U.S. from July through September 1983. Marchal Patrick, 56 A route de Schirmeck 67200, Strasbourg, France.

WANTED: An owner of an Apple 48K CP/M who is a French computer science student seeks people willing to correspond and to exchange software ideas. Holtzmann Thierry, 24 Grand Rue 68320, Urschenheim, France.

WANTED: A position in a U.S. computer company during the summer of '83 is sought by a French computer science student with experience in CP/M, minicomputers, COBOL, BASIC, FORTRAN, Pascal, Assembler, and PL/1. Meyer Eric, 2 rue Lamartine 68460, Lutterbach, France.

WANTED: Tax-deductible contribution of any home computer equipment to a nonprofit youth organization for use by a disabled teenager in our program. Dan Seidel, Youth Advocates, Foster Care Program, 2317 East John, Seattle, WA 98112, (206) 322-7838.

WANTED: Consider a tax-deductible donation by yourself or your company of obsolete but functional hardware and/or software. Tax-exempt nonprofit historical-preservation organization in archaeology needs data processing, word processing, and accounting capabilities. Our references and IRS information on request. Darrell Fulmer, Mitchell National Historic Landmark, 305 Medical Arts Building, POB 621, Mitchell, SD 57301, (605) 996-5473.

WANTED: A microcomputer user interested in spending a holiday in Italy for free. I am interested in computer science: studying microelectronics, programming mostly in Pascal, and own an Apple II Plus. I will graduate from the University of Turin. He/she will offer me an equal holiday in the States. Send a short curriculum vitae. Roberto Tonetti, POB 9, Brusnengo, VC 13060, Italy.

FOR SALE: Texas Instruments 745 terminals, used. Russ White, (212) 997-6075.

WANTED: New Apple owner would like to purchase back issues of Nibble. Needed are all of volume 1 and all of volume 2 except No. 6. Please send list of available issues and prices requested. Bob Steinberg, 9030 Niles Center Rd., Skokie, IL 60076.

FOR SALE: Full ASCII keyboard, $50; Dynabyte naked terminal board (Model 57), $150; Processor Technology 3 parallel and serial I/O board, $150; New SDS Expandoram 64K board, 150 ns, $400. New DRC 16K EPROM board, $175. Send cashier's check or money order plus $5 shipping and handling per board. William Whitney, 2063-43rd Ave., San Francisco, CA 94116.

FOR SALE: IMSAI S-100 system includes DIO-C, VIO-C, MPU-B, RAM 64, in a 10-slot mainframe; monitor; keyboard; and two sets of Persci dual 8-inch drives. Purchased new in 1981, scarcely used, $3200 firm. Will sell system with one set of dual 8-inch drives for $2500, or one set of drives for $700. Greg Baker, POB 3044, Clinton, IA 52732.

WANTED: Ideas for interesting but not too complex games that I can write for personal use. Games can be of any type. I don't want listings, just ideas. Games will be written for the Commodore VIC-20. A copy of the finished project will be mailed to sender on request. David Alexander, 1667 Midland Dr., East Meadow, NY 11554.

FOR SALE: First 16 issues of BYTE (September 1975 through December 1976). This includes charter issue, #1. Like-new condition. Best offer over $80. Paul Silagi, 83 Needletree Lane, Glastonbury, CT 06033.

FOR SALE: Sinclair ZX81 8K ROM/16K RAM with full-size typewriter-style keyboard, like new. Have many programs including assembler/disassembler, graphics utility, and games. Will include these programs free with purchase of computer. Best offer. R. Beaber, 803 Euclid, Centralia, WA 98531.

WANTED: Used ZX81 microcomputer in good condition. Derry Bryson, POB 433, Wendell, ID 83355.

FOR SALE: Apple II Plus with 64K RAM. System includes 48K computer (Revision 7), Microsoft Ramcard, Apple II disk with controller, Sup 'R' Mod II, Videx Keyboard Enhancer II, E-Z Port (adds game I/O socket outside computer), all cables and manuals, and over 40 program-filled disks worth over $1500. Best offer. Also, have Integer Firmware card with old monitor ROM. Best offer. Jonothon Cone, 7921 Garner St., Long Beach, CA 90808, (213) 596-5228.

WANTED: Manuals or tapes with program listings for Central Data Co. 2650 BASIC interpreter, 8K and/or extended version. Also, want other Central Data information and documentation, such as manuals/listings for debugger, editor/assembler, assembly-language package, character generator program, disk-operating system, printer interface, etc. G.A. Luce, 2907 Greenlawn Parkway, Austin, TX 78757.

WANTED: Commodity Trading Systems. I am a marketing genius without a system, looking for a programming genius without a market. System must be fully developed, previously unmarketed, extensively tested, and extraordinarily successful. Send details and financial requirements. Hugh Martin, 305 San Anselmo Ave., San Anselmo, CA 94960.

WANTED: Apple II peripherals. Modem, double-density disk drive, color monitor, printer buffer, 80-column board, letter-quality printer, etc. Will trade for what you need. I am a member of a barter/exchange: tell me what you have and what you want. Walter Bristow, Box 11278, Eugene, OR 97440, (503) 485-7001 or 741-1464.

FOR SALE: AIM 65 with Video 1 board, power supply, 16K of memory, and case. Asking $500. Joe Hootman, 3022 Clover Dr., Grand Forks, ND 58201, (701) 775-8353.

FOR SALE: HP 9845A computer, 16-bit microprocessor, 62K-byte core memory, high-resolution display, built-in printer, two cassette tape I/O, graphics, 4 years old, excellent condition, original price about $21,000, asking $6000. R.O. Prindle, 54 Crest Rd., Piedmont, CA 94611, (415) 845-3800 days.

FOR SALE: Z80 Starter Kit with 2K RAM in good condition, $200. Also, several Tektronix and Hewlett-Packard oscilloscopes, not working: $50 each. Also, assorted test equipment; send SASE for complete list. Bill Stottlemyer, Rt. 1, Box 125, Corinth, MS 38834.

FOR SALE: PRIAM 15450, 150-MB disk drive, SMART-E controller, power supply and rack slides, all new in the box: $6200. New Shugart SA-400 disk drive: $100. Old SD Sales 4K memory boards: $10 each. Polymorphics 64 by 16 S-100 video board, new factory-assembled and -tested: $20. Jim Amick, 3009 Collin Court, Plano, TX 75075, (214) 596-3788 evenings.

FOR SALE: Commodore 2001 computer with 32K and assorted software. Also, Commodore 8050 dual-disk drive and Commodore cassette drive. All in mint condition. Items sold individually or as a set. Make an offer. Donald Lemma, POB 130, Holmdel, NJ 07733, (201) 946-8735.

WANTED: To complete my collection of BYTE I need November 1978 and November 1977. In return, I offer BYTE 1976: Numbers 13, 14, 15, 16, and BYTE 1977: Numbers 8 and 10. I am also interested in back issues of Creative Computing, Interface Age, Radio Electronics, and Popular Electronics. Jaroslav Budinsky, Palackeho 956, 282 01 Cesky Brod, Czechoslovakia.

WANTED: I would like to correspond with someone familiar with both Centronics 700 series printers and Data General equipment, mainly Dasher D-200 video displays. Kleber Vianna, 440 Park Ave. S, Apt. 1317, New York, NY 10016, (212) 686-2206.

FOR SALE: Godbout S-100 boards: RAM 20 (32K), $225; Interfacer I (two serial I/O), $140; Spectrum with 8105 routine for Epson parallel and Sublogic 2D and 3D software, $225. Heath H-14 printer, $250. Zenith green monitor, $95. All perfect. Jack Hersh, (415) 549-3257.

WANTED: SOL units and 5¼-inch floppy-disk readers for use and replacement parts. Tax-deductible donations are most welcome. Mr. Walter Hoy, Principal, Campolindo High School, 300 Moraga Rd., Moraga, CA 94556.

WANTED: 9-inch black-and-white Panasonic video monitor (TR-930), in good condition; $125 or best offer. HP-34C advanced programmable scientific calculator with continuous memory, owner's handbook, mathematics and statistics applications books; $70 or best offer. David Body, 1530 Cambridge St. #2, Cambridge, MA 02139.

WANTED: Documentation on programming home video game cartridges for the Atari VCS, Intellivision, etc. Particularly interested in schematics and instruction manuals for the discontinued Magicard module advertised page 450 August 1981 BYTE. Will cover your shipping and printing costs. Rick Roberson, 903 Danville Circle, Knoxville, TN 37923, (615) 690-7765.

FOR SALE: BYTE collection: second issue through current issue. All are in excellent condition with over 80 issues. $120 plus cost of shipping. J.D. Gray, 6951 North Oatman Ave., Portland, OR 97217, (503) 289-6783. No collect calls.

FOR SALE: 32K Commodore PET with display, 40 columns, and cassette. Includes many programs and games. Asking $900 plus shipping. Peter Giroux, 2820 Route 158, Ste. Sophie, Quebec, Canada, (514) 436-7214.

WANTED: Atari computer games or other software to swap. Send name, address, and cassette and I'll return different programs. Jim Klein, 1552 Woodbridge Apt. 210, St. Paul, MN 55117.

FOR SALE: OSI C1P, 32K static RAM, disk drive, Model 35 Teletype software includes OS65D operating system (V 3.1 and V 3.3), HEXDOS, S-FORTH, Assembler, Extended Monitor, games, and applications: $750 or best offer. Computerist Video plus board, new: $150. Steve McCaughey, 524 East Broadway, Enid, OK 73701, (405) 242-2606, weekends only.

FOR SALE: RCA VP711 microcomputer with 4K static RAM, RF modulator, three programming manuals, game manual, power supply, all necessary cables, hex keypad, CHIP-8, CHIP-8X, and many games on cassette tape. Will sell for $140 or will trade for a working Shugart 801 disk drive. Tom Babaian, 1450 Beaver Rd., Southampton, PA 18966.

WANTED: New or used Atari 800 with 16K RAM or more. Manuals must be included. Would also like extra peripherals such as the 810 disk drive, Epson MX100 printer (or similar), color monitor, languages, joysticks, paddles, lightpen, or games, etc. Will cover shipping if in Western U.S. Make offer on package. Timothy Hood, 17698 Walnut St., Fountain Valley, CA 92708, (714) 964-7206.

UNCLASSIFIED POLICY: Readers who have computer equipment to buy, sell, or trade or who are requesting or giving advice may send a notice to BYTE for inclusion in the Unclassified Ads section. To be considered for publication, an advertisement must be noncommercial (individuals or bona fide computer clubs only), typed double-spaced on plain white paper, contain 75 words or fewer, and include complete name and address. This service is free of charge; notices are printed once only as space permits. Your confirmation of placement is appearance in an issue of BYTE as we engage in no correspondence. Please allow at least three months for your ad to appear. Send your notices to Unclassified Ads, BYTE/McGraw-Hill, POB 372, Hancock, NH 03449.

Unclassified Ads

FOR SALE: TRS-80 Model III with two double-sided double-density disk drives; RS-232C interface; Daisy Wheel 2 printer; NEWDOS-80; Scripsit/QWERTY word processor; Scripsit Dictionary; other assorted software including mailing lists, utility programs, and several games. Less than one year old. Get the works for only $3750. Ron Jones, (801) 966-6879.

FOR SALE: Heath H-8 computer, 24K, 4-port serial I/O board (H-8-4), and serial/cassette interface board (H-8-5). Includes all manuals: $250. Ralph Seiler, 70 East Sunset Ave. #1, Salt Lake City, UT 84115, (801) 484-6808.

FOR SALE: Digital Research PL/I (unopened) with update and manuals for 8-bit system, $350. Visicalc and FORTRAN with manuals for TRS-80 Model I, $50 each. Omikron Mapper II (unused) for TRS-80 Model I, $100. IBM 735 I/O Selectric, black (excellent condition), modified for TRS-80 Model I by Virginia Microsystems, operates as printer or typewriter, $450. Syd Spain, POB 10107, College Station, TX 77840, (713) 693-2835.

FOR SALE: NEC Spinwriter 7710, with tractor, new, $2200. IBM PC asynchronous communications, $100. Ron Swenson, Box 701, Boston, MA 02102, (617) 242-9213, evenings.

WANTED: Users of IBM 5100, 5110, or 5120 or users group to exchange information. I also want to purchase a spreadsheet-type program for this model. Stephen Pottie, POB 697, Montague, Prince Edward Island C0A 1R0, Canada, (902) 838-2070 or 962-2279.

FOR SALE: Teletype Model 43 30-cps dot-matrix printer terminal. RS-232C interface, pinfeed, Hall-effect keyboard. Almost new condition. With service and circuit diagram manuals: $595. Ron Mauceri, 14433 Dickens St., Sherman Oaks, CA 91423, (213) 906-3517.

WANTED: Consultant to aid in implementation of dial-up database system. Dr. L. Huber, Hampshire Educational Collaborative, 58 Pleasant St., Northampton, MA 01060.

FOR SALE: Novation Cat modem, 300 bps, good condition: $100 or best offer. Jim Larus, Apt. 4, 2415 College Ave., Berkeley, CA 94704.

WANTED: Commodore 64 owners, send me your games, music, or graphics programs on cassette, with your name and address, and I'll send back your cassette with my adventure game, "Horror Hotel." Would also like to correspond with anyone using the Commodore 64 for music synthesis. Phil Nelson, 3801 Garfield Ave. S, Minneapolis, MN 55409.

FOR SALE: Radio Shack Line Printer IV (same as Centronics 747) in excellent condition. Highest offer or best trade-in bid for daisy-wheel printer, new or used. Isai Kamen, 11 Sherman Ave., White Plains, NY 10605.

FOR SALE: Atari 800, new: $670 COD. Also, every computer magazine available. Send SASE. Jack Gindi, REF301, 2079 East 3 St., Brooklyn, NY 11223.

WANTED: I am interested in obtaining the following publications: PC—The Independent Guide to IBM Personal Computers—Vol. 1, No. 2, 80 Microcomputing—Vol. 2, No. 2 (February 1981). Send asking price. Thomas Kariya, POB 33, Brookeville, MD 20833.

FOR SALE: Back issues of BYTE, January '81, July '81 through July '82: $10. Nat Stevens, 46 Elm St., North Andover, MA 01845, (617) 687-3421.

FOR SALE: Radio Shack Color Computer plastic dust cover, $4 with Radio Shack Cassette recorder cover. Also, would like a copy of Eliza written in Microsoft BASIC under 20K. Send price. Bosco T. Tsang, 575 University Ave. W #505, Windsor, Ontario N9A 5R4, Canada.

FOR SALE: SwTPC 6800 with 28K RAM socketed for 48K, three serial I/O ports, LFD-400 disk drive with INDEX DOS, CT-64 terminal with VT-VM green screen monitor and software: $1400. Jim Benson, 1719 North Woodlawn, Derby, KS 67037, (316) 788-5756.

FOR SALE: ABT Softkey pad for Apples. Accessory-programmable keypad plugs into game port. Can be used as numeric pad or keys may be programmed as command keys. With all documentation, like new (never used). First $100 takes. Evan Julber, Numismatics Ltd., Suite 600, 9665 Wilshire Blvd., Beverly Hills, CA 90212, (800) 421-0678 or (213) 550-1766.

FOR SALE: S-100 boards. Flashwriter II, $150. Cromemco Bytesaver, $100. IMSAI SIO, $25. Processor Technology: PROM board, $50; CUTS, $25; VDM-1 video, $25. Tarbell cassette I/O, $25. Percom cassette I/O, $25. Jay Dowling, 804 Bristol Court, Richardson, TX 75080, (214) 690-1752.

FOR SALE: 32K Commodore PET with interfacing and software to control lights, motors, etc. Many games. Asking $400 or best offer. Ed Jemmings, 688 Ida-Maybee Rd., Monroe, MI 48161, (616) 269-2133.

FOR SALE: TRS-80 Color Computer, 32K Ext. BASIC, original packing. Plus approximately $400 worth of software, including CBUG, Editor/Assembler, Colorcom(E) V3, Telewriter Word-processor, Space Invaders, Asteroids, Pacman, Berserk, Chess, and many more. Includes manuals. Asking $525. J.A. Czyryca, 6014 County Line Rd., Perry, NY 14530.

FOR SALE: Universal Data Systems 212LP: 1200 bps, direct-connect, full-duplex modem. New, in original carton, never used. List price is $495, will sell for $300 (postpaid), or best offer. Harold Miller, Tumbling Waters, Route 2, Box 2330, Clayton, GA 30525, (404) 782-2843.

FOR SALE: Commodore VIC-20 Color Computer with these extras: 8K memory cartridge, Commodore cassette player, joystick, three games, and two instruction books. All like new. $225 or trade for accessories and equipment for my TRS-80 Color Computer. Hal Mermelstein, RFD 2, Webb Rd., South Windham, ME 04082, (207) 892-9042.

FOR SALE: Qume Sprint 5 daisy-wheel printer in excellent condition. Two printwheels included: $2000. Steve Kaplan, 661 Wingate Dr., Sunnyvale, CA 94087, (408) 733-4139.

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BYTE's Ongoing Monitor Box

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Compaq Leads Off

BYTE readers voted Mark Dahmke first-place winner in the January BOMB contest for his product description of "The Compaq Computer," a portable and affordable alternative to the IBM Personal Computer. He will receive the $100 prize. Second place goes to John Smith for his article, "Public Key Cryptography." He will get the $50 kitty. Gregg Williams holds third place for his report from London on "Microcomputing, British Style."

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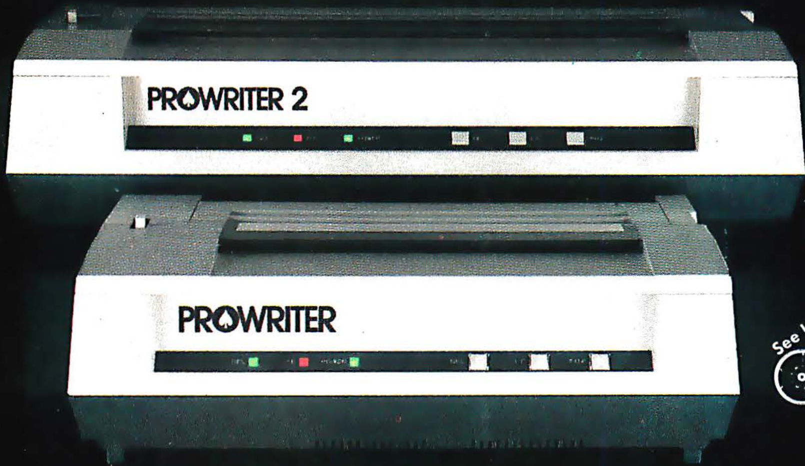
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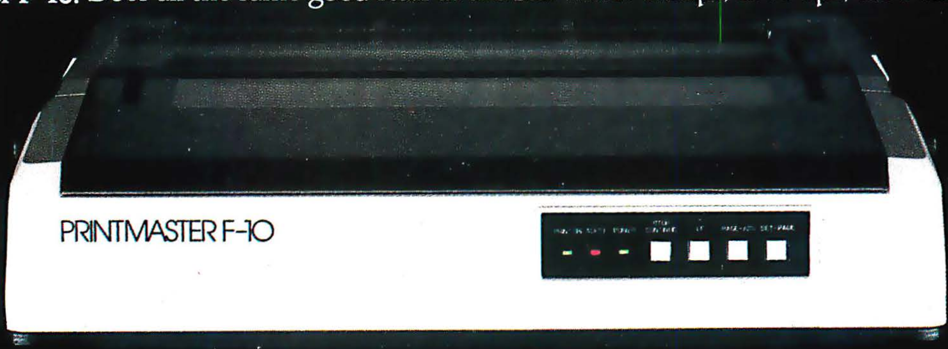
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